Features

- Lead free versions available
- RoHS compliant (lead free version)*
- Bidirectional EMI filtering
- ESD protection
- Protects 6 data lines

Applications

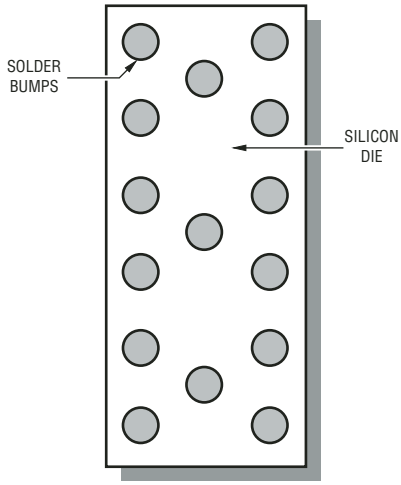
- Cell phones
- PDAs and notebooks
- Digital cameras
- MP3 players and GPS

2FAE-C15R - Integrated Passive & Active Device using CSP

General Information

The 2FAE-C15R device, manufactured using Thin Film on Silicon technology, provides ESD protection and EMI filtering for the data port of portable electronic devices such as cell phones, modems and PDAs. The device incorporates six low pass filter channels where each channel has a series 100 ohm resistor assuring a minimum of -30 dB attenuation from 800 MHz to 3 GHz. The device is suitable for EMI filtering of GSM, CDMA, W-CDMA, WLAN and Bluetooth frequencies.

Each internal and external port of the six channels includes a TVS diode for ESD protection. The ESD protection provided by the component enables a data port to withstand a minimum ±8 KV Contact / ±15 KV Air Discharge per the ESD test method specified in IEC 61000-4-2. The device measures 1.33 mm x 2.96 mm and is available in a 15 bump CSP package intended to be mounted directly onto an FR4 printed circuit board. The CSP device meets typical thermal cycle and bend test specifications without the use of an underfill material.



Electrical & Thermal Characteristics

Electrical Characteristics (T_A = 25 °C unless otherwise noted)	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Unit**
Per Line Specification Resistance	R	80	100	120	Ω
Capacitance @ 2.5 V 1 MHz	C	44	54	64	pF
Rated Standoff Voltage	V_{WM}		5.0		V
Breakdown Voltage @ 1 mA	V_{BR}	6.0			V
Forward Voltage @ 10 mA	V_F		0.8		V
Leakage Current @ 3.3 V	I_R		0.1	0.5	μA
Filter Attenuation @ 800 - 3000 MHz	S21	-30	-35		dB
ESD Protection: IEC 61000-4-2 Contact Discharge Air Discharge		 ±8 ±15			 kV kV
Thermal Characteristics (T_A = 25 °C unless otherwise noted)					
Operating Temperature Range	T_J	-40	25	+85	°C
Storage Temperature Range	T_{STG}	-55	25	+150	°C
Power Dissipation Per Resistor	P_D			100	mW

BOURNS®

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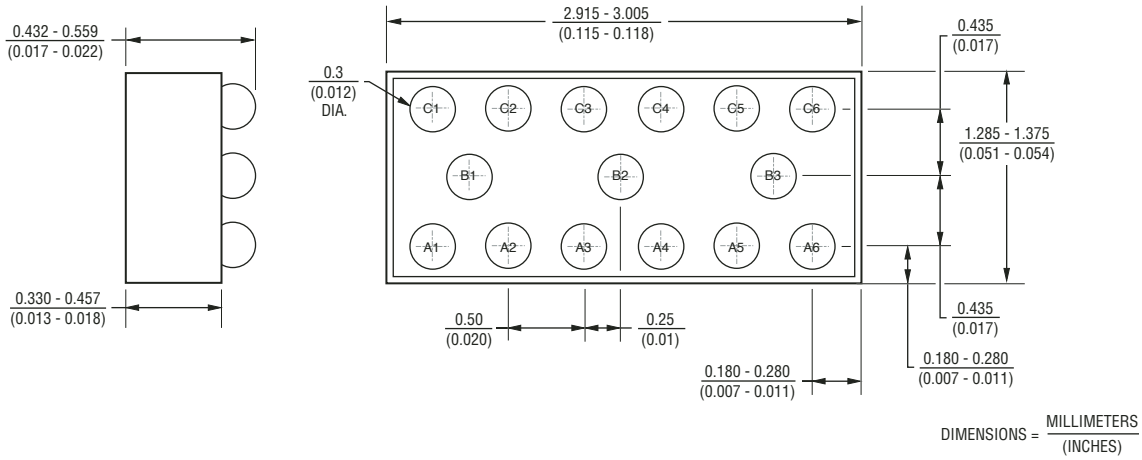
*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

Mechanical Characteristics

This is a silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5 mm and the dimensions for the packaged device are shown below.



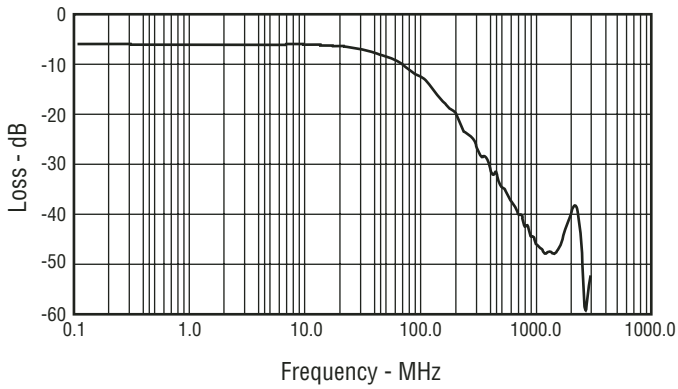
Reliability Data

Reliability data is gathered on an ongoing basis for Bourns® Integrated Passive and Active Devices.

“Package level” testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose (part number 2TAD-C25R). This is a 5 x 5 array featuring 0.5 mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is similar to that of the 2FAE-C15R and is thus deemed suitable for Thermal Cycle testing.

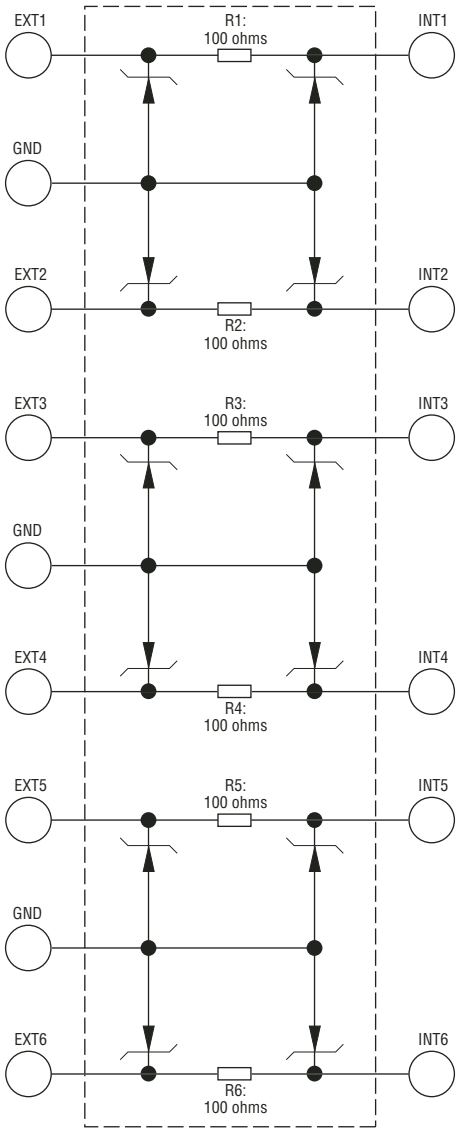
“Silicon level” reliability performance is based on similarity to other integrated passive CSP devices from Bourns.

Frequency Response



Block Diagram

The CSP device block diagram below includes the pin names and basic electrical connections associated with each channel.



PCB Design and SMT Processing

Please consult the “Bourns Design Guide Using CSP” for notes on PCB design and SMT Processing.

How to Order

2 FAE - C15R __

Thinfilm

Model

Chipscale

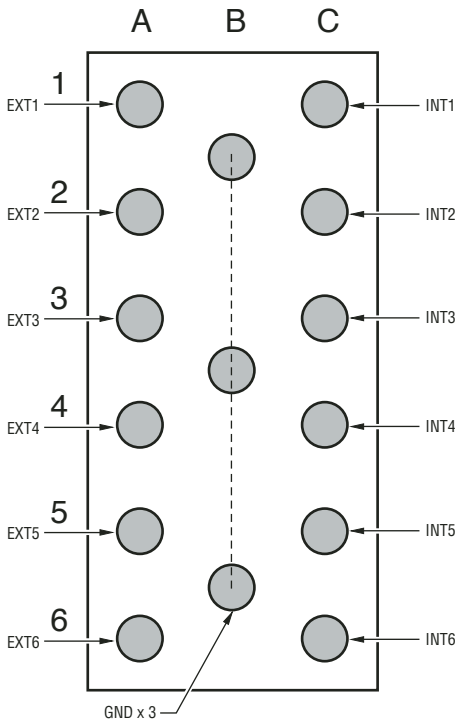
No. of Solder Bumps

Packaging Option
R = Tape and Reel
Packaged 3000 pcs. / 7 ” reel

Terminations
LF = Sn/Ag/Cu (lead free)
Blank = Sn/Pb

Device Pin Out

The pin-out for the device is shown below with the bumps facing up.



Pin Out	Function	Pin Out	Function
A1	EXT1	C1	INT1
A2	EXT2	C2	INT2
A3	EXT3	C3	INT3
A4	EXT4	C4	INT4
A5	EXT5	C5	INT5
A6	EXT6	C6	INT6
B1	GND		
B2	GND		
B3	GND		

Packaging

The surface mount product is packaged in an 8 mm x 4 mm Tape and Reel format per EIA-481 standard.