FUJITSU SEMICONDUCTOR
DATA SHEET

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89560H Series

MB89567H/567HC/P568/PV560

■ DESCRIPTION

The MB89560H series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as I²C interface, timers, 2 ch PWM timers, 8/16-bit timer, 21bit timebase timer, 8 bit PWC timer , 17-bit Watch prescaler, Watch-dog timer, High speed UART, 8-bit SIO, UART/SIO, LCD controller/driver (optional booster), Two type Programmable Pulse Generators (PPG), an A/D converter, and external interrupt.

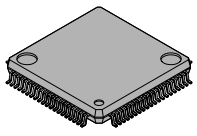
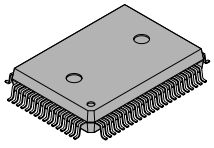
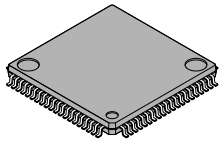
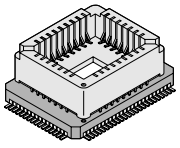
*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8L family CPU core
- Low-voltage operation (when an A/D converter is not used)
- Low current consumption (applicable to the dual-clock system)
- Minimum execution time: 0.32 μs at 12.5 MHz
- I²C interface circuit
- LCD controller/driver : 24 segments x 4 commons (max. 96 pixels, duty LCD mode and Static LCD mode)
- LCD booster function (option)
- Wild register (max. 6 different address locations)
- 10-bit A/D converter: 8 channels

(Continued)

■ PACKAGE

80-pin Plastic LQFP	80-pin Plastic QFP	80-pin Plastic LQFP	80-pin Ceramic MQFP
			
FPT-80P-M05	FPT-80P-M06	FPT-80P-M11	MQP-80C-P01

(Continued)

- Three types of Serial Interface:
  - High Speed UART (Transfer rate from 300 to 192000 bps /10 MHz main clock)
  - 8-bit Serial I/O (SIO)
  - UART/SIO
- Two type of Programmable Pulse Generator(PPG) : 6-bit PPG and 12-bit PPG
- Six types of timer
  - 8 bit PWM 2 channels timers
  - 8/16 bit timer/counter (8 bits x 2 channels or 16 bits x 1 channel)
  - 21bit timebase timer
  - 8 bit PWC timer operation
  - Watch prescaler(17 bits)
  - Watch-dog timer
- I/O ports: max. 50 channels
- External interrupt 1: 8 channels
- External interrupt 2 (wake-up function): 4 channels
- Low-power consumption modes (stop mode, sleep mode, and watch mode)
- LQFP-80 and QFP-80 package
- CMOS technology

■ PRODUCT LINEUP

Part number / Parameter	MB89567H	MB89567HC	MB89P568	MB89PV560
Classification	Mass production products (mask ROM products)		OTP	Piggy-back
ROM size	32 K × 8 bits (internal mask ROM)		48 K × 8 bits (internal PROM)	56 K × 8 bits (external ROM)
RAM size	1K × 8 bits			1K × 8 bits
CPU functions	Number of instructions: : 136 Instruction bit length: : 8 bits Instruction length: : 1 to 3 bytes Data bit length: : 1, 8, 16 bits Minimum execution time: : 0.4 µs/10 MHz Minimum interrupt processing time: : 3.6 µs/10 MHz			
Ports	General-purpose I/O ports (N-channel open drain) : 20 pins (2 shared with I^2C inputs, 16 shared with LCD, 2 shared with other resources) General-purpose I/O ports (CMOS) : 30 pins (shared with resources) Total : 50 pins			
21-bit timebase timer	21 bits Interrupt cycle: 2^{11}, 2^{13}, 2^{16} or 2^{20} t_{inst} *5			
Watchdog timer	Reset generate cycle: min. 2^{20} t_{inst} for main clock, min. 2^{13} t_{inst} for sub clock			
Watch prescaler	17 bits Interrupt cycle: 0.50s, 1.00s, 2.00s, 4.00s/32.768 KHz for subclock			
8/16-bit timer/ counter	Can be operated either as a 2-channel 8-bit timer/counter (Timer 1 and Timer 2, each with its own independent operating clock cycle), or as one 16-bit timer/counter In Timer 1 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable			
8-bit PWM 2 ch timer	8-bit interval timer operation (square wave output capable, operating clock cycle: 1, 8, 16, 64 t_{inst}) 8-bit resolution PWM operation (conversion cycle: 256 to 256 x 64 t_{inst}) 8/16-bit timer/counter output for counter clock selectability			

Parameter \ Part number	MB89567H	MB89567HC	MB89P568	MB89PV560
PWC timer	8-bit timer operation (count clock cycle: 1, 4, 32 t_{inst}) 8-bit reload timer operation (toggle output possible, operating clock cycle: 1 - 32 t_{inst}) 8-bit pulse width measurement (continuous measurement possible: High and Low widths, H to H, L to L, period & H at same time and High & rising to rising)			
10-bit A/D converter*2	10-bit resolution × 8 channels A/D conversion function (conversion time: 60 t_{inst}) Continuous activation by an 8/16-bit timer/counter output or a timebase timer output capable.			
6 bit PPG	Internal 6-bit counter Pulse width and cycle are program selectable			
12 bit PPG	Internal 12-bit counter Pulse width and cycle are program selectable			
I^2C interface*4	Not Available	1 channel Use a 2-wire protocol to communicate with other device		
High speed UART	Transfer data length: 4, 6, 7, 8 bits Transfer rate (300 to 192000 bps /10 MHz main clock) support sub-clock mode			
UART/SIO	Transfer data length: 7, 8 bits for UART, 8 bits for SIO Transfer rate (1201 to 78125 bps / 10 MHz main clock) support sub-clock mode			
8-bit serial I/O	8 bits, LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 2, 8, 32 t_{inst})			
LCD	Common output: 4 (max.) Segment output: 24 (max.) LCD driving power (bias) pins: 4 LCD display RAM size: 12 bytes (24 × 4 bits, max. 96 pixels) Duty LCD mode and Static LCD mode Booster for LCD driving: option Dividing resister for LCD driving: Built-in*1			
Wild register	Maximum of 6-byte data can be assigned in 6 different address. Used to replace any data in the ROM when specific address and data are assigned in Wild register. Wild register can be set up by using different communication methods through the device.			
External interrupt 1 (wake-up function)	8 independent channels (interrupt vector, request flag, request output enable) Edge selectability (rising/falling) Used also for wake-up from stop/sleep mode. (edge detection is also permitted in stop mode.)			
External interrupt 2 (wake-up function)	4 channels (“L” level interrupts, independent input enable). Used also for wake-up from stop/sleep mode. (Low-level detection is also permitted in stop mode.)			
Standby mode	Sleep mode, stop mode and clock mode			
Process	CMOS			
Operating voltage*	3.5 V to 5.5 V	3.5 V to 5.5 V	2.7 to 5.5 V	2.7 to 5.5 V*3

* :Varies with conditions such as the operating frequency. (See “■ Electrical Characteristics.”)

*1 : When booster is used, the bias is reduced by 1/3. it can be selected by mask option.

*2 : When the A/D converter is used, operating voltage must be 3.5V to 5.5V.

*3 : Use MBM27C512-20 as the external ROM (operating voltage: 4.5 V to 5.5 V)

*4 : I^2C is complied to Intel Corp. System Management Bus Rev. 1.0 specification and to the Philips I^2C specification.

*5 : 1 tinst = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock if main clock mode is selected , or 1/2 of the subclock if subclock mode is selected

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89567H MB89567HC	MB89P568-101 MB89P568-102	MB89PV560-101 MB89PV560-102
FPT-80P-M05	○	○	×
FPT-80P-M06	○	○	×
FPT-80P-M11	○	○	×
MQP-80C-P01	×	×	○

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the OTPROM (one-time PROM) products, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- For the MB89PV560, add the current consumed by the EPROM mounted in the piggy-back socket.
- When operating at low speed, the current consumed by the one-time PROM product is greater than for the mask ROM product. However, the current consumption is roughly the same in sleep or stop mode.
- (For more information, see "■ Electrical Characteristics.")

3. Mask Options

The functions available as options and the method of specifying options differ between products.

Before using options check "■ Mask Options."

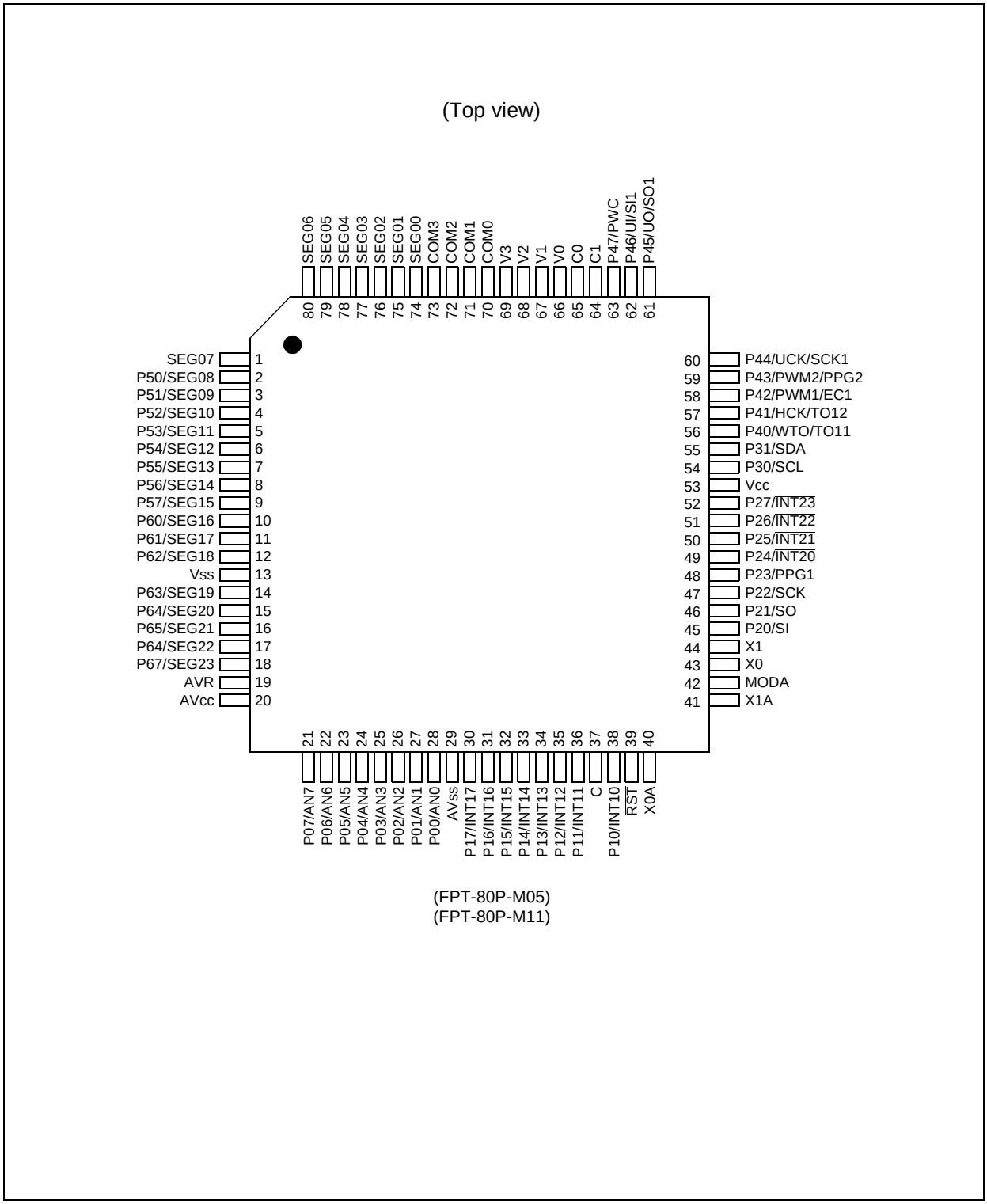
4. Functionalities different between products in MB89560H series

Functionalities	MB89567H	MB89567HC	MB89P568	MB89PV560
Power-on reset wait time	Regulator stab. time + Regulator recovery. time + Osc. stab. time		Regulator stab. time + Osc. stab. time	Osc. stab. time
Wait time for external reset in stop/sub/clock mode or wait time for external interrupt trigger recover from main stop mode	Regulator recovery time + Osc. stab. time		Osc. stab. time	
Port pin pullup resistors	Selectable by software.			Not available.
AD conversion time	60 t_{INST} *			33 t_{INST} *
I^2C noise cancelling circuit	—	Always available independent of ICCR:DMBP bit selection.		Not available when ICCR:DMBP bit is asserted.

Note: For more information on t_{INST} see "■ Electrical Characteristics (4) Instruction cycles"

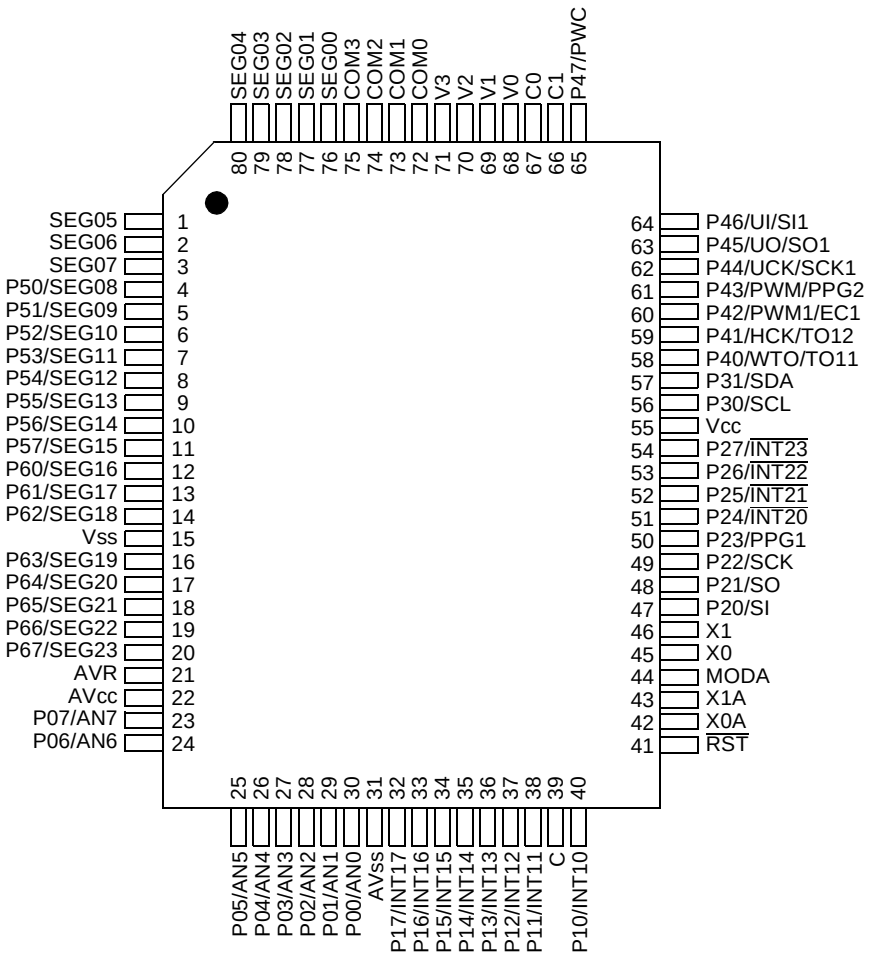
* : Instruction cycle

■ PIN ASSIGNMENT



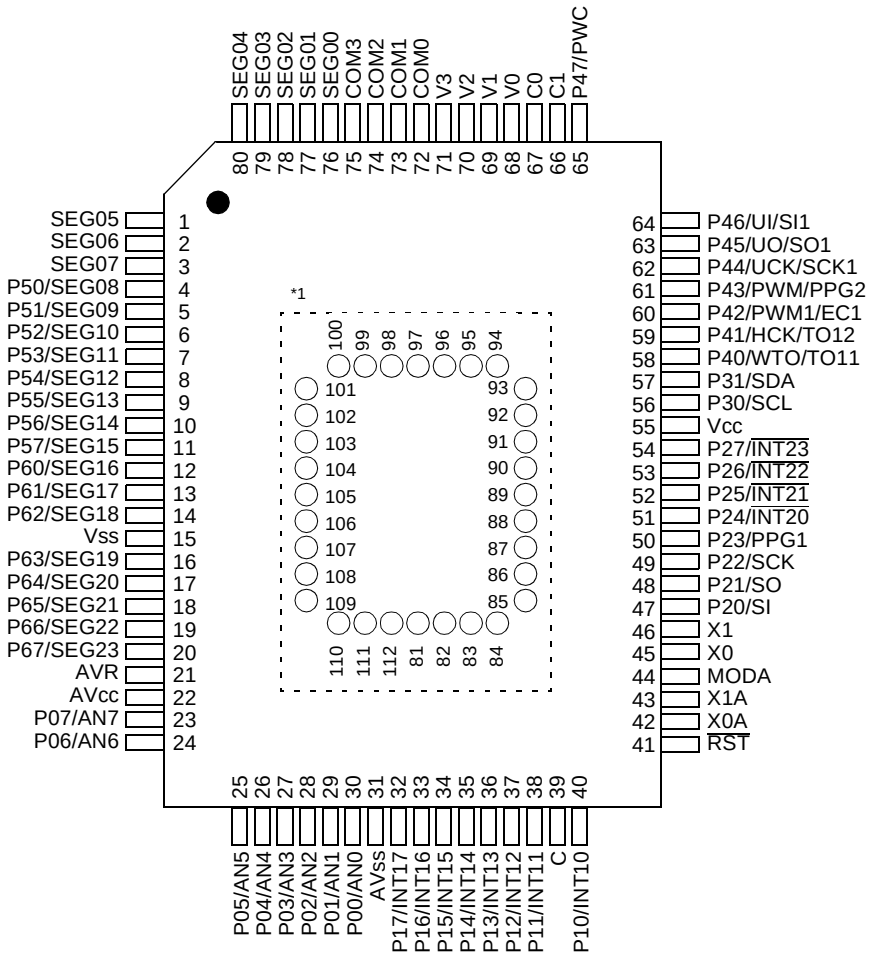
(FPT-80P-M05)
(FPT-80P-M11)

(Top view)



FPT-80P-M06

(Top view)



(MQP-80C-P01)

*1 :Pin assignment on package top (MB89PV560 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	AD2	97	N.C.	105	$\overline{OE}$
82	A15	90	AD1	98	04	106	N.C.
83	A12	91	AD0	99	O5	107	A11
84	AD7	92	N.C.	100	O6	108	A9
85	AD6	93	O1	101	07	109	A8
86	AD5	94	O2	102	O8	110	A13
87	AD4	95	O3	103	$\overline{CE}$	111	A14
88	AD3	96	VSS	104	A10	112	VCC

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type	Function
LQFP*1 LQFP*2	MQFP*3 QFP*4			
43	45	X0	A	Crystal or other resonator connector pins for the main clock. The external clock can be connected to X0. When this is done, be sure to leave X1 open. CR oscillation selectability in model with a mask ROM only.
44	46	X1		
42	44	MODA	C	Memory access mode setting pins. Connect directly to VSS. Hysteresis input type.
39	41	$\overline{RST}$	D	Reset I/O pin This pin is a CMOS output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset request (optional). The internal circuit is initialized by the input of "L".
49 to 52	51 to 54	P24/$\overline{INT20}$ to P27/$\overline{INT23}$	E	General-purpose CMOS I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input is hysteresis input. Selectable pull-up resistor.
30 to 36 ,38	32 to 38,40	P10/INT10 to P17/INT17	E	General-purpose CMOS I/O ports Also serve as input for external interrupt 1 input. External interrupt 1 input is hysteresis input. Selectable pull-up resistor.
60	62	P44/UCK/ SCK1	E	General-purpose CMOS I/O ports Also serve as the clock I/O for the High-speed UART and Serial IO. The peripheral is a hysteresis input type. Selectable pull-up resistor.
61	63	P45/UO/SO1	F	General-purpose CMOS I/O ports Also serves as the data output for the High-speed UART and Serial I/O. The peripheral is a hysteresis input type. Selectable pull-up resistor.
62	64	P46/UI/SI1	G	N-ch open drain general-purpose I/O ports Also serves as the data input for the High-speed UART and Serial I/O. The peripheral is a hysteresis input type.
63	65	P47/PWC	G	N-ch open drain general-purpose I/O port Also serve as the external clock input for PWC. The peripheral is a hysteresis input.
56	58	P40/WTO/ TO11	F	General-purpose CMOS I/O port Also serves as an 8/16-bit timer/counter output and PWC output.

(Continued)

*1: FPT-80P-M05
*2: FPT-80P-M11
*3: MQP-80C-P01
*4: FPT-80P-M06

(Continued)

Pin no.		Pin name	I/O circuit type	Function
LQFP*1 LQFP*2	MQFP*3 QFP*4			
57	59	P41/HCK/ TO12	F	General-purpose CMOS I/O port Also serves as an 8/16-bit timer/counter output. and half of main clock output Selectable pull-up resistor.
45	47	P20/SI	E	General-purpose CMOS I/O port Also serves as the data input for the serial I/O. The peripheral is a hysteresis input type. Selectable pull-up resistor.
46	48	P21/SO	F	General-purpose CMOS I/O port Also serves as the data output for the serial I/O. Selectable pull-up resistor.
47	49	P22/SCK	E	General-purpose CMOS I/O port Also serves as the clock I/O for the serial I/O. The peripheral is a hysteresis input type. Selectable pull-up resistor.
48	50	P23/PPG1	F	General-purpose CMOS I/O port Also serves as the 6 bit programmable pulse generator. Selectable pull-up resistor.
54	56	P30/SCL	G	N-ch open-drain general-purpose I/O port Data I/O pin for I^2C interface
55	57	P31/SDA	G	N-ch open-drain general-purpose I/O port Data I/O pin for I^2C interface
65	67	C0	—	Function as capacitor connection pin in the products with a booster.
64	66	C1	—	Function as capacitor connection pin in the products with a booster.
59	61	P43/PWM2/ PPG2	F	General-purpose CMOS I/O port Also serves PWM wave output for the 8-bit PWM timer 1 and as 12 bit programmable pulse generator output. Selectable pull-up resistor.
58	60	P42/PWM1/ EC1	E	General-purpose CMOS I/O port Also serves as the PWM wave output and external clock for the 8/16 bit timer counter. Selectable pull-up resistor.
21 to 28	23 to 30	P00/AN0 to P07/AN7	J	General-purpose CMOS I/O ports Also serve as the analog input for the A/D converter. Selectable pull-up resistor.
10 to 12 14 to 18	12 to 14 16 to 20	P60/SEG16 to P67/SEG23	H/I	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver segment output.
2 to 9	4 to 11	P50/SEG8 to P57/SEG15	H/I	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver segment output.

(Continued)

*1: FPT-80P-M05
*2: FPT-80P-M11
*3: MQP-80C-P01
*4: FPT-80P-M06

(Continued)

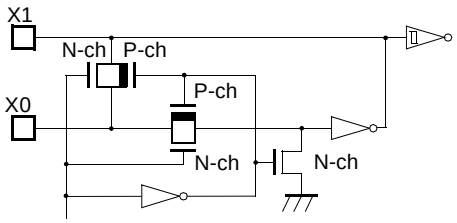
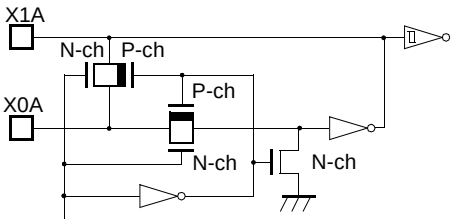
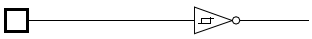
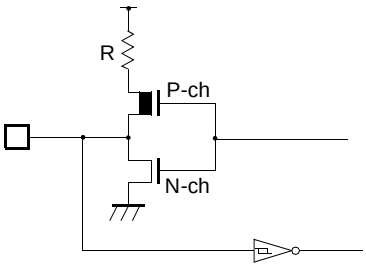
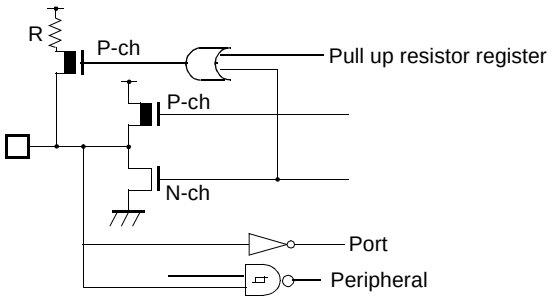
Pin no.		Pin name	I/O circuit type	Function
LQFP*1 LQFP*2	MQFP*3 QFP*4			
74 to 80, 1	1 to 3 76 to 80	SEG0 to SEG7	I	LCD controller/driver segment output-only pins
70 to 73	72 to 75	COM0 to COM3	I	LCD controller/driver common output-only pins
68 to 71	70 to 73	V0 to V3	—	LCD driving power supply pins.
42	44	X0A	B	Crystal or other resonator connector pins for the subclock (Subclock: 32.768 kHz) The external clock can be connected to X0A. When this is done, Be sure to leave X1A open.
43	45	X1A		
55	57	Vcc	—	Power supply pin
39	41	C	—	Capacitor connection pin *5
15	17	Vss	—	Power supply (GND) pin
22	24	AVcc	—	A/D converter power supply pin
21	23	AVR	—	A/D converter reference voltage input pin
31	33	AVss	—	A/D converter power supply pin Use this pin at the same voltage as VSS.

*1: FPT-80P-M05
*2: FPT-80P-M11
*3: MQP-80C-P01
*4: FPT-80P-M06
*5: When MB89PV560-101 or MB89PV560-102 is used, this pin will become a NC pin without internal connection.
When MB89P568-101 or MB89P568-102 is used, this pin will be select a regulator stabilization delay time.
If 5V used in MB89P568-101 or MB89P568-102, this pin must be connected to Vss.
If 3V used in MB89P568-101 or MB89P568-102, this pin must be connected to Vcc.
If MB89567H or MB89567HC is used, 0.1µF capacitor should connect to this pin.

■ PIN DESCRIPTION FOR EXTERNAL EPROM SOCKET (MB89PV560 ONLY)

Pin no.	Pin name	I/O	Function
82 83 84 85 86 87 88 89 90 91	A15 A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	Vss	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
104	A10	O	Address output pin
105	$\overline{OE}/V_{pp}$	O	ROM output enable pin Outputs “L” at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	Vcc	O	EPROM power supply pin
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Main clock (main clock crystal oscillator) • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V • CR oscillation is selectable (mask products only)
B		Subclock (subclock crystal oscillator) • At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V
C		• Hysteresis input
D		• CMOS output • Hysteresis input • At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V
E		• CMOS output • CMOS input • The peripheral is a hysteresis input type. • Selectable pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V

(Continued)

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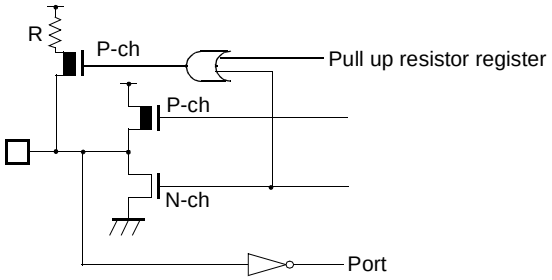
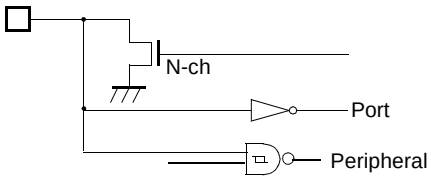
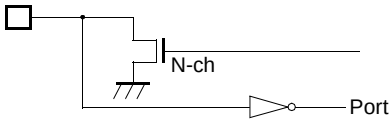
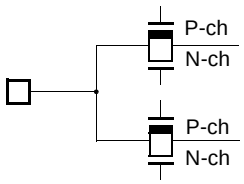
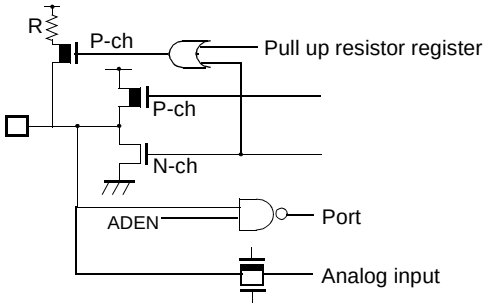
Type	Circuit	Remarks
F		• CMOS output • CMOS input • Selectable pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V
G		• N-ch open-drain input/output • CMOS input • The peripheral is a hysteresis input type.
H		• N-ch open-drain output • CMOS input
I		• LCD controller/driver common/segment output
J		• General CMOS I/O • Analog input (A/D converter) • Selectable pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Pull-up resistors must be disabled when used as an analog input).

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P568

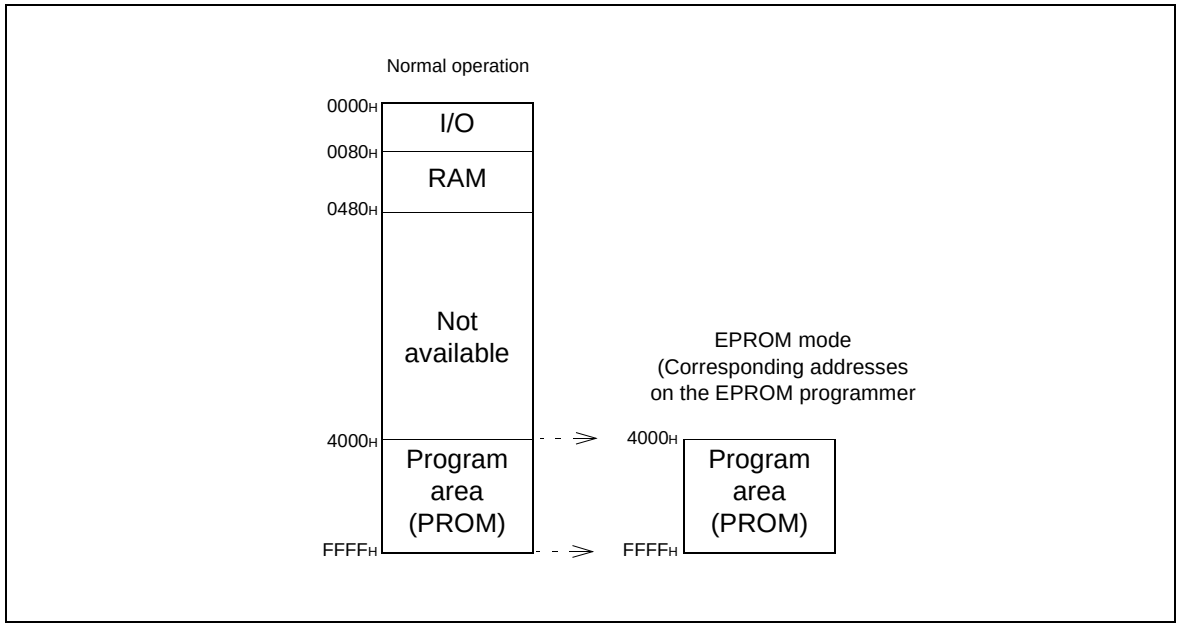
The MB89P568 is an OTPROM version of the MB89567H and MB89567HC.

1. Features

- 48-Kbyte PROM on chip
- Equivalency to the MBM271001A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P568 functions equivalent to the MBM27C1001A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

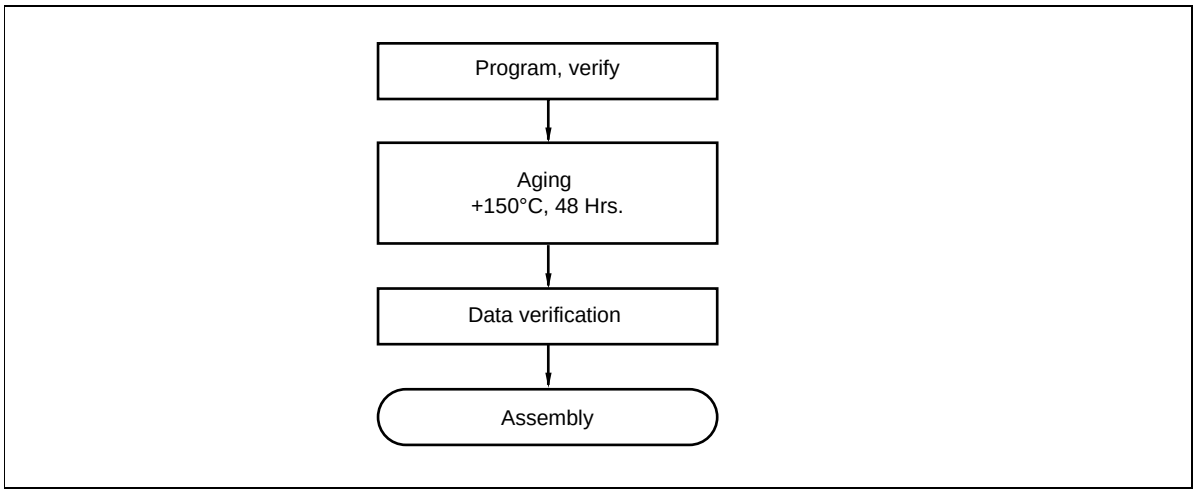
(1) Set the EPROM programmer to the MBM27C1001A.

(2) Load program data into the EPROM programmer at 4000_H to $FFFF_H$

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M05	ROM-80SQF-32DP-8LA
FPT-80P-M06	ROM-80QF-32DP-8LA2
FPT-80P-M11	ROM-80SQF-32DP-8LA

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

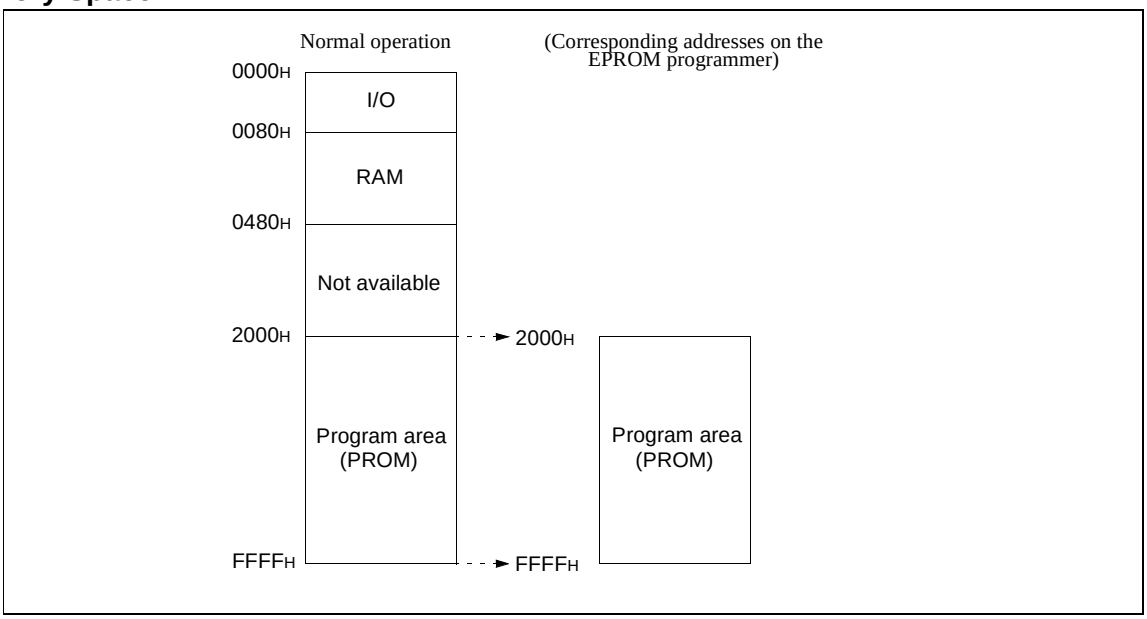
2. Programming Socket Adaptor

To program to the PROM using an EPROM programmer, use the socket adaptor (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adaptor socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-5396-9106

3. Memory Space



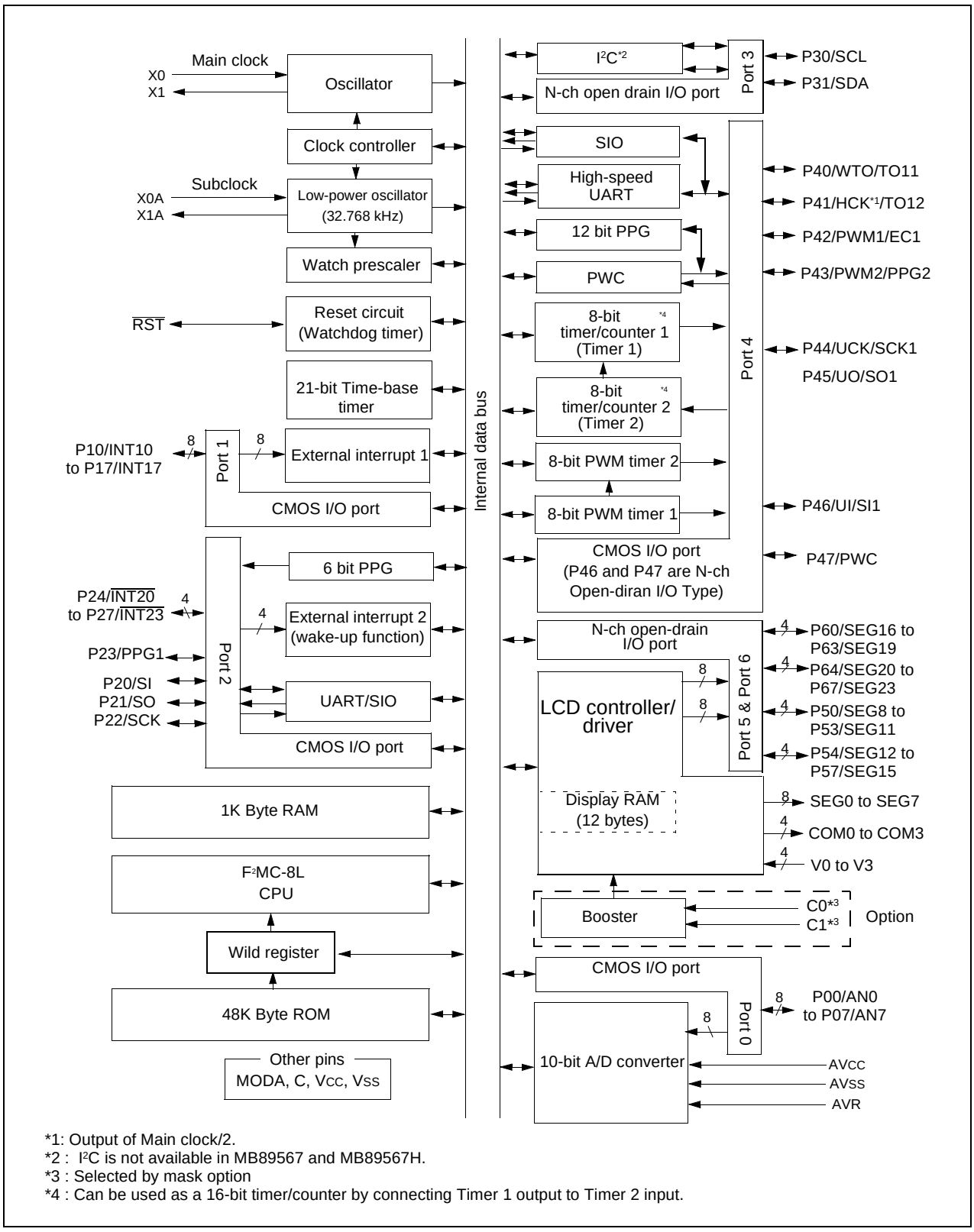
4. Programming to EPROM

(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at 2000H to FFFFH.

(3) Program to 2000H to FFFFH with the EPROM programmer.

■ BLOCK DIAGRAM



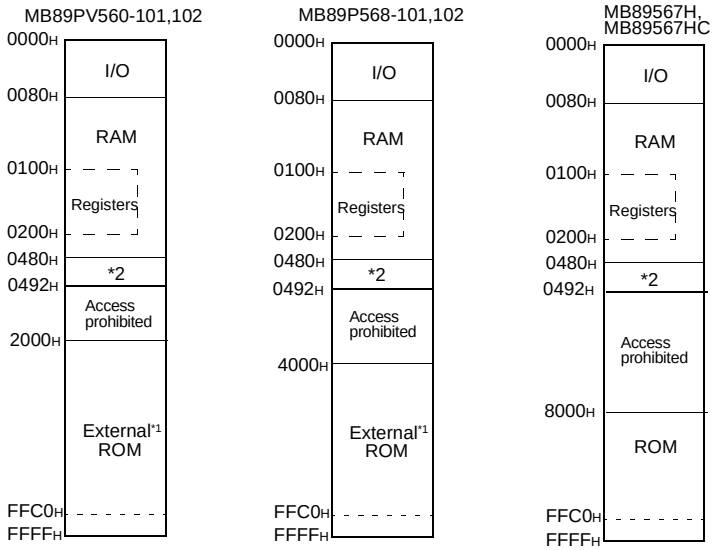
*1: Output of Main clock/2.
*2 : I²C is not available in MB89567 and MB89567H.
*3 : Selected by mask option
*4 : Can be used as a 16-bit timer/counter by connecting Timer 1 output to Timer 2 input.

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89560H series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89560H series is structured as illustrated below.

Memory Space

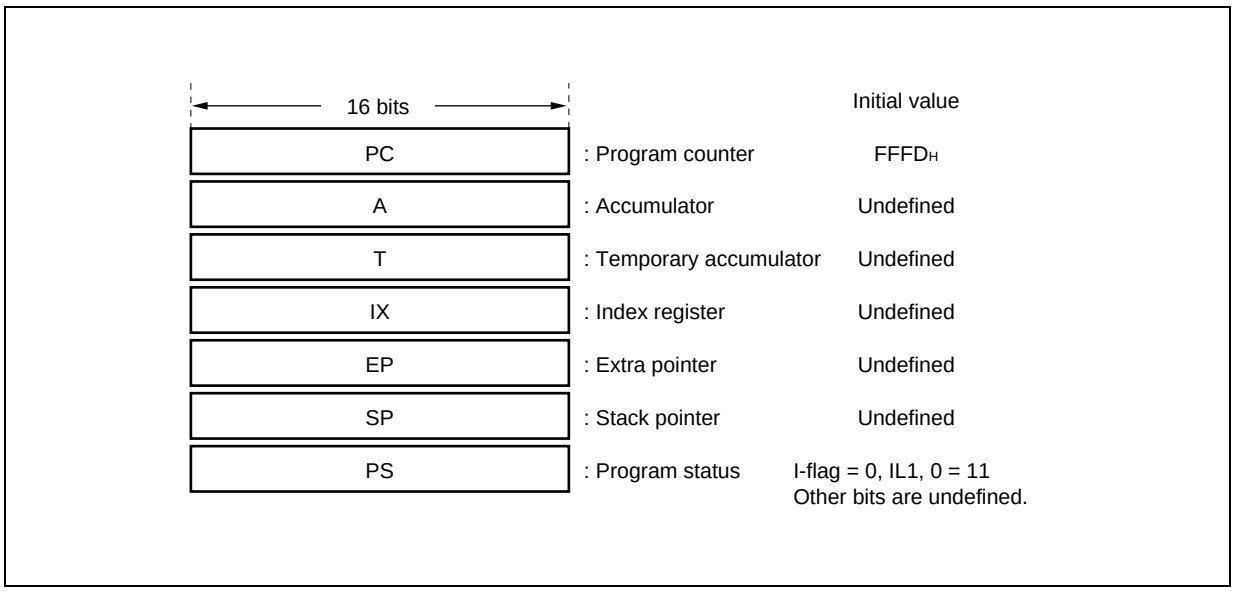


*1: MB89P568-101,102 has OTP ROM inside
*2 : Wild register setting registers

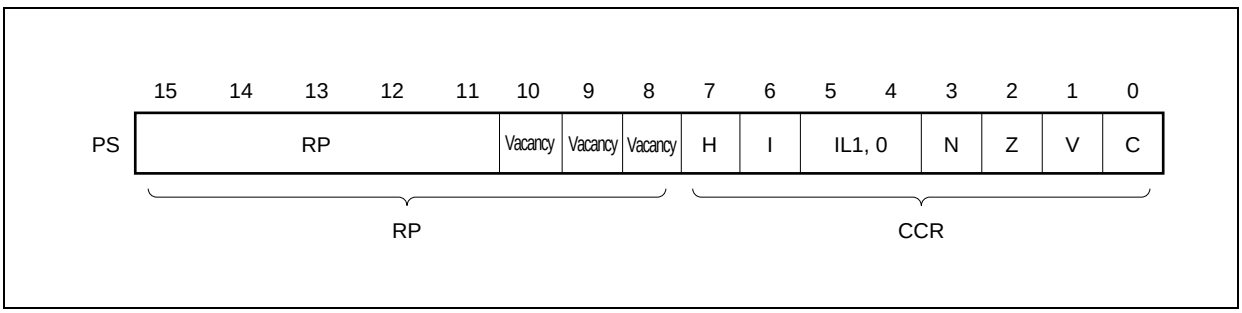
2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

Program counter (PC):	A 16-bit register for indicating specifies instruction storage positions.
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code

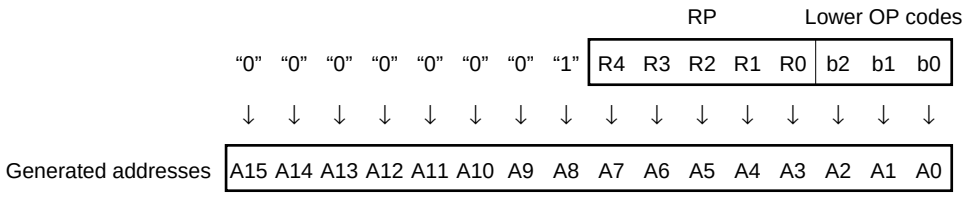


The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

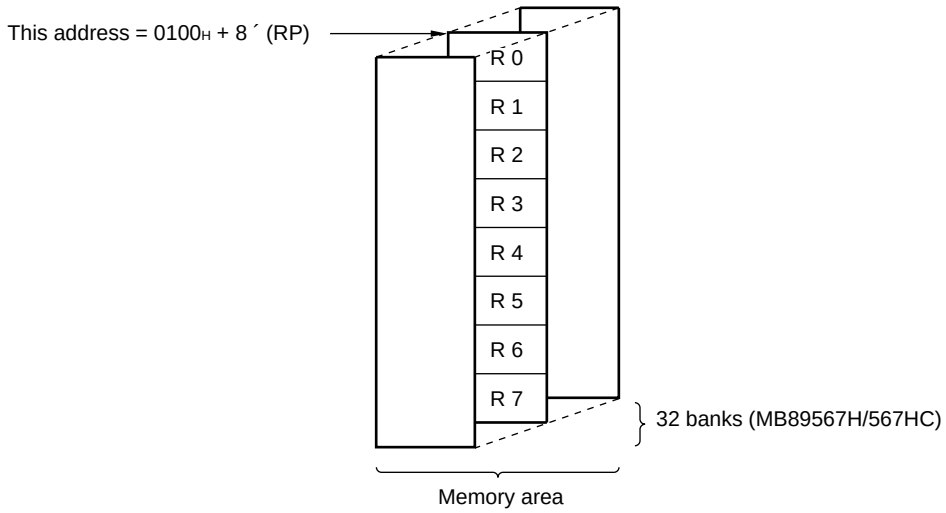
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit resister for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on MB89567H and MB89567HC. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00_H	PDR0	Port 0 data register	R/W	$XXXXXXXX_B$
01_H	DDR0	Port 0 data direction register	W	00000000_B
02_H	PDR1	Port 1 data register	R/W	$XXXXXXXX_B$
03_H	DDR1	Port 1 data direction register	W	00000000_B
04_H - 06_H	(Vacancy)			
07_H	SYCC	System clock control register	R/W	$XXXMM100_B$
08_H	STBC	Standby control register	R/W	$00010XXX_B$
09_H	WDTC	Watchdog timer control register	W	$0XXXXXXX_B$
$0A_H$	TBTC	Timebase timer control register	R/W	$00XXX000_B$
$0B_H$	WPCR	Watch prescaler control register	R/W	$00XX0000_B$
$0C_H$	PDR2	Port 2 data register	R/W	$XXXXXXXX_B$
$0D_H$	DDR2	Port 2 data direction register	R/W	00000000_B
$0E_H$	PDR3	Port 3 data register	R/W	$XXXXXX11_B$
$0F_H$	PDR4	Port 4 data register	R/W	$XXXXXXXX_B$
10_H	DDR4	Port 4 direction register	R/W	00000000_B
11_H	PDR5	Port 5 data register	R/W	00000000_B
12_H	(Vacancy)			
13_H	PDR6	Port 6 data register	R/W	00000000_B
14_H - 19_H	(Vacancy)			
$1A_H$	T2CR	Timer2 control register	R/W	$X000XXX0_B$
$1B_H$	T2DR	Timer2 data register	R/W	$XXXXXXXX_B$
$1C_H$	T1CR	Timer1 control register	R/W	$X000XXX0_B$
$1D_H$	T1DR	Timer1 data register	R/W	$XXXXXXXX_B$
$1E_H$ - 21_H	(Vacancy)			
22_H	SMC11	UART1 mode control register 1	R/W	00000000_B
23_H	SRC1	UART1 mode data register	R/W	$XX011000_B$
24_H	SSD1	UART1 status/data register	R/W	$00100X1X_B$
25_H	SIDR1/SODR1	UART1 data register	R/W	$XXXXXXXX_B$
26_H	SMC12	UART1 mode control register 2	R/W	$XX100001_B$
27_H	CNTR1	PWM control register 1	R/W	00000000_B
28_H	CNTR2	PWM control register 2	R/W	$000X0000_B$
29_H	CNTR3	PWM control register 3	R/W	$X000XXXX_B$
$2A_H$	COMR1	PWM compare register 1	W	$XXXXXXXX_B$
$2B_H$	COMR2	PWM compare register 2	W	$XXXXXXXX_B$
$2C_H$	PCR1	PWC pulse width control register 1	R/W	$000XX000_B$
$2D_H$	PCR2	PWC pulse width control register 2	R/W	00000000_B
$2E_H$	RLBR	PWC reload buffer register	R/W	$XXXXXXXX_B$
$2F_H$	SMC21	UART2/SIO mode control register	R/W	00000000_B
30_H	SMC22	UART2/SIO mode control register 2	R/W	00000000_B

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
31H	SSD2	UART2/SIO status/data register	R/W	00001XXXB
32H	SIDR2/SODR2	UART2/SIO data register	R/W	XXXXXXXXB
33H	SRC2	UART2/SIO rate control register	R/W	XXXXXXXXB
34H	ADC1	A/D control register 1	R/W	X00000X0B
35H	ADC2	A/D control register 2	R/W	X0000001B
36H	ADDL	A/D data register L	R/W	XXXXXXXXB
37H	ADDH	A/D data register H	R/W	XXXXXXXXB
38H	RCR21	PPG control register 1(PPG2)	R/W	00000000B
39H	RCR23	PPG control register 2(PPG2)	R/W	0X000000B
3AH	RCR22	PPG control register 3(PPG2)	R/W	XX000000B
3BH	RCR24	PPG control register 4(PPG2)	R/W	XX000000B
3CH - 3EH	(Vacancy)			
3FH	EIC1	External interrupt 1 control register 1	R/W	00000000B
40H	EIC2	External interrupt 1 control register 2	R/W	00000000B
41H	EIC3	External interrupt 1 control register 3	R/W	00000000B
42H	EIC4	External interrupt 1 control register 4	R/W	00000000B
43H - 50H	(Vacancy)			
51H	IBSR	I²C bus status register	R	00000000B
52H	IBCR	I²C bus control register	R/W	00000000B
53H	ICCR	I²C clock control register	R/W	000XXXXXB
54H	IADR	I²C address register	R/W	XXXXXXXXB
55H	IDAR	I²C data register	R/W	XXXXXXXXB
56H	EIE2	External interrupt 2 enable register	R/W	XXXX0000B
57H	EIF2	External interrupt 2 flag register	R/W	XXXXXXX0B
58H	RCR1	PPG control register 1(PPG1)	R/W	00000000B
59H	RCR2	PPG control register 2(PPG1)	R/W	0X000000B
5AH	CKR	Clock Output control register	R/W	00000000B
5BH	LCR1	LCD controller/driver control register 1	R/W	00010000B
5CH	LCR2	LCD controller/driver control register 1	R/W	00000000B
5DH	LCR3	LCD controller/driver control register 1	R/W	XX000000B
5EH	LDR1	LCD data register 1	R/W	XXXXXXXXB
5FH	(Vacancy)			
60H - 6FH	VRAM	Display RAM	R/W	XXXXXXXXB
70H	SMR	Serial I/O mode register	R/W	00000000B
71H	SDR	Serial I/O data register	R/W	XXXXXXXXB
72H	PURR0	Pull-up resister register 0	R/W	11111111B
73H	PURR1	Pull-up resister register 1	R/W	11111111B
74H	PURR2	Pull-up resister register 2	R/W	11111111B
75H	PURR4	Pull-up resister register 4	R/W	XX111111B
76H	(Vacancy)			

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
77H	WREN	Wild register enable register	R/W	XX000000B
78H	WROR	Wild register data test register	R/W	XX000000B
79H	ADEN	A/D port input enable register	R/W	11111111B
7AH	(Vacancy)			
7BH	ILR1	Interrupt level setting register 1	W	11111111B
7CH	ILR2	Interrupt level setting register 2	W	11111111B
7DH	ILR3	Interrupt level setting register 3	W	11111111B
7EH	ILR4	Interrupt level setting register 4	W	11111111B
7FH	ITR	Interrupt test register	Access Prohibited	11111111B

■ EXTEND I/O MAP

Address	Register name	Register description	Read/Write	Initial value
480H	WRARH1	Wild register high-byte address register1	R/W	XXXXXXXXB
481H	WRARL1	Wild register low-byte address register1	R/W	XXXXXXXXB
482H	WRDR1	Wild register data register1	R/W	XXXXXXXXB
483H	WRARH2	Wild register high-byte address register2	R/W	XXXXXXXXB
484H	WRARL2	Wild register low-byte address register2	R/W	XXXXXXXXB
485H	WRDR2	Wild register data register2	R/W	XXXXXXXXB
486H	WRARH3	Wild register high-byte address register3	R/W	XXXXXXXXB
487H	WRARL3	Wild register low-byte address register3	R/W	XXXXXXXXB
488H	WRDR3	Wild register data register3	R/W	XXXXXXXXB
489H	WRARH4	Wild register high-byte address register4	R/W	XXXXXXXXB
48AH	WRARL4	Wild register low-byte address register4	R/W	XXXXXXXXB
48BH	WRDR4	Wild register data register4	R/W	XXXXXXXXB
48CH	WRARH5	Wild register high-byte address register5	R/W	XXXXXXXXB
48DH	WRARL5	Wild register low-byte address register5	R/W	XXXXXXXXB
48EH	WRDR5	Wild register data register5	R/W	XXXXXXXXB
48FH	WRARH6	Wild register high-byte address register6	R/W	XXXXXXXXB
490H	WRARL6	Wild register low-byte address register6	R/W	XXXXXXXXB
491H	WRDR6	Wild register data register6	R/W	XXXXXXXXB

- **Read/write access symbols**
  R/W: Readable and writable
  R: Read-only
  W: Write-only

- **Initial value symbols**
  0: The initial value of this bit is “0”.
  1: The initial value of this bit is “1”.
  X: The initial value of this bit is undefined.
  M: The initial value of this bit is determined by mask option.

Note:Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	MB89567H, MB89567HC, MB89P568 and MB89PV560
	AVR	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
Program voltage	V_{PP}	$V_{SS} - 0.6$	V_{SS} +13.0	V	Only for the MB89P568
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	For pins other than P30 and P31
		$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	For P30 and P31
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	For pins other than P30 and P31
		$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	For P30 and P31
“H” level maximum output current	I_{OL}	—	15	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AVR and AV_{CC} + 0.3V does not exceed V_{CC}, such as when power is turned on.

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	3.5*	5.5*	V	For MB89567H and MB89567HC
		3.0	5.5	V	Retains the RAM state in stop mode for MB89567H and MB89567HC
		2.7*	5.5*	V	For MB89PV560 and MB89P568
		1.5	5.5	V	Retains the RAM state in stop mode for MB89PV560 and MB89P568
A/D converter reference input voltage	AVR	3.5	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

* : These values depend on the operating conditions and the analog assurance range. See Figure 1, Figure 2, Figure 3 and “5. A/D Converter Electrical Characteristics.”

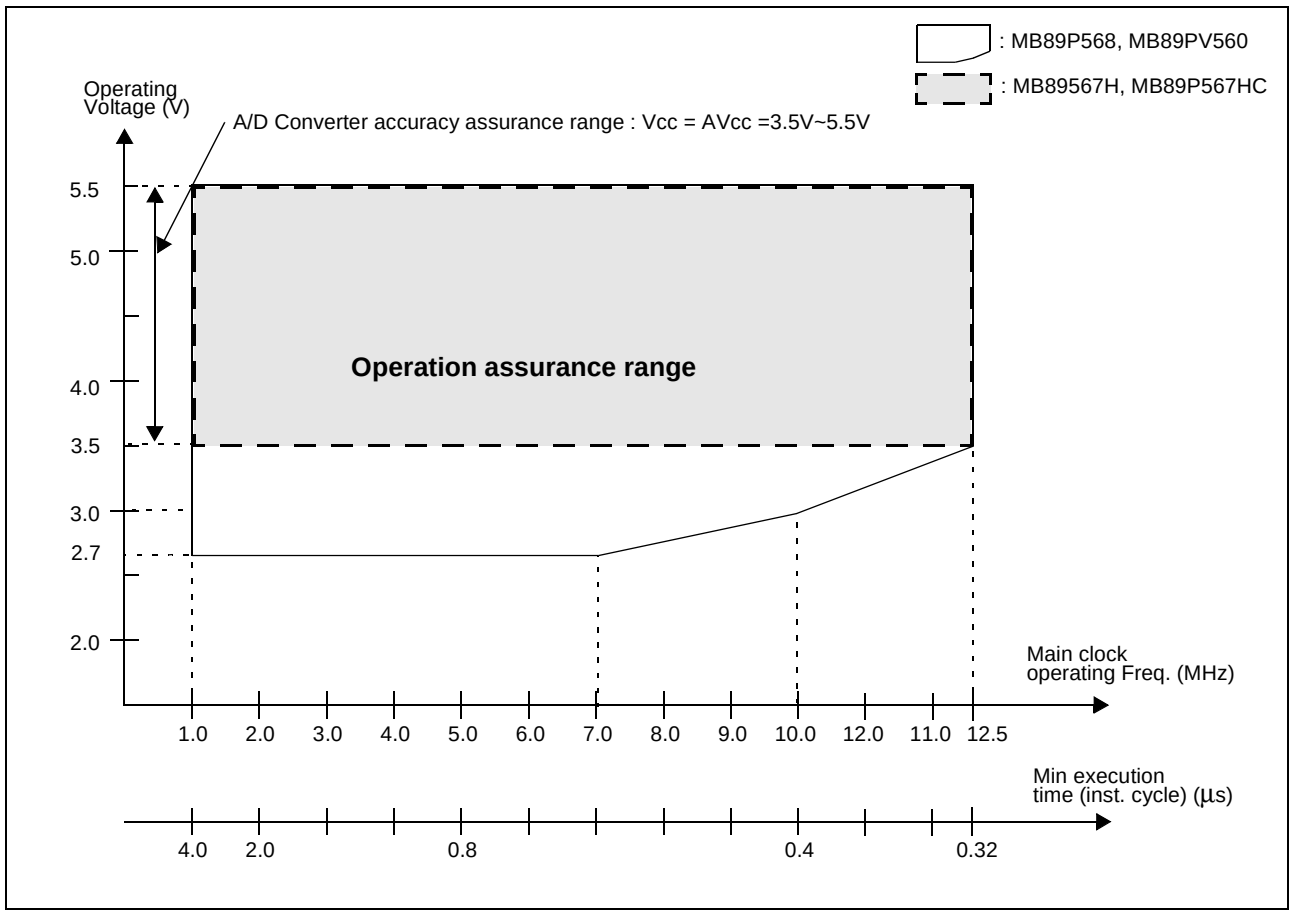


Figure 1 Operating Voltage vs. Main Clock Operating Frequency

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37 P40 to P45	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MODA INT10 to INT17, INT20 to INT23, SI,SCK,EC1,UCK, SCK1,UI,SI1,PWC	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHSMB}	SDL, SDA	—	V_{SS} +1.4	—	V_{SS} + 5.5	V	SMB input buffer selected
	V_{IHI2C}		—	0.7 V_{CC}	—	V_{CC} + 0.3	V	I2C input buffer selected
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P40 to P45	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MODA INT10 to INT17, INT20 to INT23, SI,SCK,EC1,UCK, SCK1,UI,SI1,PWC	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILSMB}	SCL, SDA	—	V_{SS} - 0.3	—	V_{SS} + 0.6	V	SMB input buffer selected
	V_{ILI2C}		—	V_{SS} – 0.3	—	0.3 V_{CC}	V	I2C input buffer selected
Open-drain output pin application voltage	V_D	P60 to P67 P50 to P57 P46, P47 P30, P31	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P40 to P45	I_{OH} = –2.0 mA	4.0	—	—	V	
		P20 to P27	I_{OH} = –15.0 mA					
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P30 to P31, P40 to P47, P50 to P57, P60 to P67, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
		P20 to P27	I_{OL} = 15.0 mA					

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current	I_{CC1}	V_{CC} ‘	F_{CH} = 10.0 MHz V_{CC} = 5.0 V t_{inst}*3 = 0.4 µs Main clock run mode	—	15	20	mA	MB89PV560 MB89P568
				—	6	10		MB89567H MB89567HC
	I_{CC2}		F_{CH} = 10.0 MHz V_{CC} = 5.0 V t_{inst}*3 = 6.4 µs Main clock run mode	—	5	8.5	mA	MB89PV560 MB89P568
				—	1.5	3		MB89567H MB89567HC
	I_{CCS1}		F_{CH} = 10.0 MHz V_{CC} = 5.0 V t_{inst}*3 = 0.4 µs Main clock sleep mode	—	5	7	mA	MB89PV560 MB89P568
				—	2	4		MB89567H MB89567HC
	I_{CCS2}		F_{CH} = 10.0 MHz V_{CC} = 5.0 V t_{inst}*3 = 6.4 µs Main clock sleep mode	—	1.5	3	mA	MB89PV560 MB89P568
				—	1	2		MB89567H MB89567HC
	I_{CCL}		F_{CL} = 32.768 kHz V_{CC} = 5.0 Subclock mode	—	3	7	mA	MB89PV560 MB89P568
				—	20	50	µA	MB89567H MB89567HC
	I_{CCLS}		F_{CL} = 32.768 kHz V_{CC} = 5.0 V Subclock sleep mode	—	30	50	µA	MB89PV560 MB89P568
				—	15	30		MB89567H MB89567HC
	I_{CCT}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V • Watch mode • Main clock stop mode	—	5	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode	—	3	10	µA	
	I_A	AV_{CC}	F_{CH} = 10.0 MHz,	—	4	6	mA	when A/D conversion is activated
	I_{AH}		F_{CH} = 10.0 MHz, T_A = +25°C,	—	1	5	µA	when A/D conversion is stopped

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0V, , AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input leakage current	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P40 to P45, P50 to P57, P60 to P67	0.0V < V_I < V_{CC}	-5	—	+5	µA	Without pull-up Resister
		MODA		-10	—	+10	µA	
Open-drain output leakage current	I_{LIOD}	P30, P32 P46, P47	0.0V < V_I < V_{ss} + 5.5V	—	—	+5	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P45, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistor selected except RST
LCD divided resistance	R_{LCD}	—	Between V_{CC} and V_{SS}	300	500	750	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COM0 to 3	V1 to V3 = 5.0V	—	—	2.5	kΩ	
SEG0 to 23 output impedance	R_{VSEG}	SEG0 to 23		—	—	15	kΩ	
LCD controller/ driver leakage current	I_{LCDL}	V0 to V3, COM0 to 3 SEG0 to 23	—	—	—	±1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

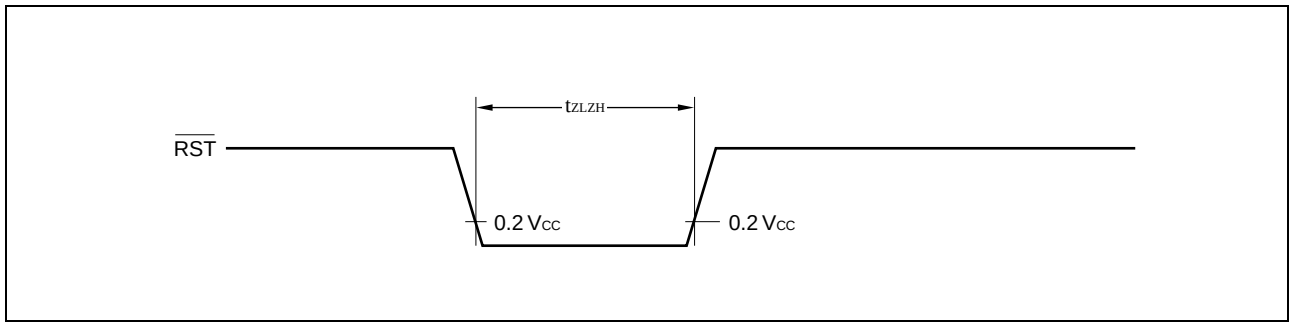
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}*	—	ns	

* : t_{HCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.

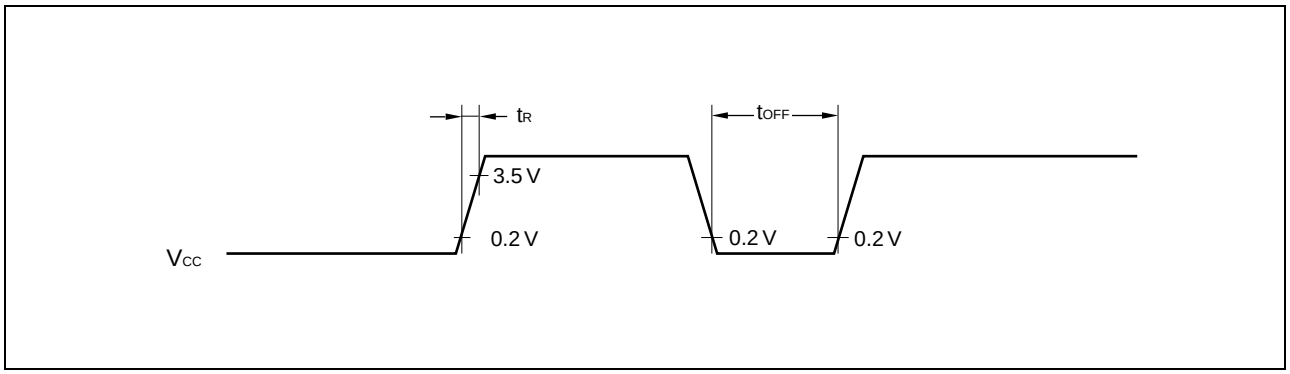


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	0.5	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
For example, when the main clock is operating at 10 MHz (F_{CH}) and the oscillation stabilization time select option has been set to $2^{18}/F_{CH}$, the oscillation stabilization delay time is 26.2 ms. Therefore, the maximum value of power supply rising time is about 26.2 ms.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

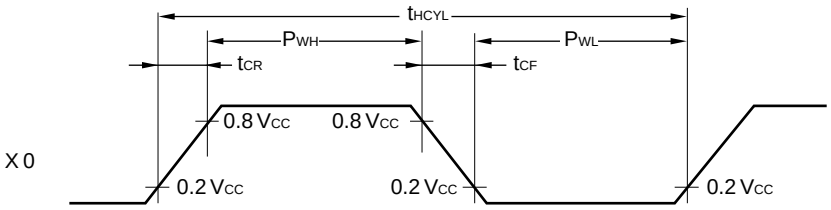


(3) Clock Timing

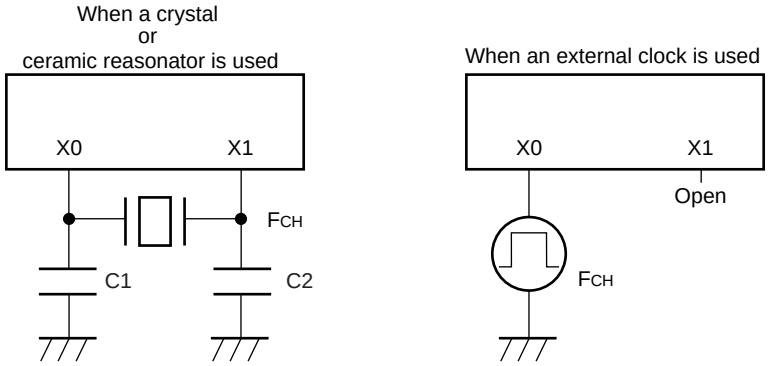
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	12.5	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	80	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
	P_{WH} P_{WL}	X0A	—	15.2	—	µs	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	External clock

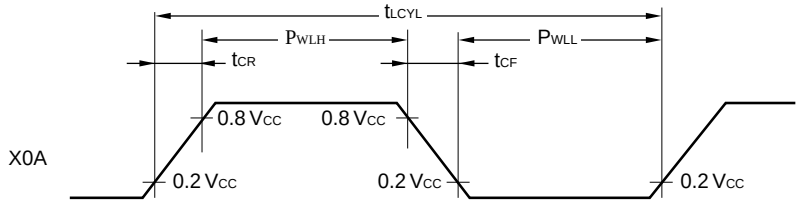
X0 and X1 Timing and Conditions



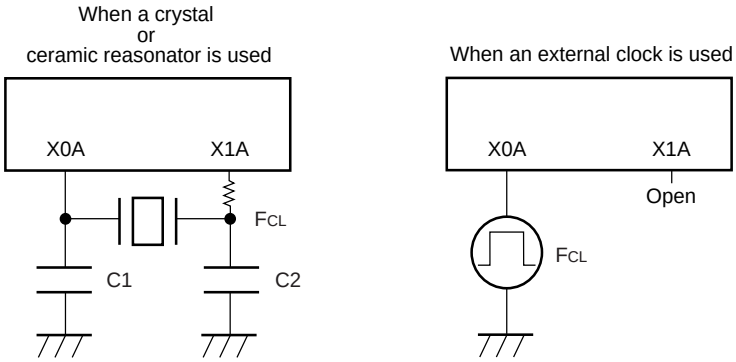
Main Clock Conditions



X0A and X1A Timing and Conditions



Subclock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	t_{inst} = 0.32µs when operating at F_{CH} = 12.5 MHz ($4/F_{CH}$)
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

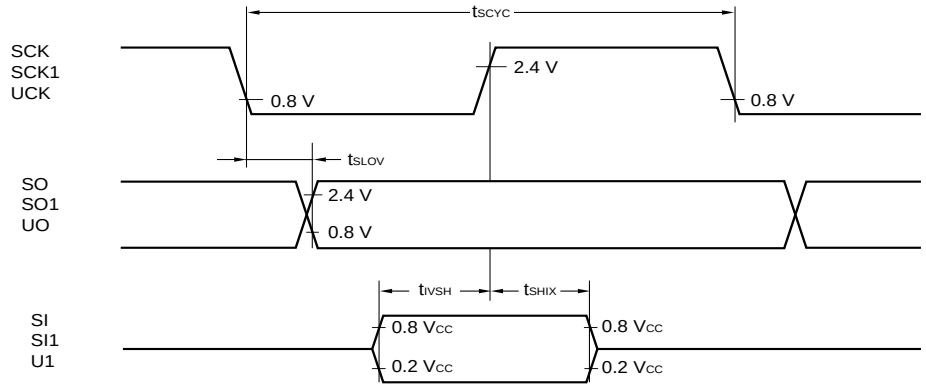
(5) Serial I/O Timing

(V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

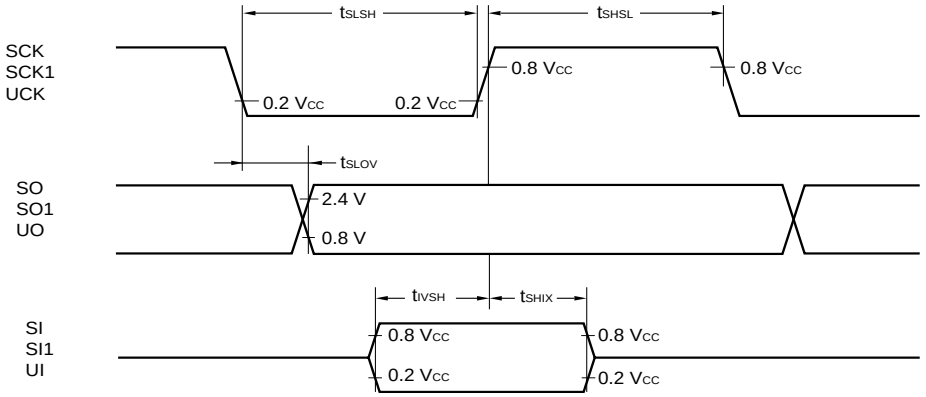
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK, SCK1, UCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO, SCK1, SO1, UCK, UO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK, SI1, SCK1, UI, UCK		200	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI, SCK1, SI1, UCK, UI		200	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK, SCK1, UCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO, SCK1, SO1, UCK, UO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK, SI1, SCK1, UI, UCK		200	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI, SCK1, SI1, UCK, UI		200	—	ns	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

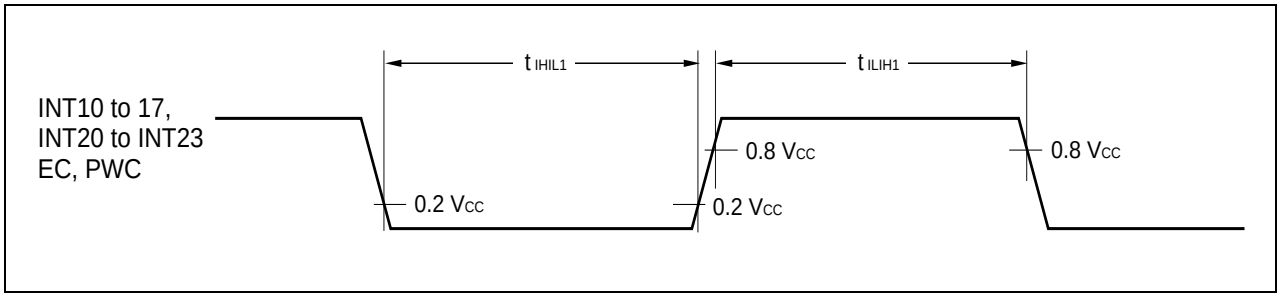


(6) Peripheral Input Timing

(V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT10 to INT17, INT20 to INT23, EC, PWC	—	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}			2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

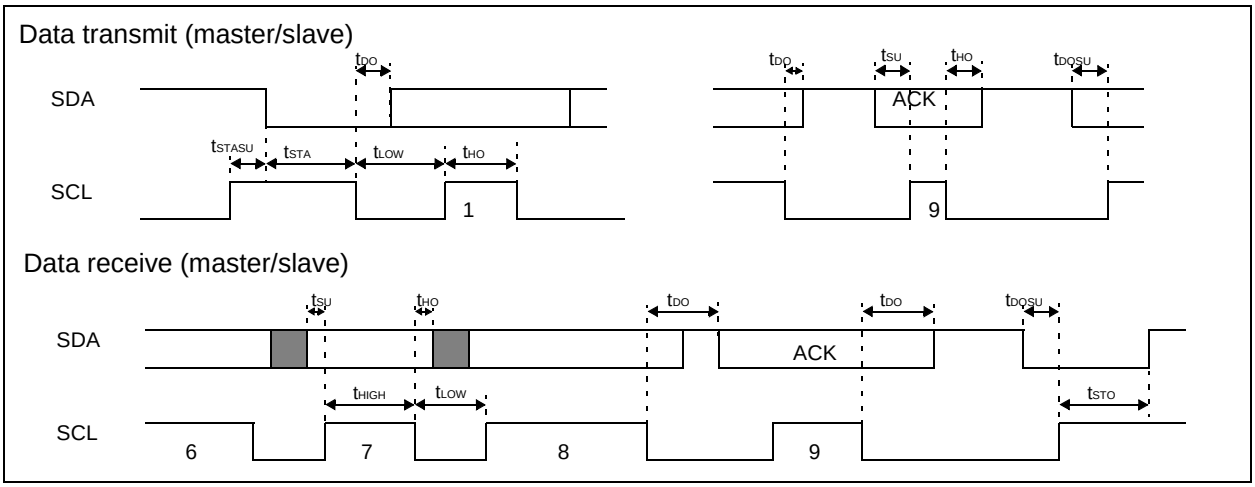


(7) I²C timing

(Vcc = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Start condition output	t_{STA}	SCL SDA		1/4t_{INST} x m x n - 20	1/4t_{INST} x m x n + 20	ns	master mode
Stop condition output	t_{STO}	SCL SDA		1/4t_{INST} x (m x n + 8) - 20	1/4t_{INST} x (m x n + 8) + 20	ns	master mode
Start condition detect	t_{STA}	SCL SDA		1/4t_{INST} x 6 + 40	—	ns	
Stop condition detect	t_{STO}	SCL SDA		1/4t_{INST} x 6 + 40	—	ns	
Re-start condition output	t_{STASU}	SCL SDA		1/4t_{INST} x (m x n + 8) - 20	1/4t_{INST} x (m x n + 8) + 20	ns	master mode
Re-start condition detect	t_{STASU}	SCL SDA		1/4t_{INST} x 4 + 40	—	ns	
SCL output LOW width	t_{LOW}	SCL		1/4t_{INST} x m x n - 20	1/4t_{INST} x m x n + 20	ns	master mode
SCL output HIGH width	t_{HIGH}	SCL		1/4t_{INST} x (m x n + 8) - 20	1/4t_{INST} x (m x n + 8) + 20	ns	master mode
SDA output delay	t_{DO}	SDA		1/4t_{INST} x 4 - 20	1/4t_{INST} x 4 + 20	ns	
SDA output setup time after interrupt	t_{DOSU}	SDA		1/4t_{INST} x 4 - 20	—	ns	
SCL input LOW pulse width	t_{LOW}	SCL		1/4t_{INST} x 6 + 40	—	ns	
SCL input HIGH pulse width	t_{HIGH}	SCL		1/4 t_{INST} x 2 + 40	—	ns	
SDA input setup time	t_{SU}	SDA		40	—	ns	
SDA hold time	t_{HO}	SDA		0	—	ns	

- For information in t_{INST}, see "(4) Instruction Cycle".
- m is defined in the ICCR CS4 and CS3 (bit 4 to bit 3)
- n is defined in the ICCR CS2 to CS0 (bit 2 to bit 0)



5. A/D Converter Electrical Characteristics

(1) For MB89567H A/D Converter

(AVcc=3.5~5.5V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	10	bit	1LSB = AVR/1024
Total error			AVR=AV_{CC}	—	—	±5.0	LSB	
Non-linearity error				—	—	±2.5	LSB	
Differential linearity error				—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	—		AVR - 3.5 LSB	AVR + 0.5 LSB	AVR + 4.5 LSB	mV	
Full-scale transition voltage	V_{FST}			AVR – 6.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	
Interchannel disparity	—			—	—	4	LSB	1LSB = AVR/1024
A/D mode conversion time *3			—	—	60 t_{inst}*1	—	µs	
A/D Sampling time				—	16 t_{inst}*1	—		
Analog port input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	V_{AIN}			AVss	—	AVR	V	
Reference voltage	—	AVR		AVss+3.5	—	AV_{CC}	V	
Reference voltage supply current	I_R		A/D is Activated	—	400	—	µA	
	I_{RH}		A/D is Stopped	—	—	5	µA	*2

* : 1 For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

* : 2 When A/D conversion is not in operation, and the CPU is in STOP mode.

* : 3 Included sampling time

(2) For MB89P568 A/D Converter

(AVcc=3.5~5.5V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	10	bit	1LSB = AVR/1024
Total error			AVR=AV_{CC}	—	—	±3.0	LSB	
Non-linearity error				—	—	±2.5	LSB	
Differential linearity error				—	—	±1.9	LSB	
Zero transition voltage	V_{OT}			AVR - 1.5 LSB	AVR + 0.5 LSB	AVR + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}			AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	
Interchannel disparity	—			—	—	4	LSB	1LSB = AVR/1024
A/D mode conversion time *3			—	—	60 t_{inst}*1	—	µs	
A/D Sampling time				—	16 t_{inst}*1	—		
Analog port input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	V_{AIN}			AVss	—	AVR	V	
Reference voltage	—	AVR		AVss+3.5	—	AV_{CC}	V	
Reference voltage supply current	I_R		A/D is Activated	—	400	—	µA	
	I_{RH}		A/D is Stopped	—	—	5	µA	*2

* : 1 For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

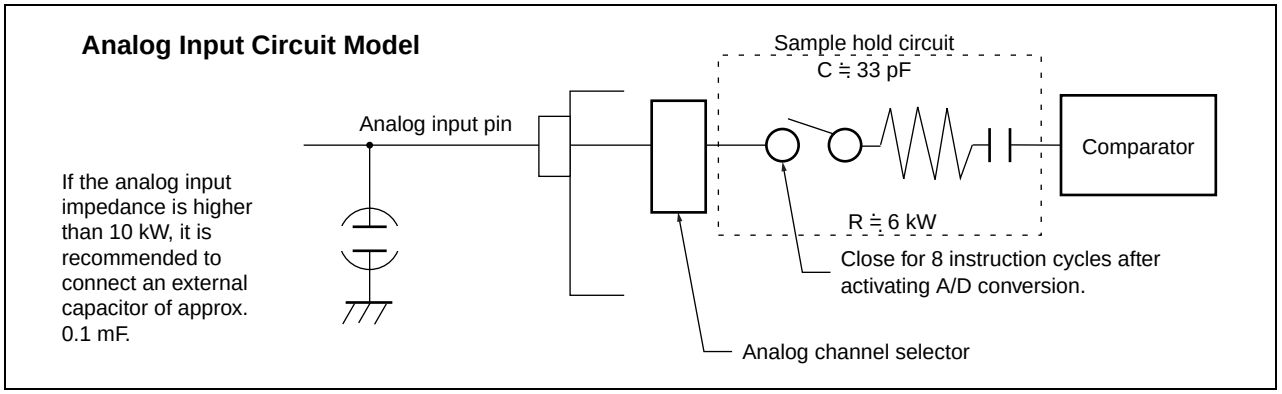
* : 2 When A/D conversion is not in operation, and the CPU is in STOP mode.

* : 3 Included sampling time

* :

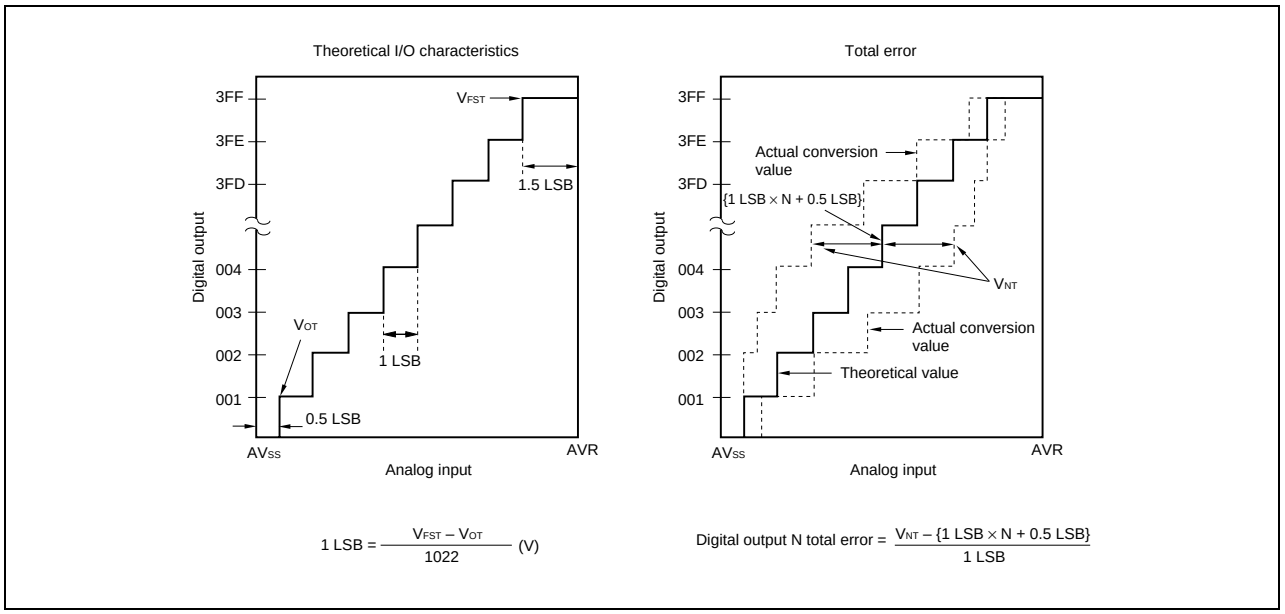
(3) Precautions

- The smaller the | AVR–AVSS |, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions:
  Output impedance of the external circuit < Approx. 10 kΩ
- If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10MHz oscillation.)



(4) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise



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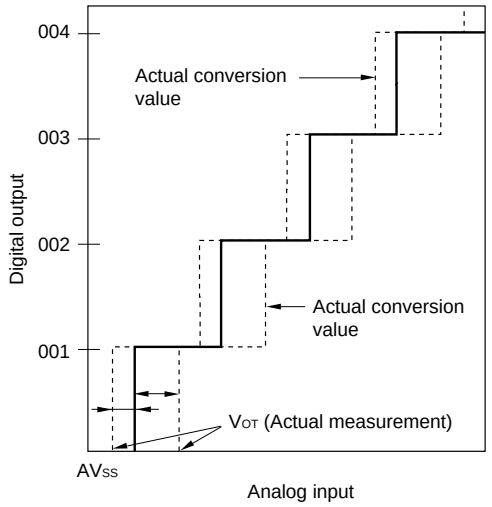
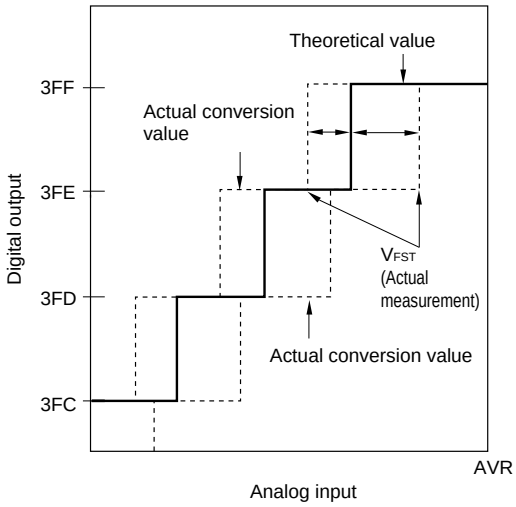
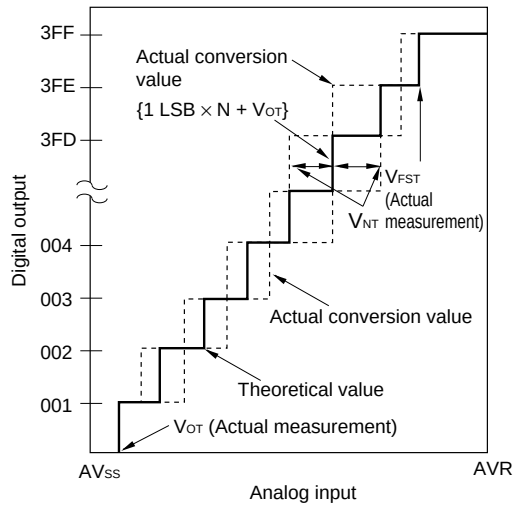
Zero transition error



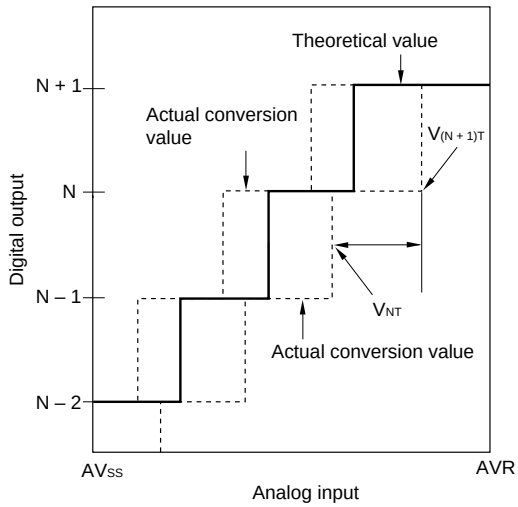
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Digital output N linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Digital output N differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTION

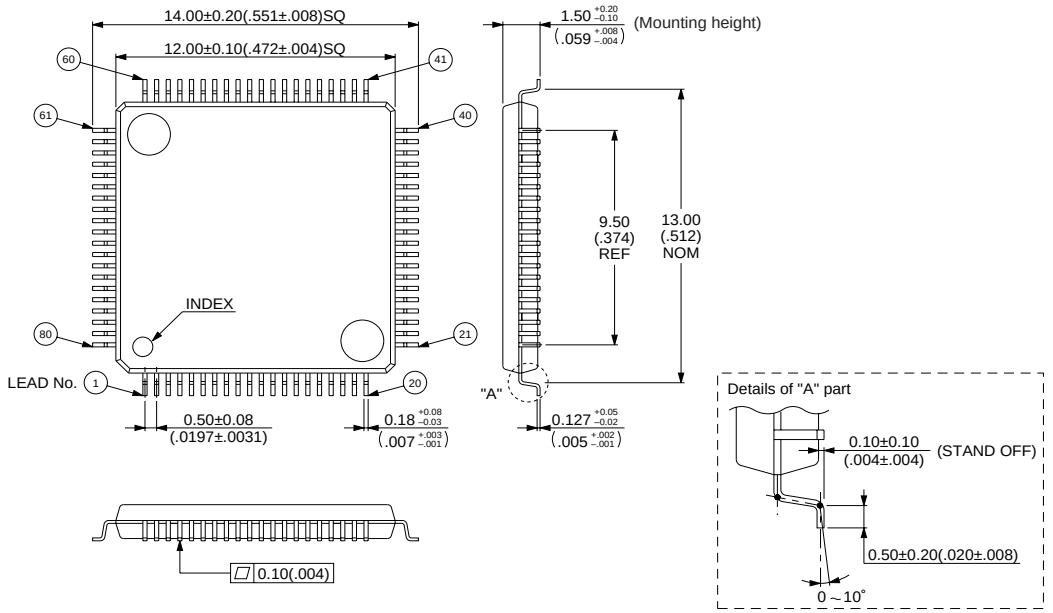
NO.	Model	MB89567H MB89567HC	MB89P568	MB89PV560
	Specification method	Specify when ordering mask.	Setting unavailable.	Setting unavailable.
1	Main clock oscillation stabilization delay time initial value* selection (FCH = 10 MHz) • 01: 2^{12}/FCH (Approx. 0.41 ms) • 10: 2^{16}/FCH (Approx. 6.55 ms) • 11: 2^{18}/FCH (Approx. 26.2 ms)	Selectable	2^{18}/FCH (Approx. 26.2 ms)	$2^{18}/F_{CH}$ (approx. 26.2ms)
2	LCD driving power supply . On-chip voltage booster . Internal voltage divider (external divider resistors can be used)	Internal voltage booster	Selectable by version number	-101 Internal voltage divider -102 On-chip voltage booster

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89567HPFV MB89567HCPFV MB89P568PFV-101	80-pin Plastic LQFP (FPT-80P-M05)	Without Booster Resistor divider
MB89567HPFV MB89567HCPFV MB89P568PFV-102		With Booster
MB89567HPF MB89567HCPF MB89P568PF-101	80-pin Plastic QFP (FPT-80P-M06)	Without Booster Resistor divider
MB89567HPF MB89567HCPF MB89P568PF-102		With Booster
MB89567HPFM MB89567HCPFM MB89P568PFM-101	80-pin Plastic LQFP (FPT-80P-M11)	Without Booster Resistor divider
MB89567HPFM MB89567HCPFM MB89P568PFM-102		With Booster
MB89PV560CF-101	80-pin Ceramic MQFP (MQP-80C-P01)	Without Booster Resistor divider
MB89PV560CF-102		With Booster

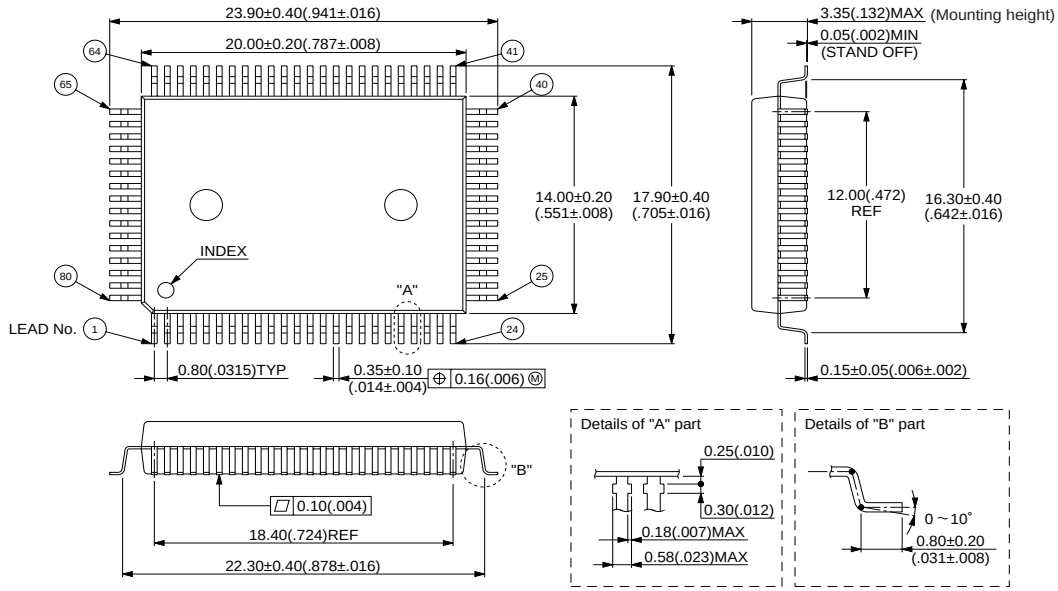
■ PACKAGE DIMENSIONS

80-pin Plastic LQFP
(FPT-80P-M05)



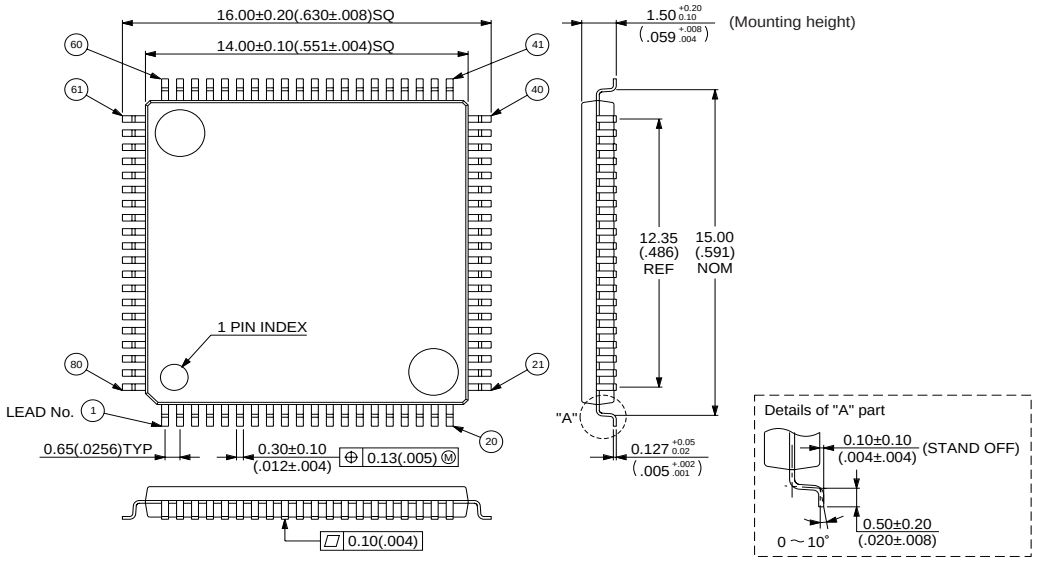
Dimension in mm (inches)

80-pin Plastic QFP
(FPT-80P-M06)



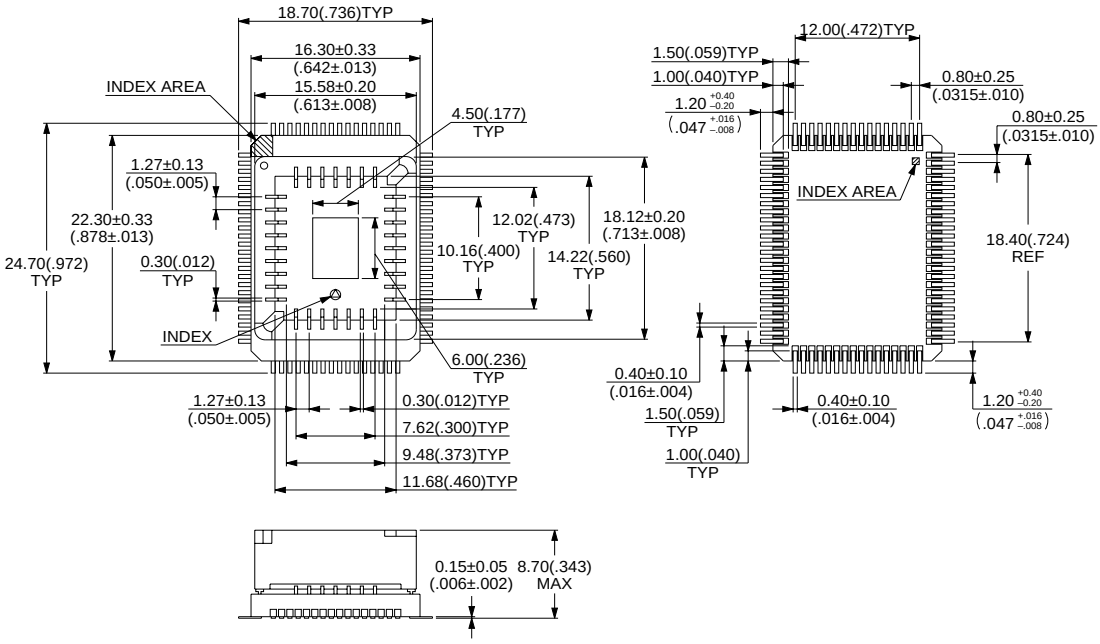
Dimension in mm (inches)

80-pin Plastic LQFP
(FPT-80P-M11)



Deminsion in mm (inches)

80-pin Ceramic MQFP
(MQP-80C-P01)



Dimension in mm (inches)

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