AK8813/14

NTSC/PAL Digital Video Encoder

GENERAL DESCRIPTION

The AK8813/14 is low voltage, low power and small packaged Digital Video Encoder. It is suitable for a STB or Digital TV. It converts ITU-R.BT601/656 standard 8- bit parallel data into analog composite video signal, S-video in NTSC and PAL formats.

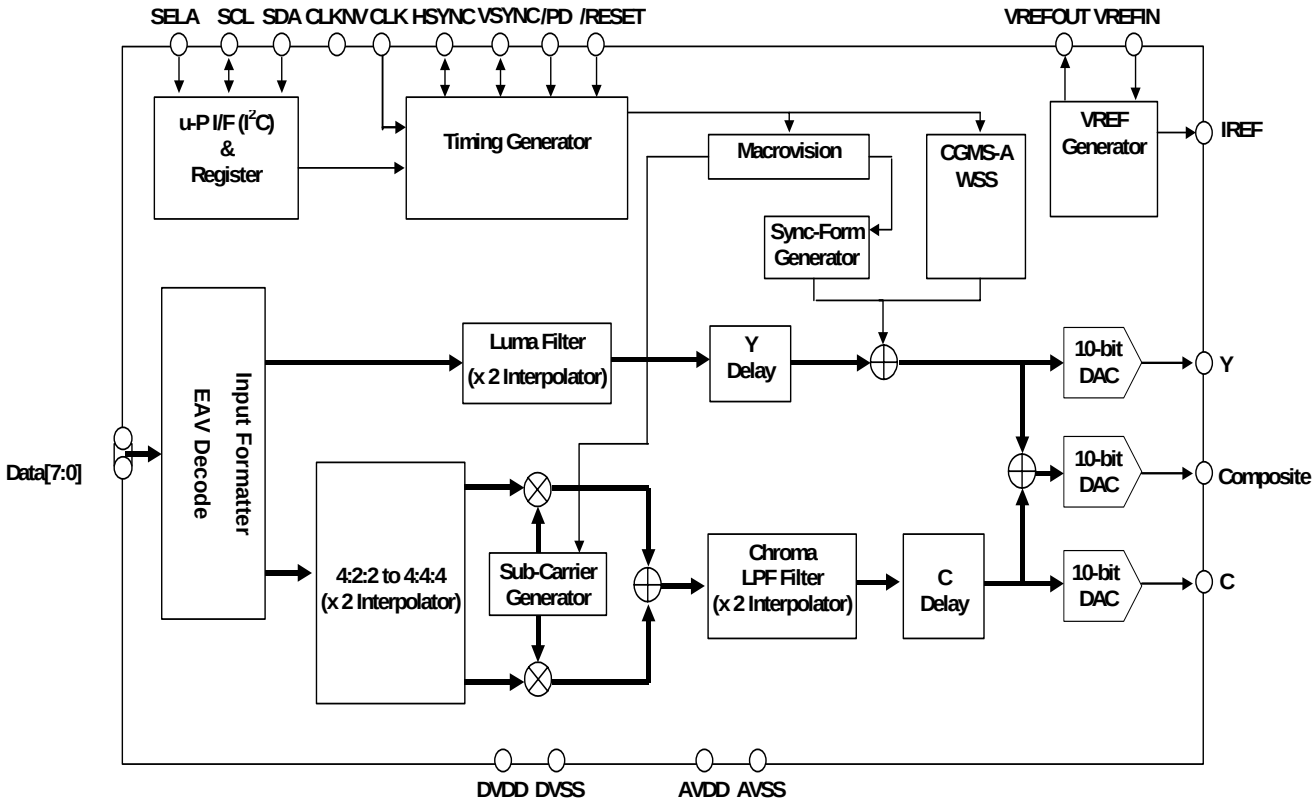
AK8813/14 supports Copy protection, Closed Captioning and Video Blanking ID(CGMS-A) and WSS. These functions are controlled by high-speed I^2C Bus interface.

FEATURES

- NTSC-M, PAL-B,D,G,H,I,M,N encoding.
- Simultaneous composite video signal and S-video signal outputs
- ITU-R BT.656 4:2:2 8-bit Parallel Input
  - EAV Decoding
- Master/Slave Operation
  - Digital Field Sync I/O
  - Digital Vertical/Horizontal Sync I/O
- Y filtering 2 x over-sampling
- C filtering 4 x over-sampling
- Single 27MHz Clock (The polarity could be inverted by SYSINV pin)
- Triple 10-bit DACs
- I^2C Bus Interface (400kHz)
- Closed Caption encoding (NTSC: line 21,284-SMPTE PAL: line 22,335-CCIR)
- Macrovision Copy Protection Rev. 7.1 * (only AK8814)
- VBID, CGMS-A(EIAJ CPR-1024)
- WSS
- On-chip color bar generator
- Low power consumption
- 2.8V to 3.3V operation CMOS Monolithic
- 48pin LQFP Package / 57pin FBGA Package

(*Note) This device is protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098, and other intellectual rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per -view use only, unless otherwise authorized in written by Macrovision. Reverse engineering or disassembly is prohibited.

Block Diagram



ORDERING GUIDE

AK8813VQ: LQFP48 Non-Macrovision (Pb Free)

AK8813VG: FBGA57 Non-Macrovision

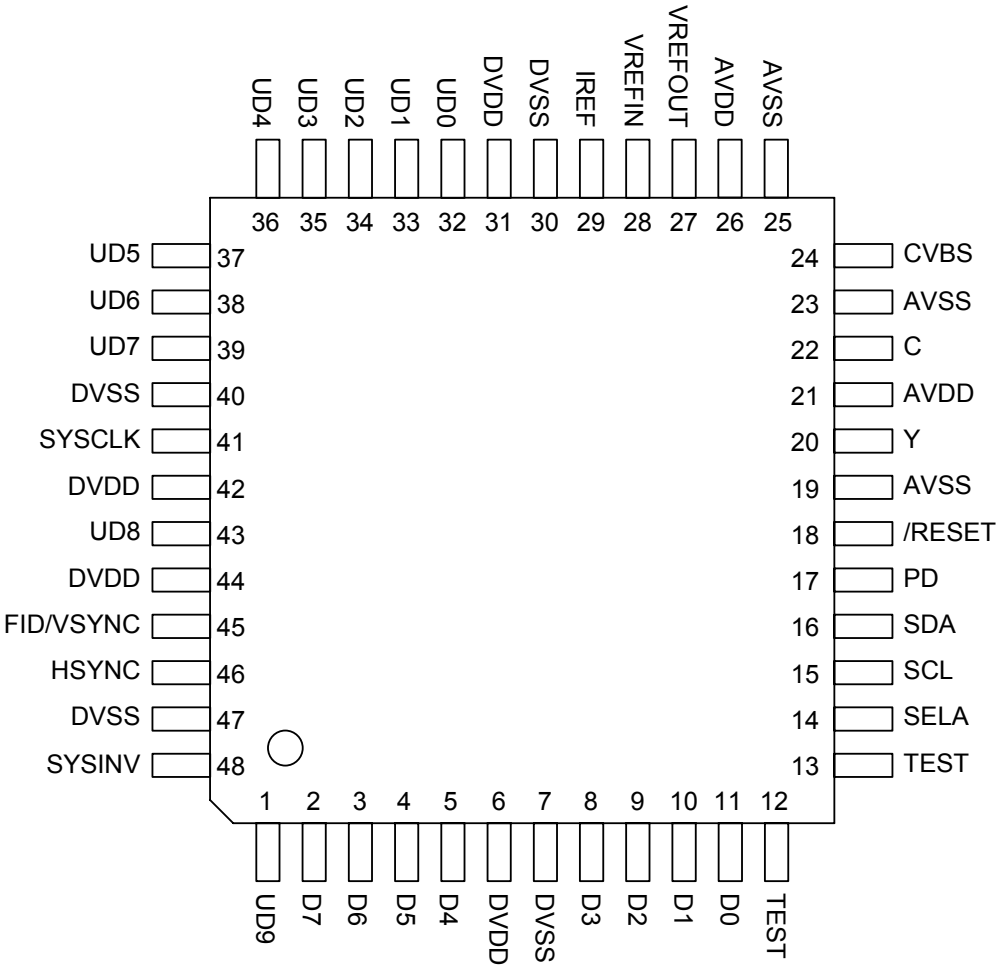
AK8813VGP: FBGA57 Non-Macrovision (Pb Free)

AK8814VQ: LQFP48 Macrovision (Pb Free)

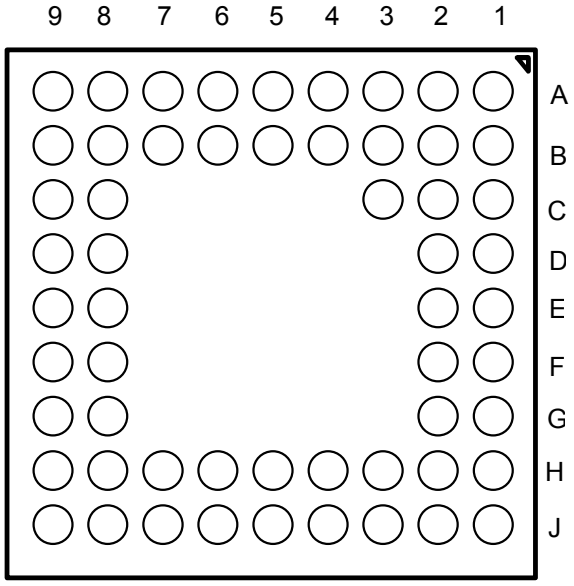
AK8814VG: FBGA57 Macrovision (Pb Free)

PIN LAYOUT

48pin LQFP



57pin FBGA



Bottom View

PIN/FUNCTION

48pin LQFP

No.	Pin Name	I/O	Description
1	UD9	I/O	Test pin. Open for normal operation
2-5, 8-11	D7 - D0	I	27MHz 8-Bit 4:2:2 multiplexed Y,Cb,Cr Data Input. For Rec.656 format, AK8813/14 decodes EAV. For non-Rec.656 format (without EAV), AK8813/14 operates in Master or Slave mode.
12-13	TEST	I	Test pin. Ground for normal operation
14	SELA	I	The slave address is set with this pin. “L”:40H “H”:42H
15	SCL	I	Serial interface clock
16	SDA	I/O	Serial interface data
17	PD	I	Power Down Pin. After returning from PD mode to normal operation, RESET Sequence should be done to AK8813/14.
18	/RESET	I	After this pin becomes “L”, AK8813/14 starts the internal initializing sequence. After initializing sequence, AK8813/14 is set NTSC mode, Rec.656 decoding mode. All DACs Off condition. After power up, AK8813/14 must be initialized with this pin. (27MHz Clock is necessary for reset sequence.)
20	Y	O	Output of Luminance Signal.
22	C	O	Output of the Chrominance signal
24	COMPOSITE	O	Output of Composite Video signal
27	VREFOUT	O	Output of the Internal Vref. Terminate with 0.1uF or more capacitor.
28	VREFIN	I	Input of the Reference Voltage
29	IREF	O	The currents flow this pin adjusts the full-scale output current of the DAC. Connect this pin to Analog ground via a 6.8kohm resistor (better than +/- 1% accuracy).
32-39	UD0-UD7	I/O	Test pin. Open for normal operation
41	SYSCLK	I	27MHz Clock Input. The polarity could be inverted by SYSINV.
43	UD8	I/O	Test pin. Open for normal operation
45	FID /VSYNC	I/O	Either of FID or VSYNC selected by the register. Rec.656 decode mode :Output Master mode : Output Slave mode : Input FID shows that “L” is odd field and ”H” is even field.
46	HSYNC	I/O	Rec.656 decode mode : Output Master mode : Output Slave mode : Input
48	SYSINV	I	“L “ : data is latched with rising edge. “H” : data is latched with falling edge.
21,26	AVDD	P	Analog Power Supply
6,31, 42,44	DVDD	P	Digital Power Supply
19,23,25	AVSS	G	Analog Ground
7,30, 40,47	DVSS	G	Digital Ground

57pin FBGA

No.	Pin Name	I/O	Description
A1	NC	-	Open for normal operation
B1	AVSS	G	Analog Ground
C1	AVDD	P	Analog Power Supply
C2	VREFOUT	O	Output of the Internal Vref. Terminate with 0.1uF or more capacitor.
D1	VREFIN	I	Input of the Reference Voltage
D2	IREF	O	The currents flow this pin adjusts the full-scale output current of the DAC. Connect this pin to Analog ground via a 6.8kohm resistor (better than +/- 1% accuracy).
E1	DVSS	G	Digital Ground
E2	DVDD	P	Digital Power Supply
F2	UD0	I/O	Test pin. Open for normal operation
F1	UD1	I/O	Test pin. Open for normal operation
G2	UD2	I/O	Test pin. Open for normal operation
G1	UD3	I/O	Test pin. Open for normal operation
H1	UD4	I/O	Test pin. Open for normal operation
J1	NC	-	Open for normal operation
J2	UD5	I/O	Test pin. Open for normal operation
H2	UD6	I/O	Test pin. Open for normal operation
H3	UD7	I/O	Test pin. Open for normal operation
J3	DVSS	G	Digital Ground
H4	SYSCLK	I	27MHz Clock Input. The polarity could be inverted by SYSINV.
J4	DVDD	P	Digital Power Supply
H5	UD8	I/O	Test pin. Open for normal operation
J5	DVDD	P	Digital Power Supply
J6	FID/VSYNC	I/O	Either of FID or VSYNC selected by the register. Rec.656 decode mode :Output Master mode : Output Slave mode : Input FID shows that “L” is odd field and ”H” is even field.
H6	HSYNC	I/O	Rec.656 decode mode : Output Master mode : Output Slave mode : Input
H7	DVSS	G	Digital Ground
J7	SYSINV	I	“L “ : data is latched with rising edge. “H” : data is latched with falling edge.
H8	UD9	I/O	Test pin. Open for normal operation
J9	NC	-	Open for normal operation
J8	D7	I	Video data input (MSB)
G8	D6	I	Video data input

H9	D5	I	Video data input
G9	D4	I	Video data input
F8	DVDD	P	Digital Power Supply
F9	DVSS	G	Digital Ground
E8	NC	-	Open for normal operation
E9	D3	I	Video data input
D8	D2	I	Video data input
D9	D1	I	Video data input
C8	D0	I	Video data input
C9	TEST	I	Open for normal operation
B9	TEST	I	Open for normal operation
A9	NC	-	Open for normal operation
A8	SELA	I	The slave address is set with this pin. “L”:40H “H”:42H
B8	SCL	I	Serial interface clock
B7	SDA	I/O	Serial interface data
A7	PD	I	Power Down Pin. After returning from PD mode to normal operation, RESET Sequence should be done to AK8813/14.
A6	/RESET	I	After this pin becomes “L”, AK8813/14 starts the internal initializing sequence. After initializing sequence, AK8813/14 is set NTSC mode, Rec.656 decoding mode. All DACs Off condition. After power up, AK8813/14 must be initialized with this pin. (27MHz Clock is necessary for reset sequence.)
B6	AVSS	G	Analog Ground
A5	NC	-	Open for normal operation
B5	Y	O	Output of Luminance Signal.
B4	AVDD	P	Analog Power Supply
A4	C	O	Output of the Chrominance signal
B3	AVSS	G	Analog Ground
A3	CVBS	O	Output of Composite Video signal
B2	NC	-	Open for normal operation
A2	NC	-	Open for normal operation
C3	NC	-	Open for normal operation

(Note1) At ITU-R.BT656 I/F mode operation, FID/VSYNC, HSYNC pins should be pulled up to VDD with 100k-ohm Resistor

(Note2) This device requires reset operation. Before resetting the state of the pin of I/O are unknown state. After reset sequence, I/Opins (FID/VSYNC, HSYNC) turns Hi-Z states.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (VDD) DVDD, AVDD	-0.3	4.6V	V
Input Pin Voltage (Vin)	-0.3	VDD+0.3	V
Input Pin Current (Iin)	-	±10	mA
Analog Reference Current (IREF)	-	0.37	mA
Analog Output Current	-	11.6	mA
Storage Temperature	-40	125	°C

(Note) When all Ground pins(DVSS, AVSS) are set to 0V.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Supply Voltage (VDD)	2.8	3.3	3.6	V
Operating Temperature	-20		85	°C

DC Characteristics

[Power Supply:2.8 ~ 3.6V Temperature:-20 ~ 85°C]

Parameter	Symbol	Min	Max	Units	Conditions
Digital Input High Voltage	VIH1	0.7VDD		V	Note1)
Digital Input Low Voltage	VIL1		0.3VDD	V	Note1)
Digital Input leak Current	IL		±10	uA	Note1)
Digital Output High Voltage	VOH	2.4/2.2 Note 3)		V	IOH =-1mA Note 2)
Digital Output Low Voltage	VOL1		0.4	V	IOL = 2mA Note 2)
I^2C Input High Voltage I^2C(SDA,SCL)	VIH2	0.7VDD		V	
I^2C Input Low Voltage I^2C(SDA,SCL)	VIL2		0.3VDD	V	
I^2C(SDA) Output Voltage	VOL2		0.4	V	IOL = 3mA

Note 1) D[9:0],FID/VSYNC, HSYNC, SYSCLK, /RESET pin
Note 2) FID/VSYNC, HSYNC pin
Note 3) DVDD=2.8V~3.0V VOH 2.2V
Note) Connected Test Pin to Ground, SELA and SYSINV Pin are desired polarity.

Analog Characteristics

[AVDD:3.3V Temperature:25°C Load Resistance 220ohm IREF Resistance 6.8kohm]

Parameter	Min	Typ	Max	Units	Conditions
DAC Resolution		10		bit	
DAC Integral linearity error		±0.6	± 2	LSB	
DAC Differential linearity error		±0.4	± 1	LSB	
DAC Output Full Scale Voltage	1.21	1.28	1.35	V	Note1)
DAC Output offset Voltage			5.0	mV	Note2)
Unbalances between DACs		±1	±5	%	Note3)
Isolation between DACs		50		dB	1MHz Full Scale
DAC Load Capacitance			30	pF	Note4)
Internal Reference Voltage	1.17	1.235	1.30	V	
Internal Reference Drift		-50		ppm/°C	

Note 1) Under the condition of output load 220Ω, IREF pin with 6.8kΩ, using internal reference. The output full-scale current IOUT is calculated as Full scale output voltage (typ. 1.28V) /220Ω=typ. 5.82mA.

Note 2) DAC output when feeding code of 0 (Decimal).

Note 3) Deviation between the DAC output when feeding 1V generating code of 800(Decimal).

Note 4) The value is a design target. This value is not tested.

Dissipation Current

[AVDD=DVDD=:3.3V Temperature:-25~85°C]

Parameter	Min	Typ	Max	Units	Conditions
DAC Current (Active mode)		24		mA	Note1)
DAC Current (Sleep mode)		10		uA	Note2)
Power Down Current		10	100	uA	Note3)
Total Current		50	65	mA	Note4)

Note 1) All DACs are operating.

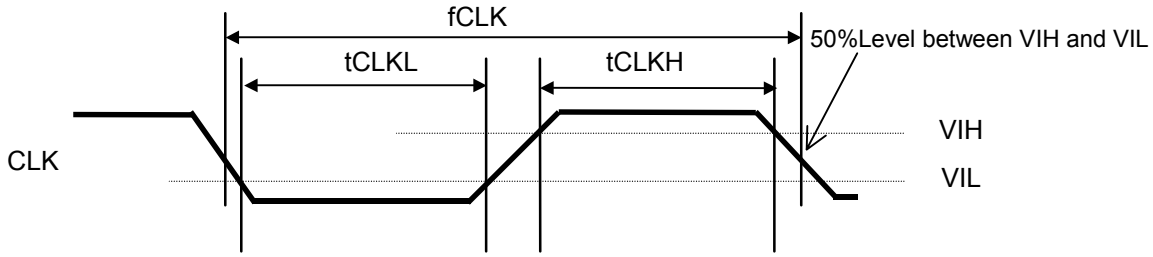
Note 2) All DACs are turned off with no system clock.

Note 3) In case the value after power down sequence.

Note 4) NTSC internal color bar with 3ch DACs operation and slave mode operation. DAC output pins is connected with only 220Ω load.

AC Characteristics (2.8V - 3.6V Temperature –20 ~ 85°C CL=30pF)

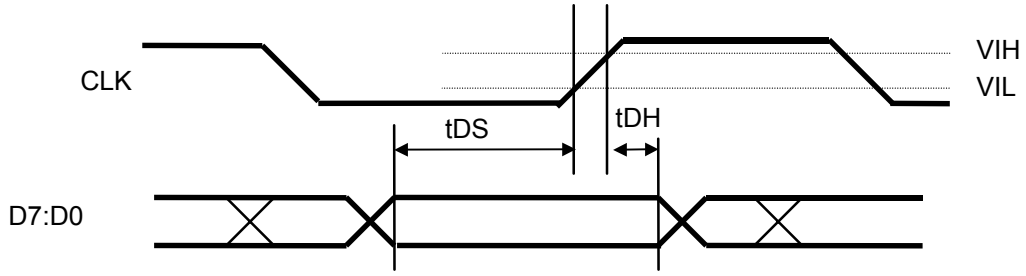
(1). SYSCLK



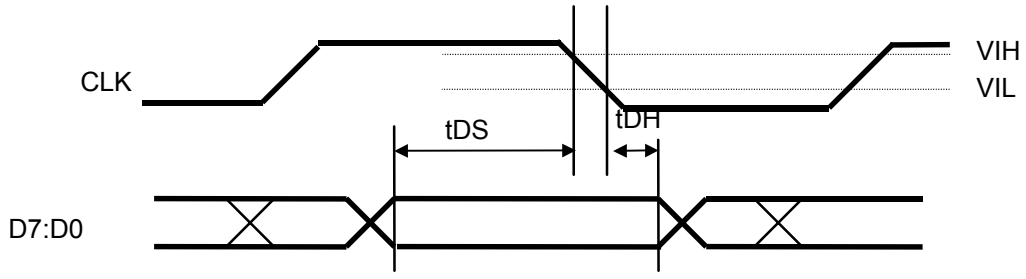
Parameter	Symbol	Min.	Typ.	Max	Unit
SYSCLK	fSYSCLK		27		MHz
SYSCLK Pulse width H	tCLKH	15			nsec
SYSCLK Pulse width L	tCLKL	15			nsec

(2). Pixel Data Input Timing

(2-1) SYSINV = Low



(2-2) SYSINV = High

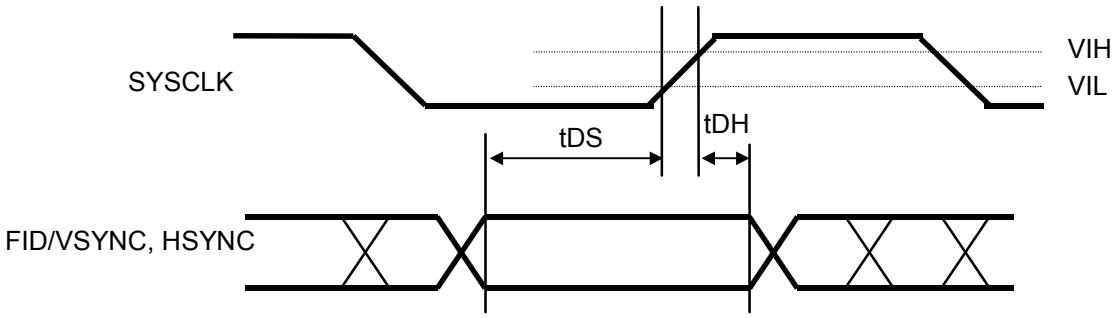


Parameter	Symbol	Min	Typ	Max	Units
Data Setup Time	tDS	5			nsec
Data Hold Time	tDH	8			nsec

(3). Synchronizing Signal (FID/VSYNC, HSYNC)

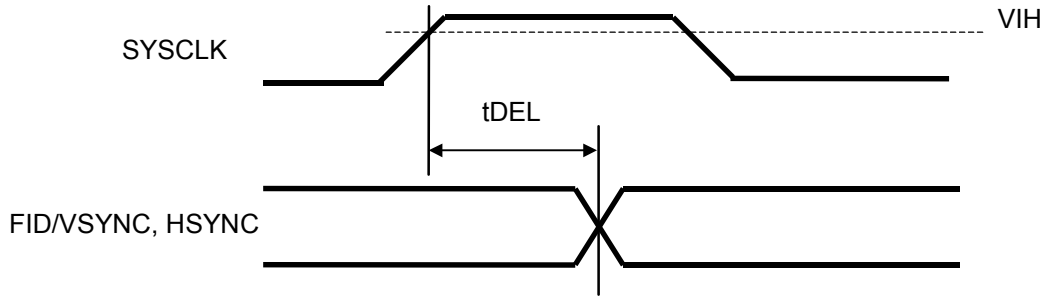
(3-1) SYSINV=Low

(3-1-1) Input Timing



Parameter	Symbol	Min	Typ.	Max	Units
Data Setup Time	tDS	5			nsec
Data Hold Time	tDH	8			nsec

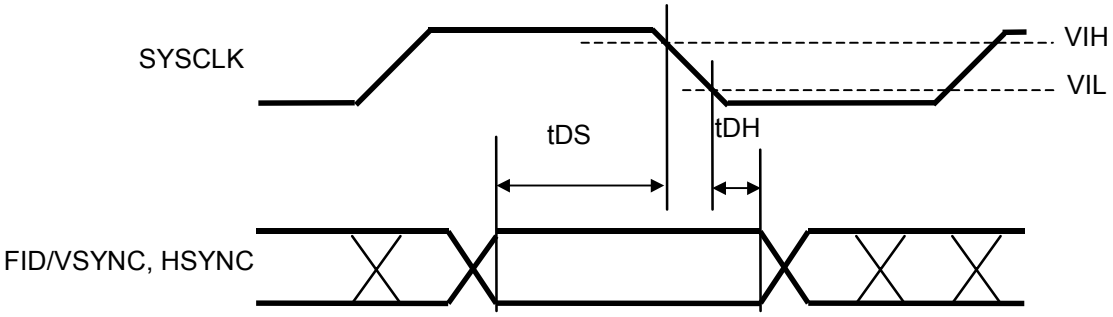
(3-1-2) Output Timing



Parameter	Symbol	Min	Typ.	Max	Units
Delay from SYSCLK	tDEL			27	nsec

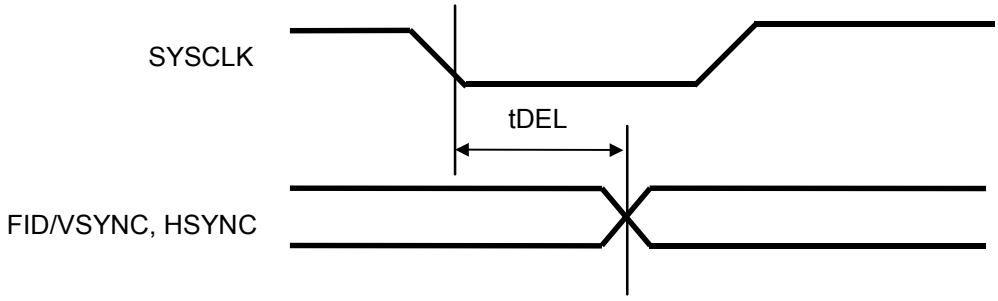
(3-2) SYSINV = High

(3-2-1) Input Timing



Parameter	Symbol	Min	Typ.	Max	Units
Data Setup Time	tDS	5			nsec
Data Hold Time	tDH	8			nsec

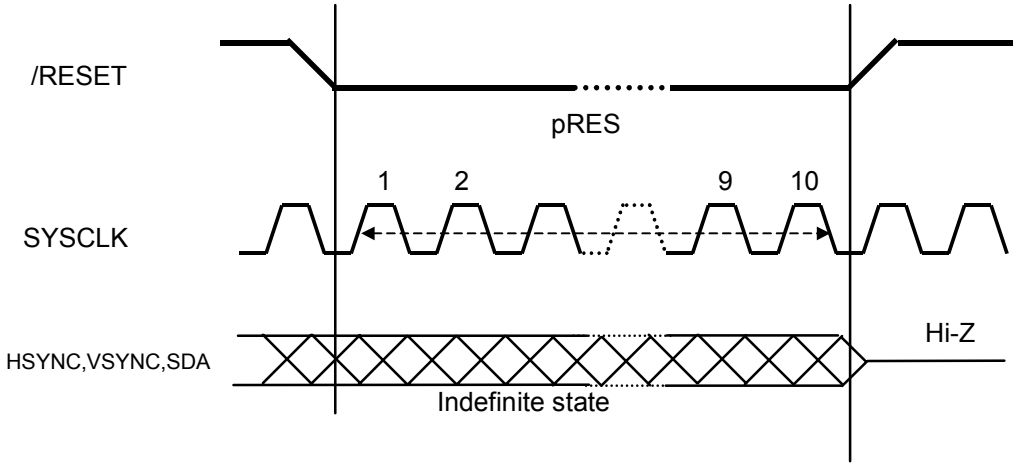
(3-2-2) Output Timing



Parameter	Symbol	Min	Typ.	Max	Units
Delay from SYSCLK	tDEL			27	nsec

(4). Reset (Initialize)

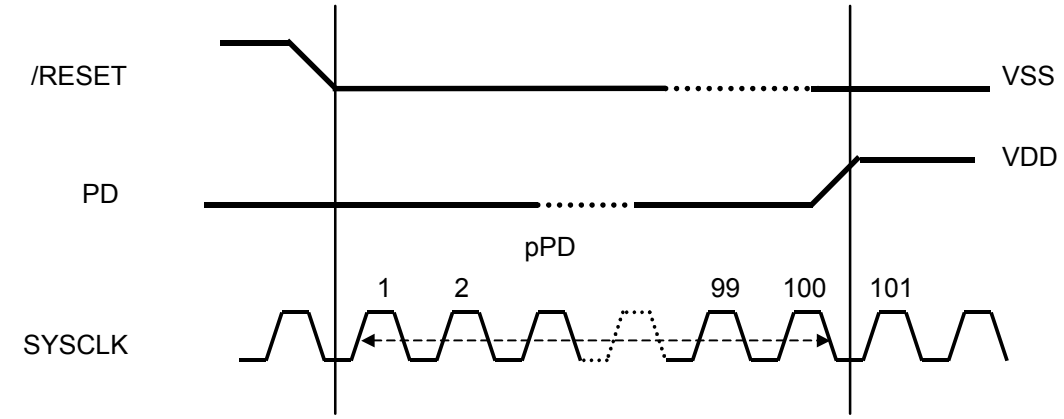
Reset Timing



Parameter	Symbol	Min	Typ.	Max	Units
/RESET Pulse Width	pRES	10			SYSCLK

After power up, I/O pins of AK8813/14 are in the indefinite state. It should be initialize with Reset sequence. While reset sequence system clock should be input to AK8813/14 and SCL, SDA should be High state.

(5) Power Down Sequence

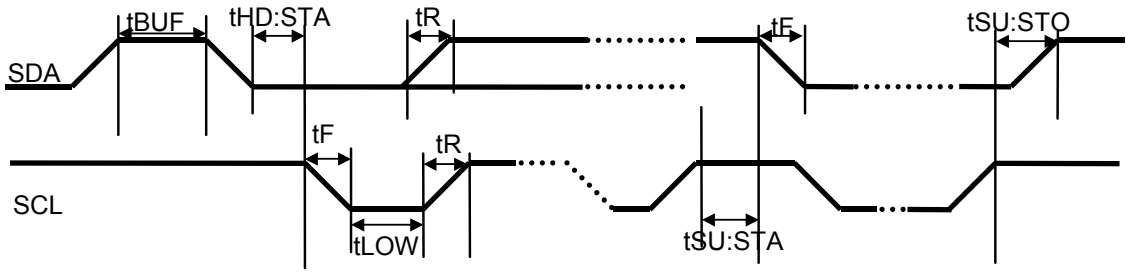


Parameter	Symbol	Min	Typ.	Max	Units
/RESET Pulse Width	pSTOP	100			SYSCLK

During “Power Down” state, control signal should be set to VDD state or VSS state.

(5). I^2C Bus (SCL 400kHz cycle mode)

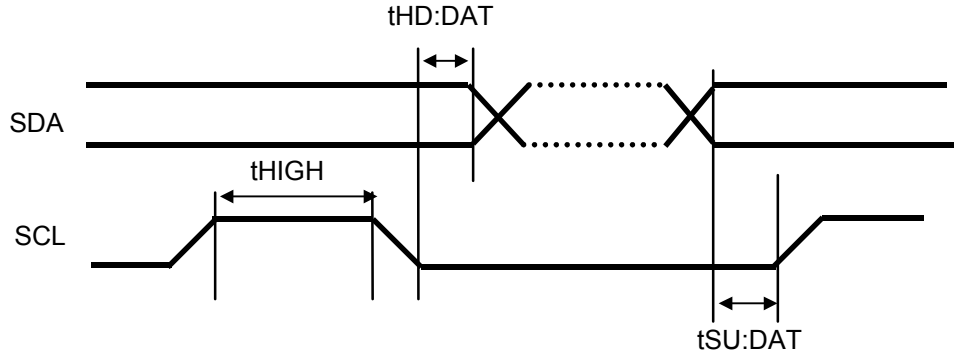
(5-1) I/O Timing 1



Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Bus Signal Rise Time	tR		300	nsec
Bus Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

All the figures shown above list are not restricted by AK8813/14 but are restricted by I^2C Bus standard. Please see the I^2C Bus standard for further details.

(5-2) I/O Timing 2



Parameter	Symbol	Min.	Max.	Unit.
Data Setup Time	tSU:DAT	100 (1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(Note1) In case of normal I^2C bus mode tSU:DAT $\geq$250nsec
(Note2) Using under minimum tLOW, this value must be satisfied.
(Note3) I2C I/F reset is done by reset sequence of AK8813/14, System clock (27MHz) is necessary to do reset sequence. However, SDA pin is always Hi-Z state when PD pin is set to High.

FUNCTIONAL DESCRIPTION

♦ Reset

When the reset pin [/RESET] set to “L”, AK8813/14 is in reset state. AK8813/14 starts in the internal initializing sequence at the trailing edge of the first SYSCLK after the reset pin is “L”. All internal registers are set to be default value by this initializing sequence. AK8813/14 needs at least 10 clock counts of SYSCLK for this reset operation. After the reset operation, the video output pins are in high-impedance. AK8813/14 requires SYSCLK for the reset operation.

♦ Master Clock

AK8813/14 requires 27MHz clock at SYSCLK pin for operation. Video input data (ITU-R BT.656) is sampled at the trailing edge of this 27MHz. SYSINV decides the edge direction.

SYSINV = L Data is sampled at rising edge of SYSCLK.
SYSINV = H Data is sampled at falling edge of SYSCLK.

♦ Video Signal Interface

AK8813/14 can interface with the video input data by the following 3 modes. The mode is set by the register [Interface mode register(00H)].

1. ITU-R BT.656 Format

AK8813/14 decodes EAV in stream data and manages an internal synchronization.
In this case, AK8813/14 outputs FID (odd : “L” even : “H”)/ VSYNC and HSYNC.
CCIR-bit of [Interface mode register (00H)] should be set “1” .

2. ITU-R BT.656 like Format (4:2:2 Y/Cb/Cr)

There are Master and Slave modes, for ITU-R BT.656 like Format which does not include EAV. In this mode, CCIR-bit of [Interface mode register(00H)] should be set “0” .

<Master Mode>

AK8813/14 provides FID/VSYNC and HSYNC to an external device according to the AK8813/14 internal timing counter. AK8813/14 starts to sample the input data at the fixed value on the internal pixel counter.
In this mode, following setting should be done to [Interface mode register(00H)].
CCIR-bit = 0
MAS-bit = 1

<Slave Mode>

FID/VSYNC and HSYNC are supplied by an external device. AK8813/14 samples the data as same manner of Master mode.
In this mode, following setting should be done to [Interface mode register(00H)].
CCIR-bit = 0
MAS-bit = 0

♦ Video Signal Conversion

Video reconstruction module converts the multiplexed data (ITU-R. BT601 Y/Cb/Cr) to the interlace format of NTSC-M, PAL-M, PAL-B,D,G,H,I,N and other formats (ex. NTSC-4.43 and PAL60). The video reconstruction format, the line number, the color encode way(NTSC or PAL) and the frequency of Color Sub-carrier is specified by [Video Process 1 register(01H)]. (cf. Burst Signal Table) The frequency and the phase of Color Sub-carrier are also adjustable by [Sub C. Freq. register(06H)] and [Sub C. Phase register(07H)]. The Sub-carrier has a free-running mode and a reset-mode. In the reset-mode, the Sub-carrier is reset automatically to the initial phase for every 4 fields (NTSC) or 8 fields (PAL).

♦ Luminance Filter

Luminance signal passes through the 2x Low Pass filter with sin(x)/x compensation. Fig.1 is the characteristic of Luminance Filter.

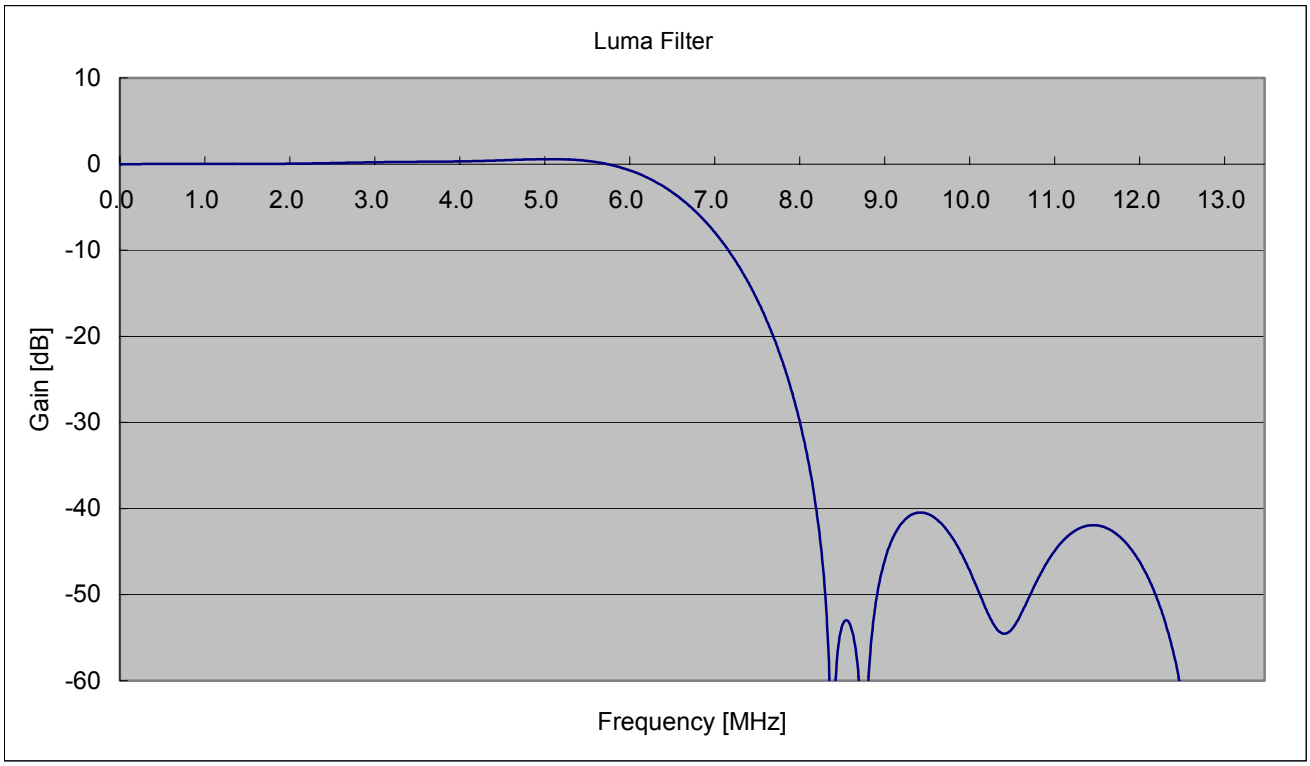


Fig. 1 Luminance Filter

♦ Chrominance Filter

Chrominance signals (Cb,Cr) before Sub-carrier modulation pass through the 1.3 MHz Low pass filter shown in Fig.2. Chrominance signal modulated by Sub-carrier passes through the filter shown in Fig.3.

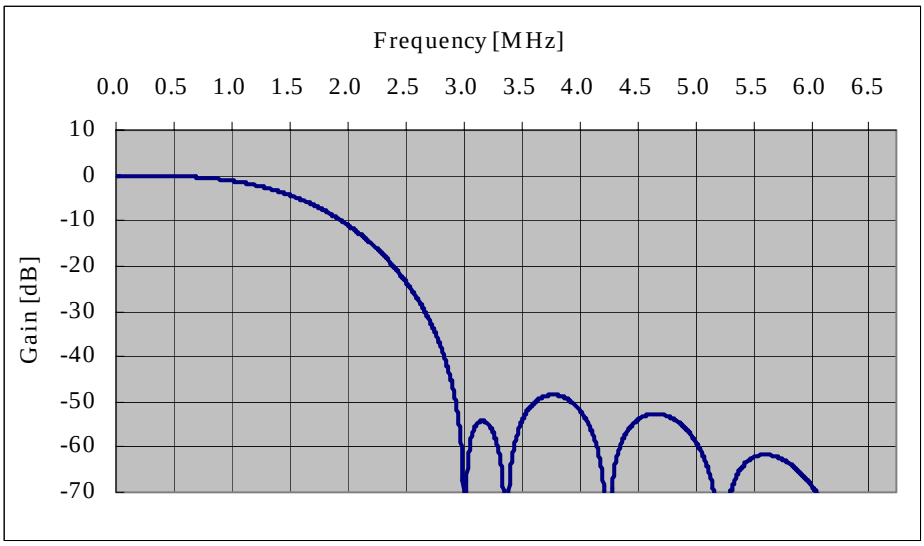


Fig. 2 Chroma-1 LPF

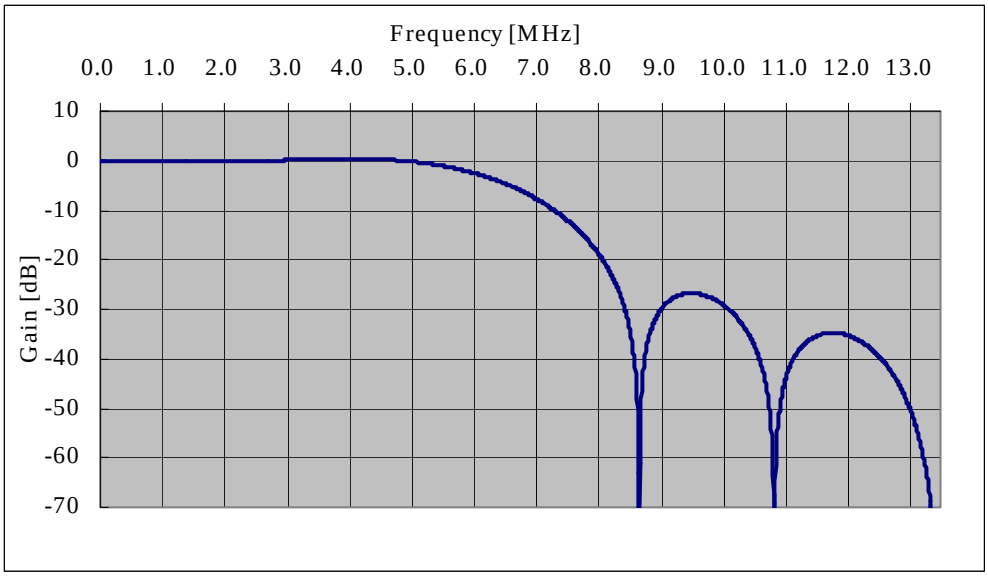


Fig. 3 Chroma-2 LPF

♦ Color burst signal

Color burst signal is generated by 32bits-length Digital Frequency Synthesizer. The Default frequency of the color burst is selected by [Video Process 1 Register(0x01)].

Standard	Sub-carrier Freq. [MHz]	Video Process 1 [VM1,VM0]
NTSC-M	3.57954545	[0,0]
PAL-M	3.57561188	[0,1]
PAL-B,D,G,H,I	4.43361875	[1,1]
PAL-N(Arg.)	3.5820558	[1,0]
PAL-N(non-Arg.)	4.43361875	[1,1]
PAL60	4.43361875	[1,1]
NTSC-4.43	4.43361875	[1,1]

Burst Signal Table

Sub-carrier frequency 3.57561188MHz is allowed when PAL-M mode is selected.

The burst frequency and initial phase resolution are as follows.

Frequency resolution	0.8046Hz
SCH Phase resolution	360°/256

♦ Video DAC

AK8813/14 has the three current driven 10bits-DACs at 27MHz operation. The full scale voltage of DAC is determined by the current output from IREF pin. Typical output voltage is 1.28Vo-p under the condition of VREFIN 1.235V, 6.8KΩ between IREF pin and Ground(AVSS) and DAC load resistance of 220Ω. This full-scale voltage should be set in the range of 1.17V to 1.33V by adjusting the resistor which terminates IREF pin. Each DAC output can be set to “active state” or to “inactive state” individually by [DAC Mode register(05H)]. When DAC is in “inactive state”, the output is Hi-impedance. When all DACs are set to “inactive state”, the analog part of AK8813/14 goes into sleep mode. In this case AK8813/14 stops outputting the reference voltage(VREF) output. When any DAC is switched over in “active state” from sleep mode, AK8813/14 starts outputting reference voltage. In this case AK8813/14 needs several milliseconds for VREF wake-up time.

Using internal VREF as the reference voltage, connect [VREF OUT] pin with [VREF IN] pin and [VREF OUT] pin is terminated with more than 0.1uF capacitor.

♦ Use external Reference Voltage

In order to improve the accuracy of DAC output, external reference voltage may be used. In this case, VREFOUT pin still needs to be terminated with more than 0.1uF capacitor.

♦ Copy Protection

AK8814 has the function of Macrovision copy protection. Information about the Macrovision encoding functions of the AK8814 is available to Macrovision licensees.

AK8813 doesn't have this function.

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♦ Closed Caption and Extended Data

AK8813/14 supports both Closed Captioning and Extended Data. They are controlled “ON” or ”OFF” respectively by [Video Process 2 Register(02H)]. Each data consists of 2 continuous bytes register(Closed Caption R (16H,17H)), and it is recognized as the data is renewed when the second byte(17H register) is written in the register. After the data is renewed, AK8813/14 encodes Closed Captioning and Extended Data at the designated line. If the data isn’t renewed, AK8813/14 outputs “ASCII-NULL” code. The data is supposed as Odd Parity and 7 bit US-ASCII code. Host should provide a parity bit.

*In PAL encoding mode, AK8813/14 outputs them at the same timing and same pattern as NTSC.

*The line where Closed Captioning data is encoded is as follows.

	525/60 System (SMPTE)	625/50 System (CCIR)
Closed Caption	21 Line default	22 Line default
Extended Data	284 Line default	335 Line default

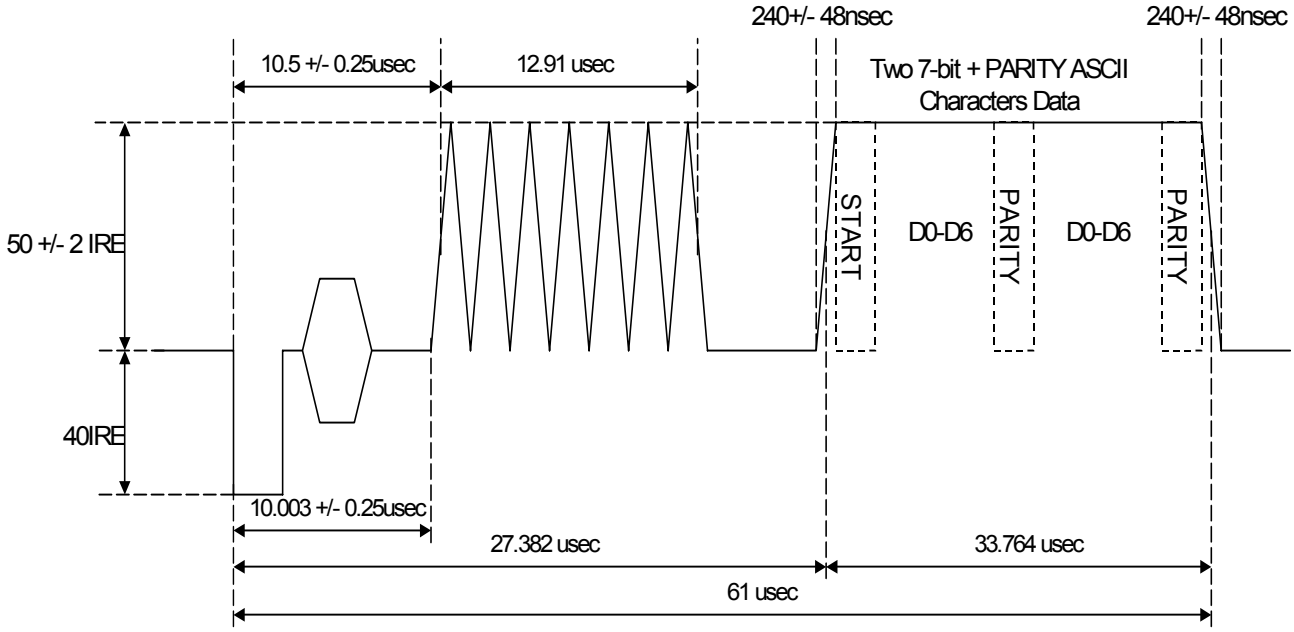


Fig. 4 Closed Captioning Wave form

♦ Video ID

AK8813/14 supports Video ID (EIAJ standard, CPR-1204) encoding for the distinction of an aspect ratio or CGMS-A etc. Setting or Resetting the VBID-bit of [Video Process 2 Register(02H)], this function is switched On/Off. The data is set by using [Video ID Data Register(1AH, 1BH)].

VBID Data Renewal Timing.

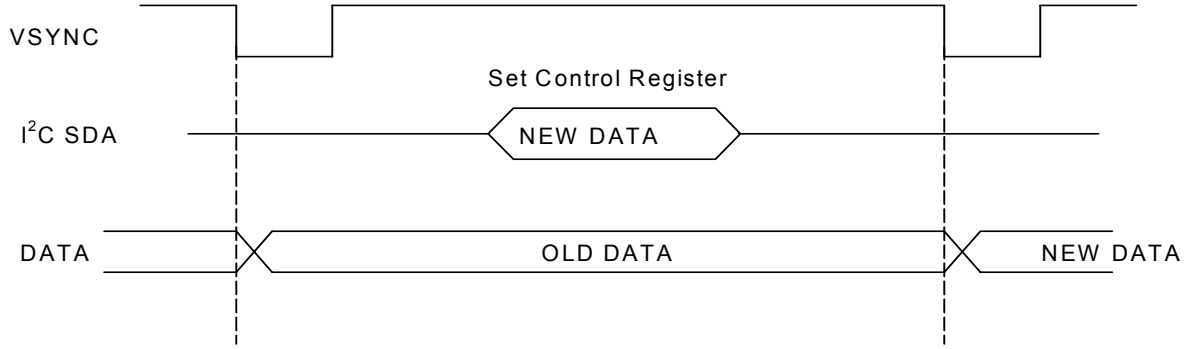


Fig. 5 VBID Data renewal Timing

VBID Data Layout

VBID is consists of 20 bits and its format is shown as follows.

AK8813/14 generates CRC code automatically and appends it to the data. Initial value of the Polynomial is 1.

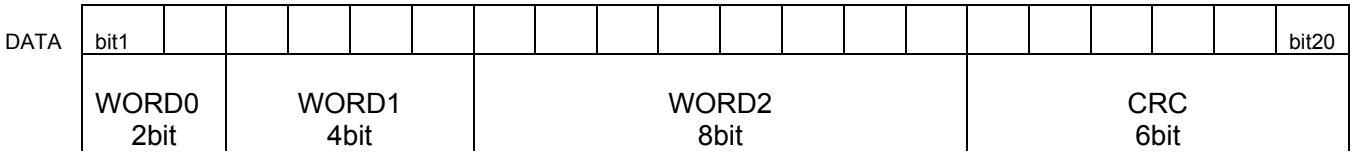


Fig. 6 VBID code assignment

VBID Waveform

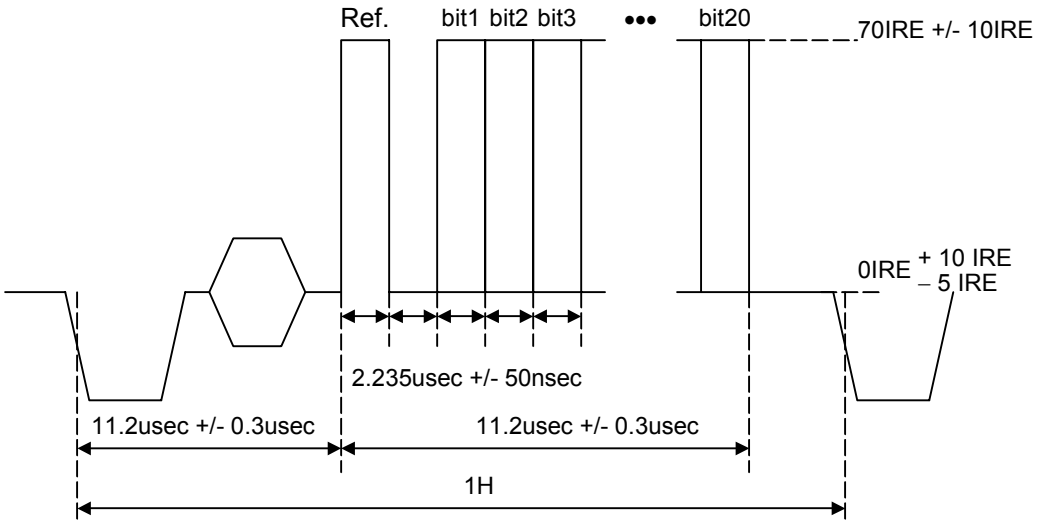


Fig. 7 VBID Wave Form

	525/60 system	625/50 system
Amplitude	70 IRE	490 mV
Encode Line	20/283	20/333

VBID parameter table

♦ WSS

AK8813/14 supports WSS(ITU-R.Bt.1119) encoding for the distinction of an aspect ratio etc. Setting or Resetting the WSS-bit of [Video Process 2 Register(02H)], this function is switched On/Off. The data is set by using [WSS Data Register(08H, 09H)].

WSS Data Renewal Timing

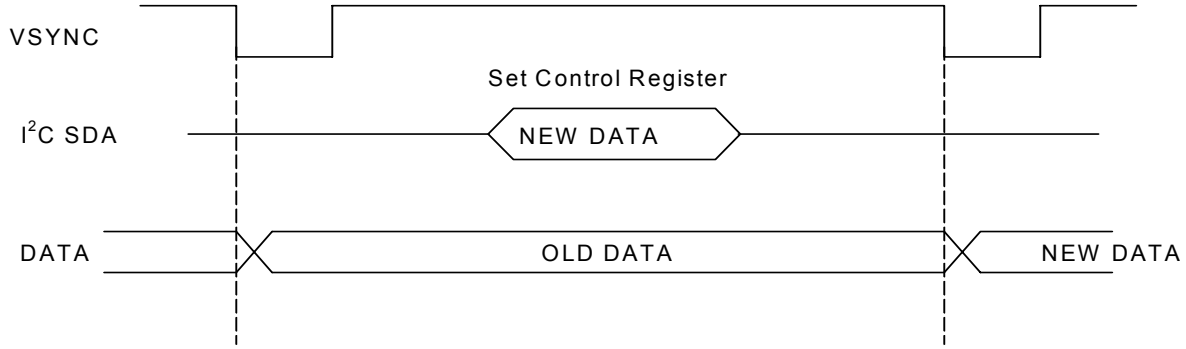


Fig. 8 WSS Data Renewal Timing

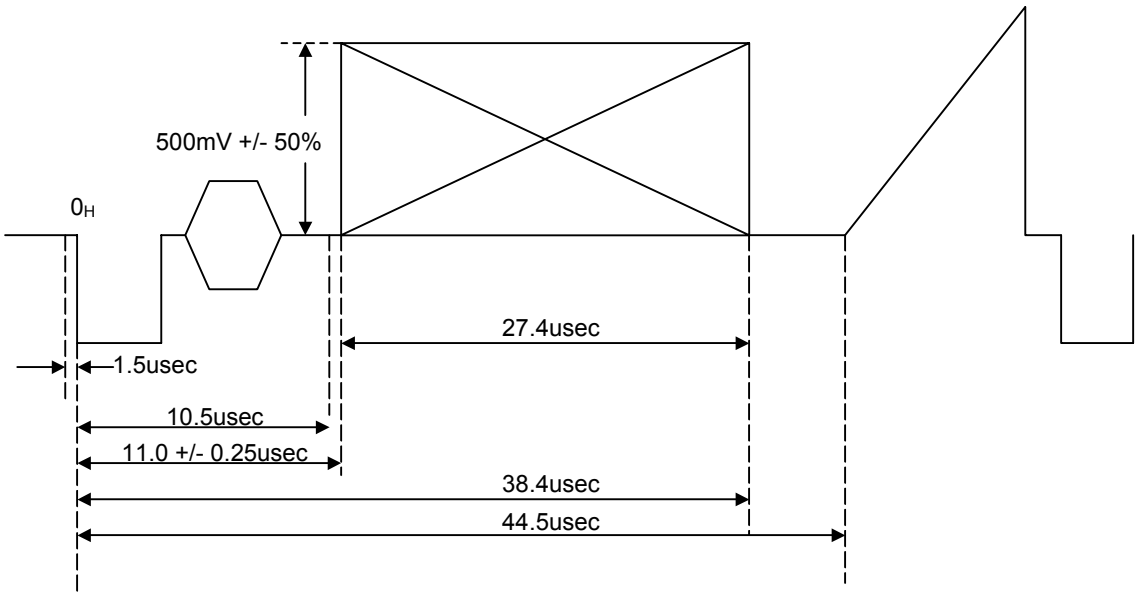


Fig. 9 WSS Wave Form

Encode Line: Line 23
Coding: bi-phase modulation coding
Clock: 5MHz (Ts = 200ns)

Run-in	Start code	Group 1 Aspect ratio	Group 2 Enhanced Services	Group 3 Subtitles	Group4 Reserved
29 elements	24 elements	24 elements	24 elements	18 elements	18 elements
		Bit numbering 0 1 2 3 LSB MSB 0 : 000111 1 : 111000	Bit numbering 4 5 6 7 LSB MSB 0 : 000111 1 : 111000	Bit numbering 8 9 10 LSB MSB 0 : 000111 1 : 111000	Bit numbering 11 12 13 LSB MSB 0 : 000111 1 : 111000
0x1F1C71C7	0x1E3C1F				

♦ AK8813/14 Interface Timing (Part 1) Master mode & ITU-R BT. 656 mode

On ITU-R BT.656 decoding mode or master mode operation, AK8813/14 outputs HSYNC and FID or VSYNC (selected by register).

When AK8813/14 receives ITU-R BT. 656 signal, AK8813/14 decodes [EAV] code in the data for synchronization then outputs the HSYNC. AK8813 outputs HSYNC at the rising edge of SYSCLK in the timing of the 32nd/24th(NTSC/PAL) data slot, which is counted from the [EAV] starting point as below. (See also AC Characteristics 2-2[Input Synchronizing Signal])

On master mode operation, the front device connected with AK8813/14 (ex. MPEG Decoder) starts to set Cb on the 276th/288th(NTSC/PAL) slot, after starting to count HSYNC falling edge as 32nd/24th(NTSC/PAL) slot.

FID/VSYNC is output synchronously with HSYNC at the timing of solid line as in Fig. 10 Video Field.

	EAV															SAV									
Y/Cb/Cr	Cb	Y	Cr	Y	Cb	Y	Cr	Y			Cb	Y	Cr			Y	Cb	Y	Cr	Y	Cb	Y	Cr	Y	Cb
Data# 525 system	360	720	360	721	361	722	361	723			368	736	368			855	428	856	428	857	0	0	0	1	1
Data# 625 system	360	720	360	721	361	722	361	723			366	732	366			861	431	862	431	863	0	0	0	1	1

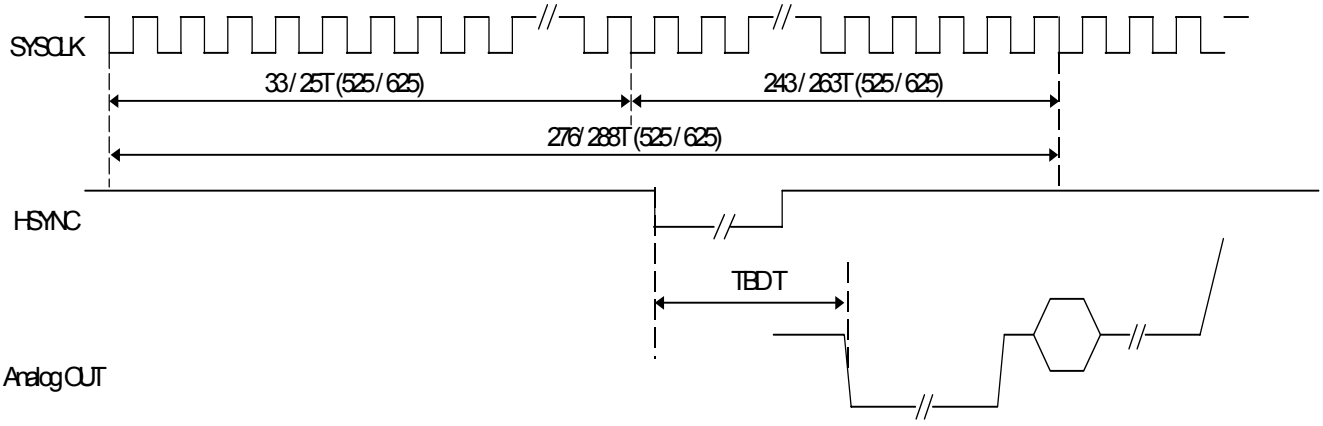


Fig. 10 Interface Timing (ITU-R BT.656 or Master mode)

♦ AK8813/14 Interface Timing (Part 2) Slave mode

On slave mode operation, HSYNC and FID or VSYNC (Selected by register) are input to AK8813/14.

AK8813/14 monitors the transition of HSYNC at the timing of the rising edge of SYSCLK. (Refer to AC Characteristic 2-1. [Input Synchronizing Signal]) After AK8813/14 recognizes HSYNC is Low-logic, AK8813/14 sets the slot number to the 32nd/24th(NTSC/PAL), internally, then AK8813/14 starts to sample the data as Cb on 276th/288th(NTSC/PAL) slot.

Video field is recognized the transition timing between FID/VSYNC and HSYNC. (Fig.10. Video Field) As in the figure, there is a tolerance of ±1/4H.

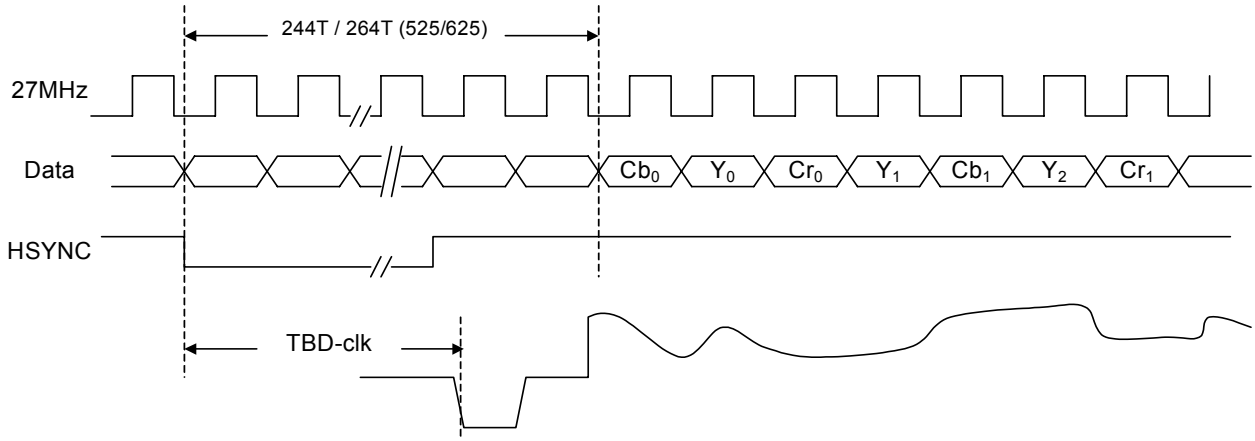


Fig. 11 Interfacing timing (Slave mode)

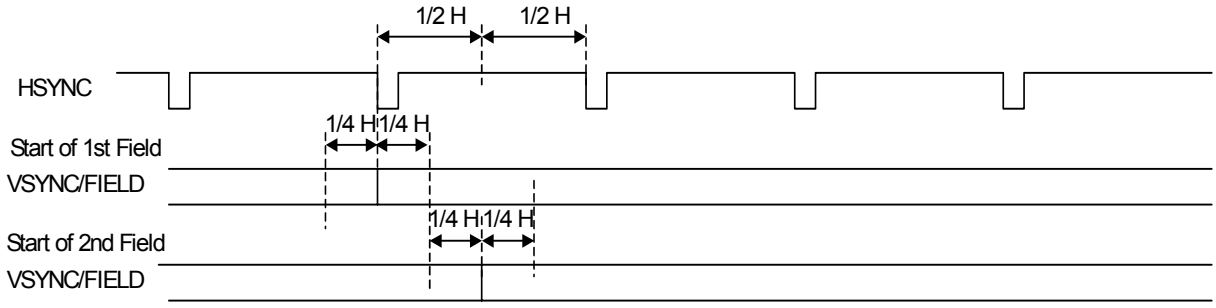
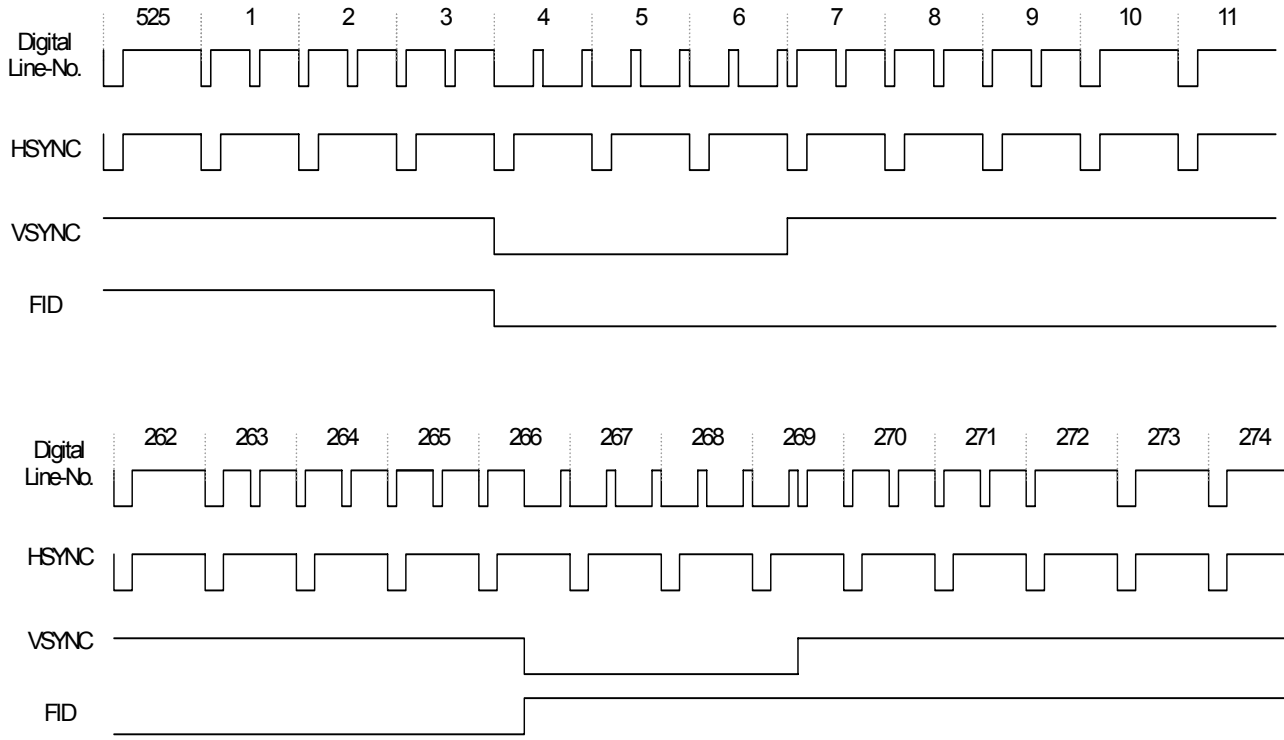


Fig. 12 Video Field

♦ HSYNC FID/VSYNC Timing

525 System



625 System

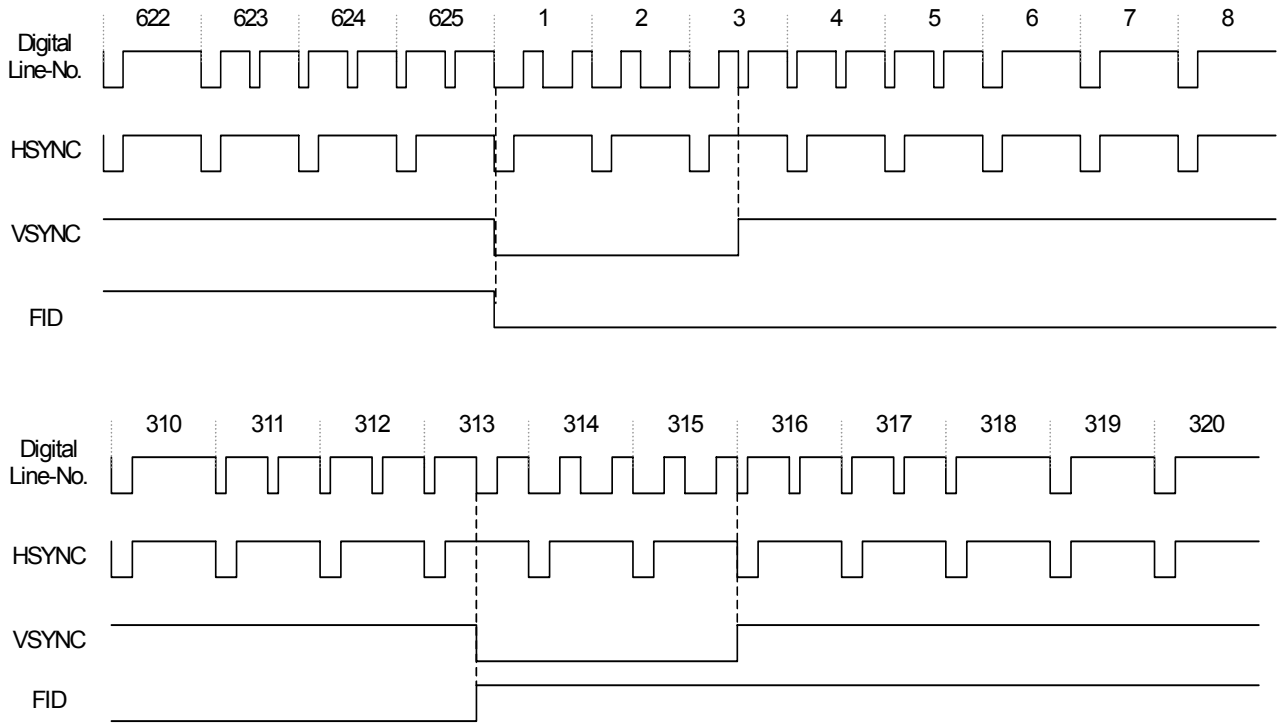


Fig. 13 HSYNC FID/VSYNC Timing

♦ Internal Color Bars Generator

AK8813/14 generates the Common Color Bar signal for NTSC and PAL internally. The generated Color Bar is “100% Amplitude, 100% Saturation”. When AK8813/14 is set to Black Burst output mode, AK8813/14 does not output Color bar even Color bar output register is set.

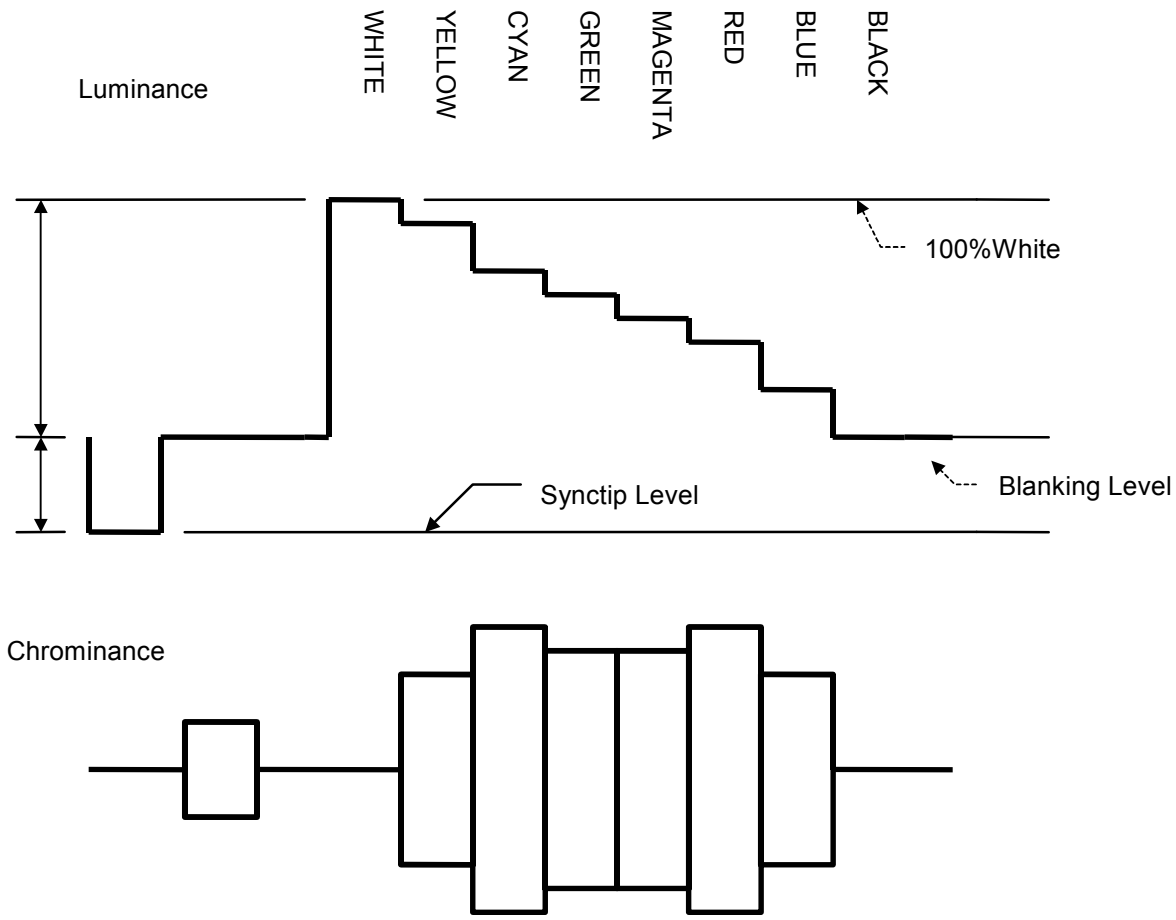


Fig. 14 Luminance and Chrominance waveform

The following values are code for ITU-R. BT601

	WHITE	YELLOW	CYAN	GREEN	MAGENTA	RED	BLUE	BLACK
Cb	128	16	166	54	202	90	240	128
Y	235	210	170	145	106	81	41	16
Cr	128	146	16	34	222	240	110	128

♦ Internal Black Burst Generator

AK8813/14 generates Black burst signal for NTSC and PAL internally. When AK8813/14 is set to Black burst output mode, AK8813/14 works same operation as that the input Y/Cb/Cr data is 16/128/128. In this mode, AK8813/14 does not output Color bar even Color bar output register is set.

♦ Synchronizing Signal and Burst Waveform

(1-1) NTSC / NTSC-4.43 / PAL-M(Video Process 1 Register [VM3:VM2]-bit = 00 / 01) (SMPTE-170M)

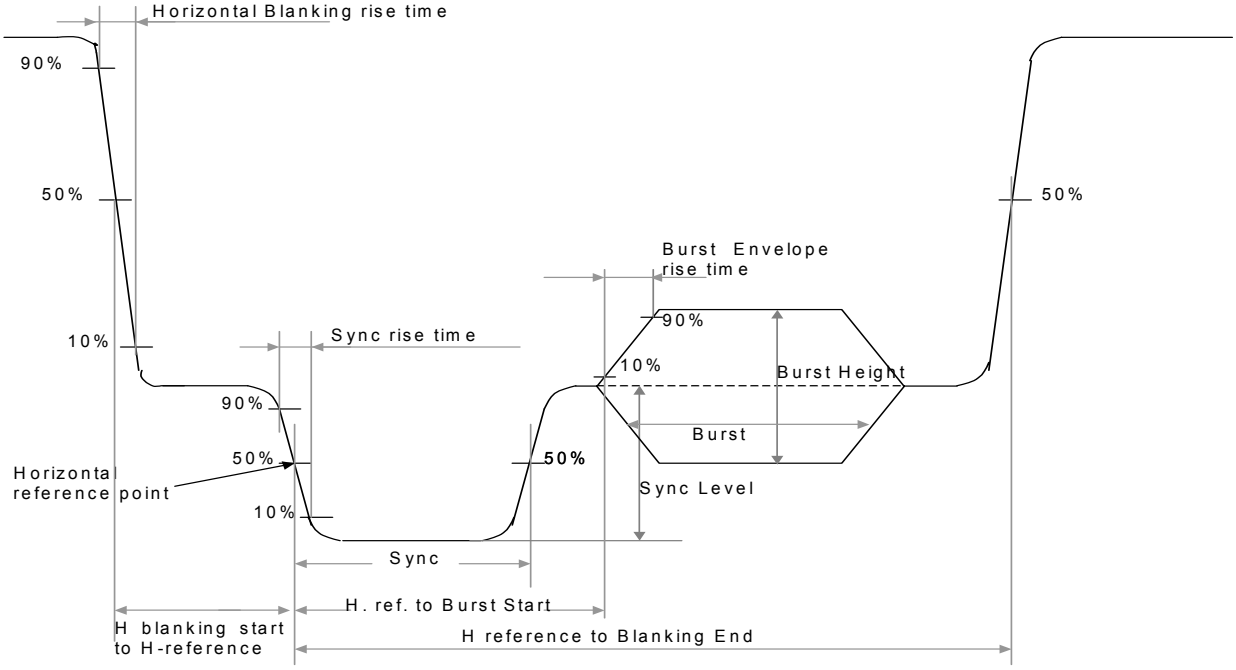


Fig. 15 Synchronizing Signal and Burst Waveform

	measurement point	value	Recommended tolerance	units
Total line period(derived)		63.556		usec
Sync Level		40	+/- 1	IRE
Horizontal Blanking rise time	10% - 90%	140	+/- 20	nsec
Sync rise time	10% - 90%	140	+/- 20	nsec
Burst envelope rise time	10% - 90%	300	+200 -100	nsec
H-Blanking start to H-reference	50%	1.5	+/- 0.1	usec
Horizontal Sync	50%	4.7	+/- 0.1	usec
Horizontal reference point to burst start	50%	19	defined by SC/H	cycles
H reference to H-blanking end	50%	9.2	+ 0.2 –0.1	usec
Burst	50%	9	+/- 1	cycles
Burst Height *		40	+/- 1	IRE

* Burst height of PAL-M is 306mV

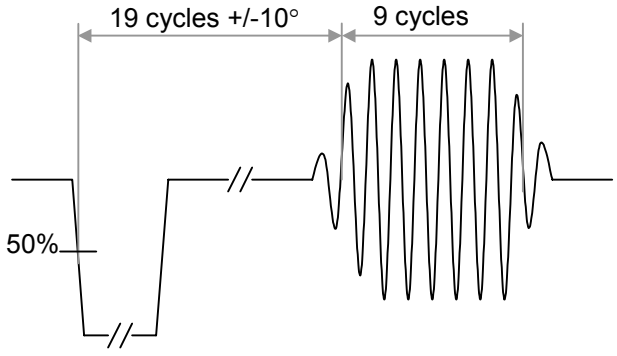


Fig. 16 Synchoronizing Signal and Burst Waveform(NTSC)

(1-2-1) HSYNC Timing (NTSC/NTSC4.43)

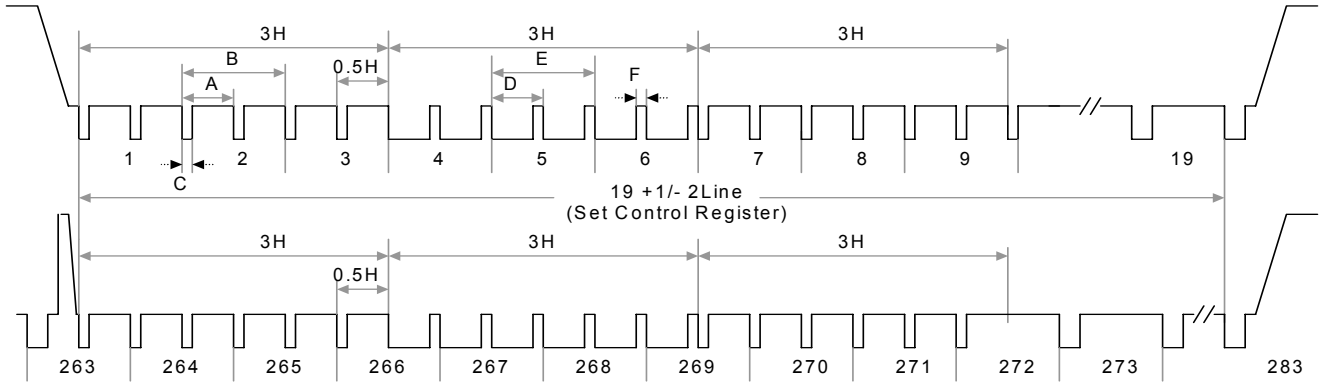


Fig. 17 HSYNC Timing

Symbol	Duration	Measurement point	Reference
A	429T	50%	13.5MHz Clock
B	858T		
C	31T		
D	429T		
E	858T		
F	63T		

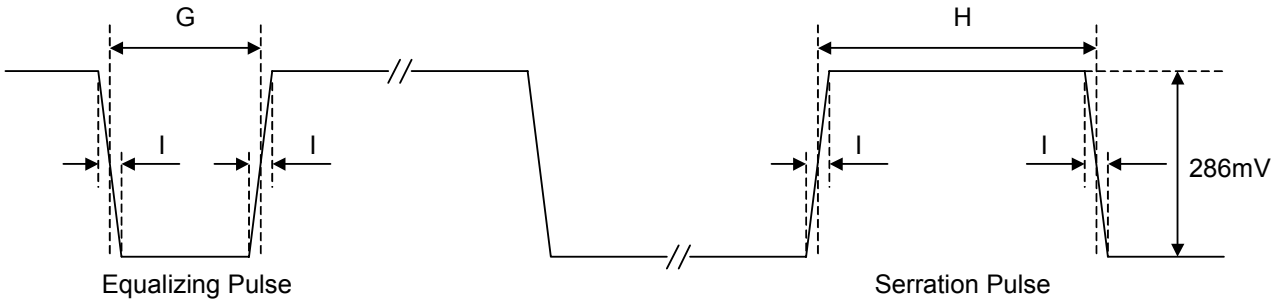


Fig. 18 Equalizing Pulse and Serration Pulse

Symbol		Measurement point	Value	Recommended tolerance	units
	Field Period (derived)		16.6833		msec
	Frame period (derived)		33.3667		msec
	Vertical blanking start before first equalizing pulse	50%	1.5	+/- 0.1	usec
	Vertical blanking (63.556usec x 20lines + 1.5usec)		19* lines + 1.5 usec	0 +/- 0.1	lines usec
	Pre-equalizing duration		3		lines
G	Pre-equalizing pulse width	50%	2.3	+/- 0.1	usec
	Vertical sync duration		3		lines
H	Vertical serration pulse width	50%	4.7	+/- 0.1	usec
	Post-equalizing duration		3		lines
G	Post-equalizing pulse width	50%	2.3	+/- 0.1	usec
I	Sync rise time		140	+/- 20	nsec

*This value can be set by the register.

(1-2-2) FID/VSYNC Timing and Phase of Burst (PAL-M)

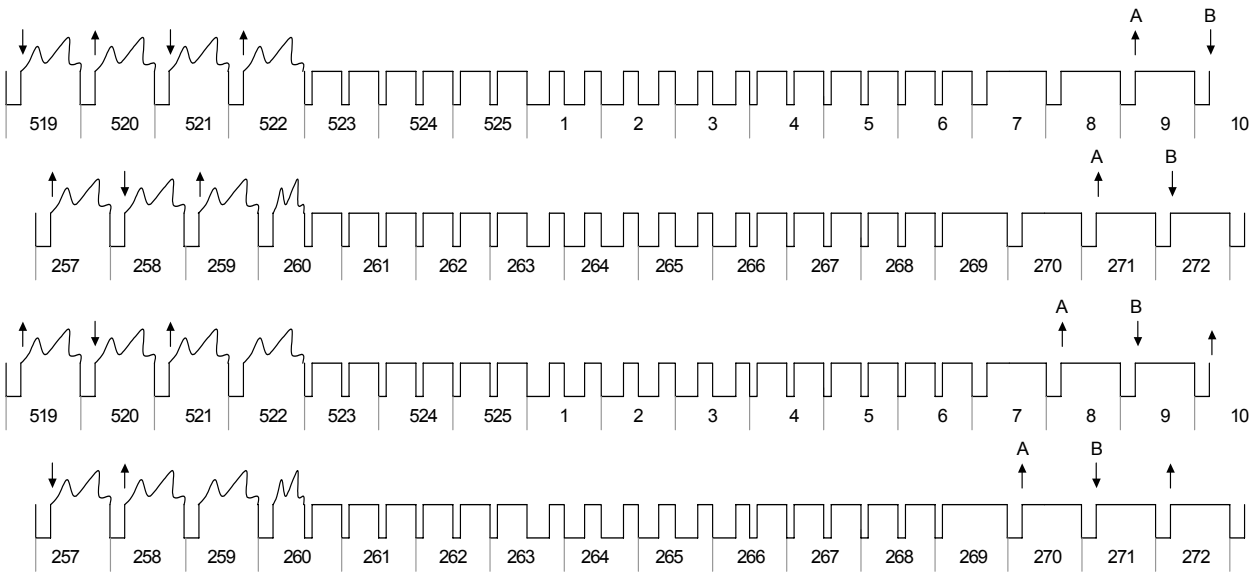


Fig. 19 FID/VSYNC Timing and Phase of Burst

A : Phase of Burst : nominal Value + 135°
B : Phase of Burst : nominal Value - 135°

(2-1) PAL-B,D,G,H,I,N / PAL-60 (Video Process 1 Register [VM3:VM2]-bit = 11)

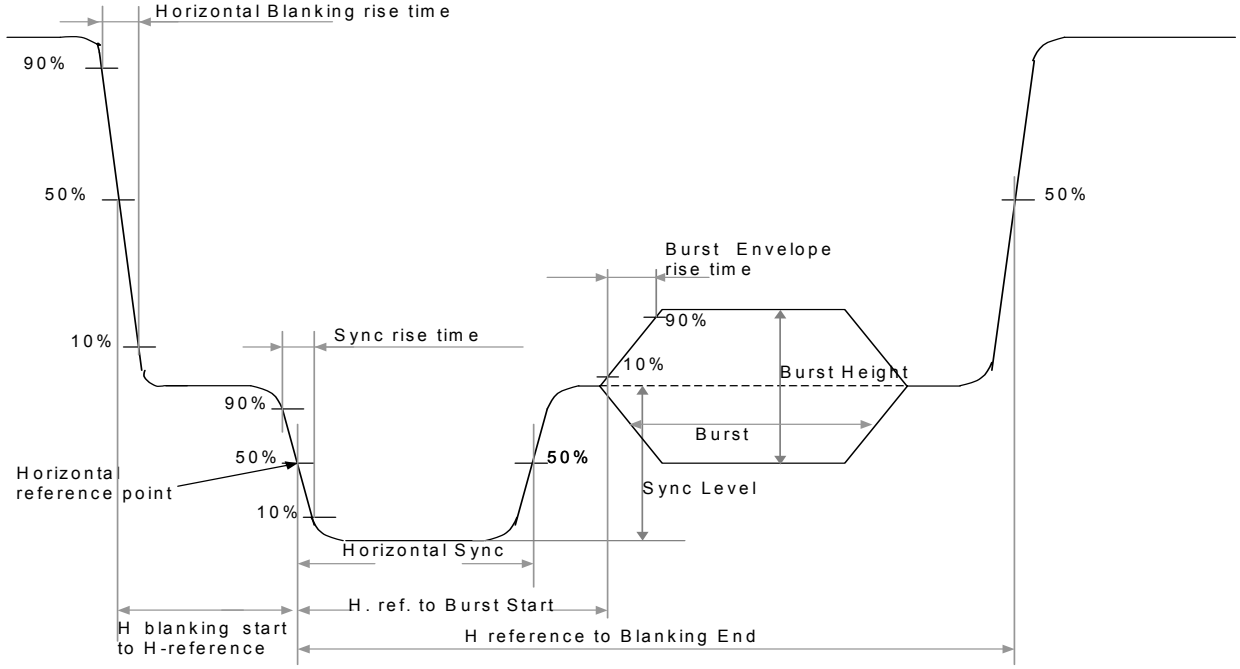


Fig. 20 PAL Waveform

	measurement point	value	Recommended tolerance	units
Total line period(derived)		64.0		usec
Sync Level		300		mV
Horizontal Blanking rise time	10% - 90%	0.3	+/- 0.1	usec
Sync rise time	10% - 90%	0.2	+/- 0.1	usec
Burst envelope rise time	10% - 90%			nsec
H-Blanking start to H-reference	50%	1.5	+/- 0.3	usec
Horizontal Sync	50%	4.7	+/- 0.2	usec
Horizontal reference point to burst start	50%	19	defined by SC/H	cycles
H reference to H-blanking end	50%	10.5		usec
Burst *	50%	10	+/- 1	cycles
Burst Height **		300		mV

(2-2) FID/VSYNC Timing and Phase of Burst PAL-B,D,G,H,I,N / PAL-60
(Video Process 1 Register [VM3:VM2]-bit = 11)

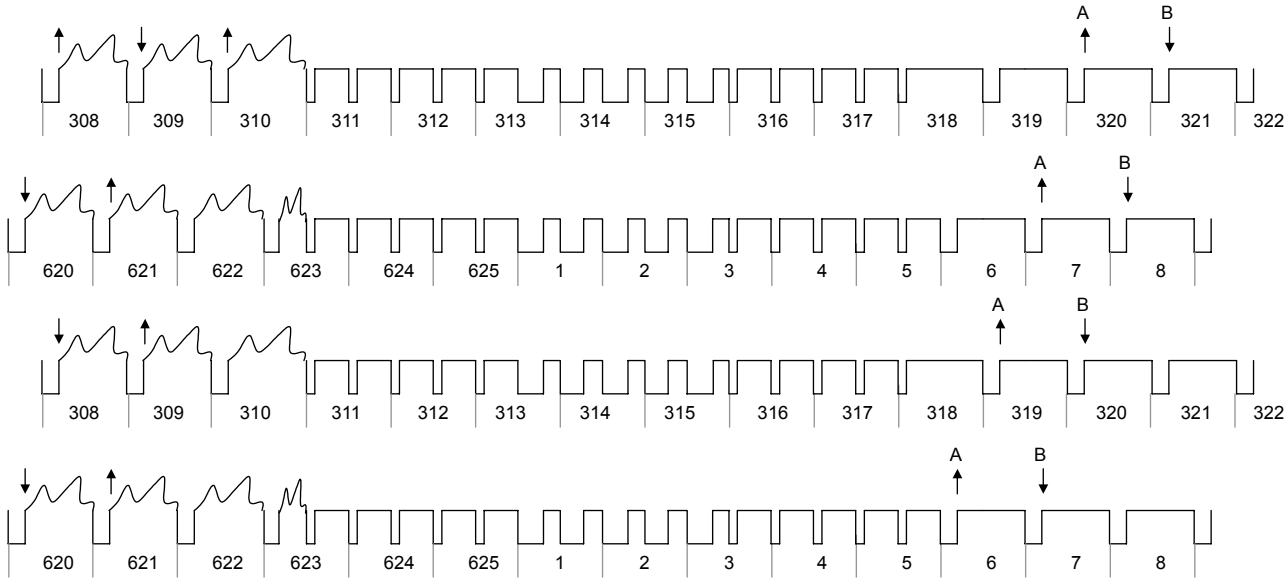


Fig. 21 FID/VSYNC Timing and Phase of Burst

A : Phase of Burst : nominal Value + 135°

B : Phase of Burst : nominal Value - 135°

♦ I²C Control Sequence

AK8813/14 is controlled by I²C bus. The slave address can be selected as 40H or 42H by selecting SELA pin.

SELA	SLAVE Address
PULL Down [Low]	0x40
PULL UP [High]	0x42

Operation :

Write Sequence:

(a)1byte Write Sequence

S	Slave Address	w	A	Sub Address	A	Data	A	Stp
	8-bits		1-bit	8-bits	1-bit	8-bits	1-bit	

(b) Sequential Write Operation

S	Slave Address	w	A	Sub Address(n)	A	Data(n)	A	Data(n+1)	A	•••	Data(n+m)	A	stp
	8-bits		1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit		8-bits	1-bit	

Read Sequence:

S	Slave Address	w	A	Sub Address(n)	A	rS	Slave Address	R	A	Data1	A	Data2	A	Data3	A	•••	Data n	Ā	stp
	8-bits		1	8-bits	1		8-bits		1	8-bits	1	8-bits	1	8-bits	1		8-bits	1	

S, rS : Start Condition
A : Acknowledge (SDA Low)
Ā : Not Acknowledge (SDA High)
stp : Stop Condition
R/W 1 : Read 0 : Write

: Master device (Host)

: Slave device (AK8813/14)

♦ Register Map

Sub Address	Register	Default	R/W	Function
0x00	Interface Mode Register	0x00	R/W	Setting Interface mode
0x01	Video Process 1 Register	0x00	R/W	Setting Standard (NTSC, PAL etc.)
0x02	Video Process 2 Register	0x00	R/W	Setting Closed Caption/Extended Data/VBID
0x03	Video Process 3 Register	0x00	R/W	Setting Composite signal or Component signal Adjusting Chrominance/Luminance Delay
0x04	Reserved Register	0xAA	R/W	
0x05	DAC Mode Register	0x00	R/W	Each DAC On/Off Switch
0x06	Sub Carrier Frequency Register	0x00	R/W	Adjusting Sub-carrier frequency
0x07	Sub Carrier Phase Register	0x00	R/W	Adjusting Sub-carrier phase
0x08	WWS Data 1 Register	0x00	R/W	WSS Data Register
0x09	WWS Data 2 Register	0x00	R/W	WSS Data Register
0x16	Closed Caption 1 Register	0x00	R/W	Closed Caption Lower byte Data
0x17	Closed Caption 2 Register	0x00	R/W	Closed Caption Upper byte Data
0x18	Closed Caption Extended 1 Register	0x00	R/W	Extended Lower byte Data
0x19	Closed Caption Extended 2 Register	0x00	R/W	Extended Upper byte Data
0x1A	Video ID 1 Register	0x00	R/W	Video ID Lower byte Data
0x1B	Video ID 2 Register	0x00	R/W	Video ID Upper byte Data
0x24	Status Register	0x00	R	Status
0x25	Device ID Register	0x00	R	Device ID
0x26	Device Revision Register	0x00	R	Revision

Interface Mode Register (R/W) [Address 0x00]

Sub Address 0x00 **Default Value 0xA4**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BLN4	BLN3	BLN2	BLN1	BLN0	FID	MAS	REC656
Default Value							
1	0	1	0	0	1	0	0

Interface Mode Register Definition

BIT	Register Name		R/W	Definition
bit 0	REC656	REC656 I/F mode bit	R/W	0 : REC656 non-decode 1 : REC656 decode (At Rec.656 mode operation, MAS-bit should be 0.)
bit 1	MAS	Master mode Set bit	R/W	0 : Slave mode 1 : Master mode When REC=0,it's valid
bit 2	FID	Field ID Set bit	R/W	0 : Select VSYNC 1 : Select FID
bit 3 ~ bit 7	BLN0 ~ BLN4	Blanking Line No bit	R/W	Line Blanking No.

Video Process 1 Register (R/W) [Address 0x01]

Sub Address 0x01 **Default Value 0x30**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BBG	CBG	SETUP	SCR	VM3	VM2	VM1	VM0
Default Value							
0	0	1	1	0	0	0	0

Video Process 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	VM0 ~ VM3	Video Mode 0 Register ~ Video Mode 3 Register	R/W	[VM1:VM0]-bit 00 : 3.57954545 MHz 01 : 3.57561188 MHz 10 : 3.5820558 MHz 11 : 4.43361875 MHz [VM3:VM2]-bit 00 : 525/60 01 : 525/60 PAL (PAL-M etc.) 10 : Reserved 11 : 625/50 PAL (PAL-B,D,G,H,I,N)
bit 4	SCR	Sub Carrier Reset bit	R/W	0 : Sub C. Phase Reset off 1 : Standard Field Reset
bit 5	SETUP	Setup bit	R/W	0 : No Set-up 1 : 7.5 IRE Set-up
bit 6	CBG	Color Bar Generator bit	R/W	0 : Video Encode 1 : Generates color bar
bit 7	BBG	Black Burst Generator	R/W	0 : Video Encode 1 : Generates black burst

Register Setting of each standard is shown as following ;

	VM3-VM0
NTSC-M	0000
PAL-B,D,G,H,I	1111
PAL-M	0101
PAL-60	0111
NTSC4.43	0011

- When SCR is “ON”, the Subcarrier Phase is reset every 4 fields for NTSC, every 8 fields for PAL.
- Even when SETUP is “ON”, there is no Set-up (Pedestal) during the blanking lines.

Video Process 2 Register (R/W) [Address 0x02]

Sub Address 0x02 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	WSS	CC284	CC21	VBID
Default Value							
0	0	0	0	0	0	0	0

Video Process 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0	VBID	Video ID bit	R/W	0 : Video ID off 1 : Video ID on
bit 1	CC21	Closed Caption bit	R/W	0 : Closed caption off 1 : Closed Caption on
bit 2	CC284	Closed Caption Extended Data bit	R/W	0 : Extended Data off 1 : Extended data on
bit 3	WSS	WSS set bit	R/W	0 : WSS off 1 : WSS on
bit 4 ~ bit 7	Reserved	Reserved bit	R/W	Reserved

Video Process 3 Register (R/W) [Address 0x03]

Sub Address 0x03 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	SYD2	SYD1	SYD0	CYD2	CYD1	CYD0
Default Value							
0	0	0	0	0	0	0	0

Video Process 3 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	CYD0 ~ CYD2	Composite Y Delay bit	R/W	S-Video Y Component delay no. from Chroma: 2's comp.
bit 3 ~ bit 5	SYD0 ~ SYD2	S-video Y Delay bit	R/W	Composite Y Component delay no. from Chroma: 2's comp.
bit 6 ~ bit 7	Reserved	Reserved bit	R/W	Reserved

- S-video and Y component of the composite signal can be shifted for the chroma signal independently at ±3-system clock (27MHz).

Reserved Register (R/W) [Address 0x04]

Sub Address 0x04 **default Value 0xAA**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value							
1	0	1	0	1	0	1	0

Reserved

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	Reserved	Reserved bit.	R/W	Reserved

DAC Mode Register (R/W) [Address 0x05]

Sub Address 0x05 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	OUTCP	OUTC	OUTY
Default Value							
0	0	0	0	0	0	0	0

DAC Mode Register Definition

BIT	Register Name		R/W	Definition
bit 0	OUTY	YDAC Out bit	R/W	0: Y signal output : OFF 1: Y signal output : ON
bit 1	OUTC	CDAC Out bit	R/W	0: Chrominance signal output : OFF 1: Chrominance signal output : ON
bit 2	OUTCP	CPDAC Out bit	R/W	0: Composite video signal or U signal output : OFF 1: Composite video signal or U signal output : ON
bit 3 ~ bit 7	Reserved	Reserved bit.	R/W	Reserved

- Video output of AK8813/14 (DAC) can be forced “OFF” independently.
  The output of DAC that is forced “OFF” is Hi-impedance. When three DACs are forced “OFF”, then the internal VREF is also forced “OFF”. In this case, it takes several milliseconds before the internal VREF reaches the proper voltage after any DAC becomes “ON”.

Sub Carrier Frequency Control Register (R/W) [Address 0x06]

Sub Address 0x06 **default Value 0x00**

bit 7	Bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SUBF7	SUBF6	SUBF5	SUBF4	SUBF3	SUBF2	SUBF1	SUBF0
Default Value							
0	0	0	0	0	0	0	0

Sub Carrier Frequency Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SUBF0 ~ SUBF7	Sub Carrier Frequency Control bit	R/W	Adjustment of frequency between +127 and –128 step of 0.8Hz

Sub Carrier Phase Control Register (R/W) [Address 0x07]

Sub Address 0x07 **default Value 0x00**

bit 7	Bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SUBP7	SUBP6	SUBP5	SUBP4	SUBP3	SUBP2	SUBP1	SUBP0
Default Value							
0	0	0	0	0	0	0	0

Sub Carrier Phase Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SUBP0 ~ SUBP7	Sub Carrier Phase Control bit	R/W	Adjustment of frequency between +127 and –128 step of 0.8Hz

- Sub- carrier phase is adjustable by (360° /256) step.

WSS Data 1 Register (R/W) [Address 0x08]

WSS Data 2 Register (R/W) [Address 0x09]

Sub Address 0x08 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x09 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8
Default Value							
0	0	0	0	0	0	0	0

- AK8813/14 generates the necessary sub-carrier frequency from a system clock by DFS (Digital Frequency Synthesizer)
- Frequency of default is adjustable by specifying this bit. This bit adjusts the default frequency.

Closed Caption Data 1 Register (R/W) [Address 0x16]

Closed Caption Data 2 Register (R/W) [Address 0x17]

Sub Address 0x16 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC 6	CC5	CC4	CC3	CC2	CC1	CC0
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x17 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8
Default Value							
0	0	0	0	0	0	0	0

Closed Caption Extended Data 1 Register (R/W) [Address 0x18]

Closed Caption Extended Data 2 Register (R/W) [Address 0x19]

Sub Address 0x18 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x19 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8
Default Value							
0	0	0	0	0	0	0	0

- When the 2nd byte of Closed Caption Data and Extended Data is written in, AK8813/14 recognizes the renewed data and encodes it in the video line.
  When the data is not renewed AK8813/14 outputs NULL code.

Video ID 1 Register (R/W) [Address 0x1A]

Video ID 2 Register (R/W) [Address 0x1B]

Sub Address 0x1A **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x1B **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14
Default Value							
0	0	0	0	0	0	0	0

- Please write value 0 at Reserved bit.
- Bit numbers correspond to Fig. 5 VBID code assignment.
- AK8813/14 generates CRC 6 bit data automatically.

Status Register (R/W) [Address 0x24]

Sub Address 0x24

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	EN284	EN21	SYNC	STS2	STS1	STS0

Status Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	STS0 ~ STS2	Status bit	R	Shows the processing field No.
bit 3	SYNC bit	S-video Y Delay bit	R	0 : Missing synchronization in slave mode. 1 : Synchronization was achieved.
bit 4	EN21	Encode21 bit	R	0 : Wait for the appointed video line to encode. 1 : Ready for the C.C. data input to the register.
bit 5	EN284	Encode 284 bit	R	0 : Wait for the appointed video line to encode. 1 : Ready for the C.C. data input to the register.
bit 6 ~ bit 7	Reserved	Reserved bit.	R	Reserved

- Status Register becomes effective when SYNC bit turns to “1”.
  When in master mode operation, this bit is ”1”.
- STS2-STS2 holds the field number of processing. Some time lag is inevitable for the I^2C acquisition.
- Closed caption data should be renewed after firm that the EN* flag is “1”.
  EN* flag bit is cleared after the second byte(Sub address 17H,19H) was accessed.
- Reserved-bit is always value 0.

Device ID Register (R/W) [Address 0x25]

Sub Address 0x25 **default Value 0x14**

bit 7	Bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
Default Value							
0	0	0	1	0	1	0	0

Device ID Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	DEV0 ~ DEV7	Device ID bit	R	Shows the Device ID. "0x13" is assigned for AK8813. "0x14" is assigned for AK8814.

Revision ID Register (R/W) [Address 0x26]

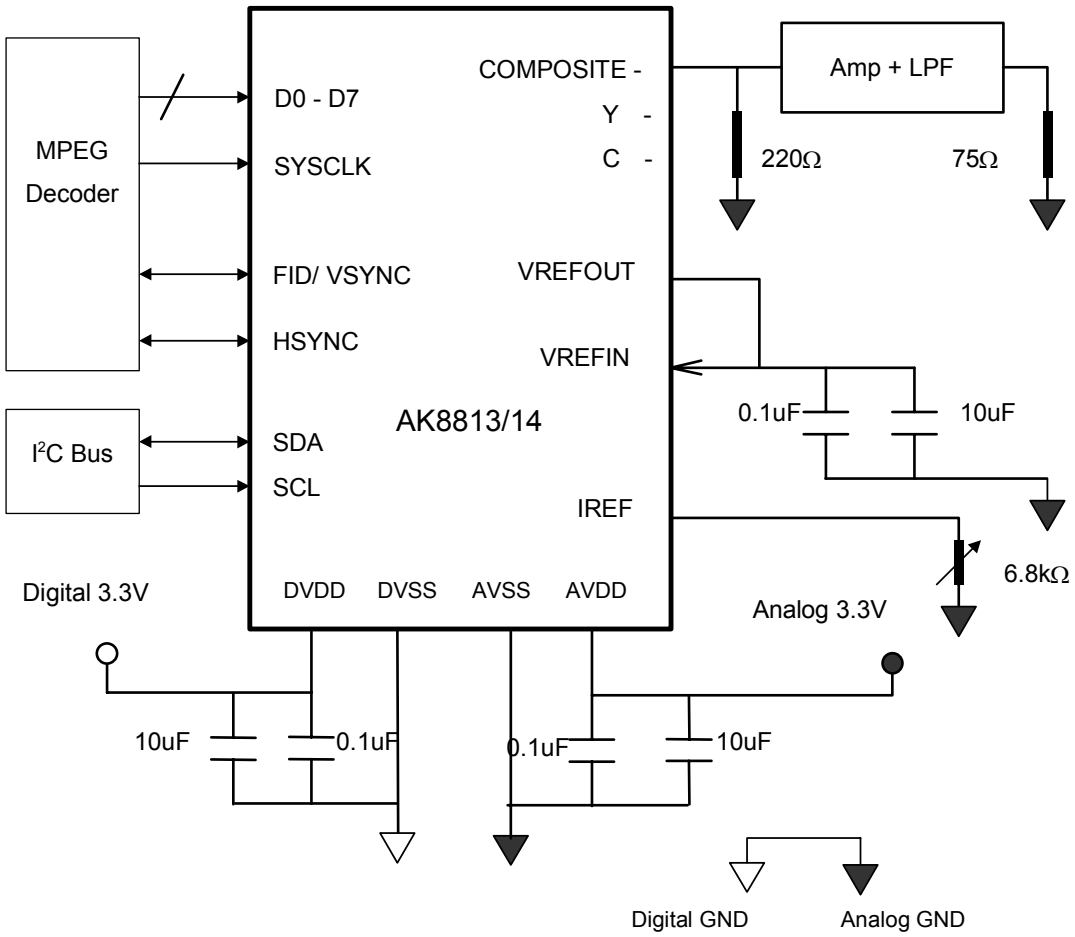
Sub Address 0x26 **default Value 0x00**

bit 7	Bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
Default Value							
0	0	0	0	0	0	0	0

Revision ID Register Definition

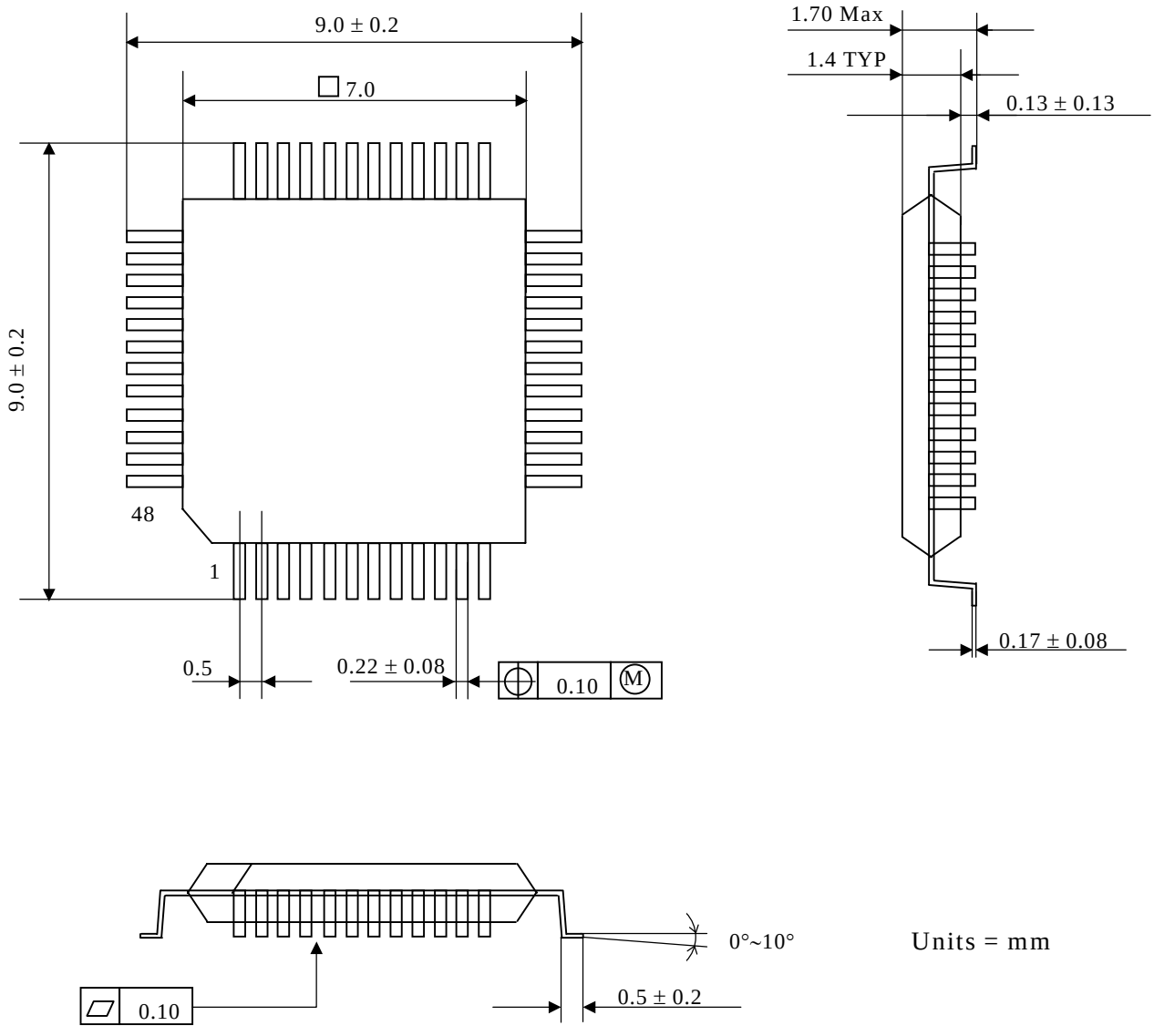
BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	REV0 ~ REV7	Revision ID bit	R	This value will be modified when the control software has to be modified. Shows the Revision ID.

SYSTEM CONNECTION EXAMPLE



PACKAGE

48pin LQFP



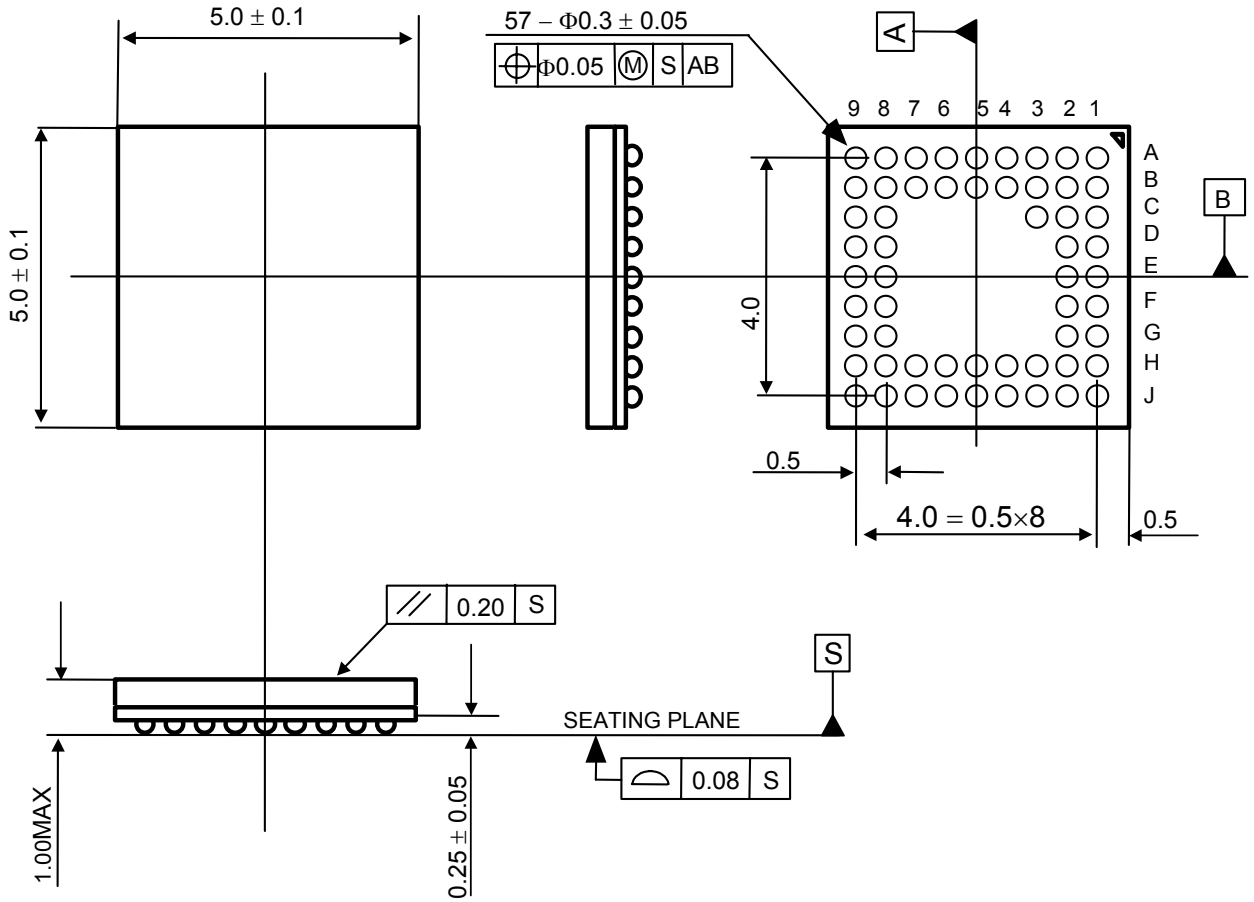
Package & Lead frame material

Package molding compound : Epoxy

Lead frame material : Cu

Lead frame surface treatment : Solder plate

57Pin FBGA

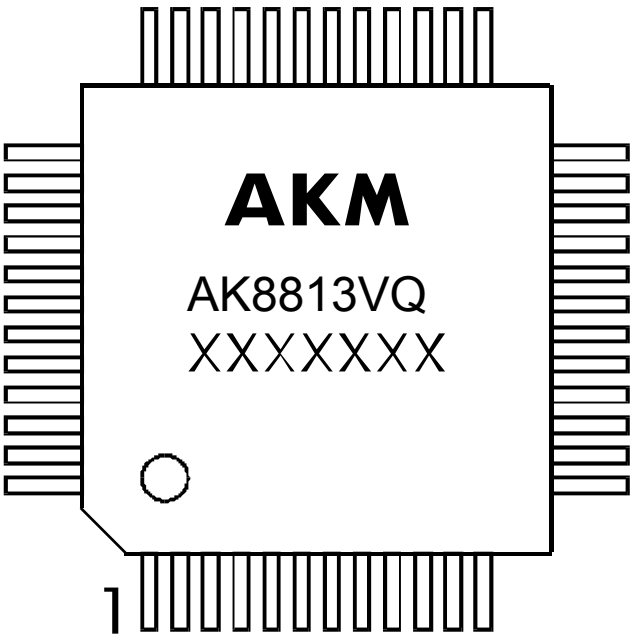


Package & Lead frame material

Package molding compound: Epoxy

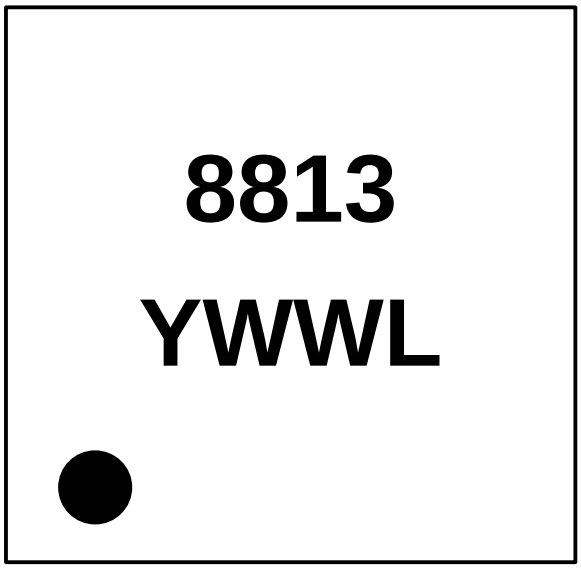
Interposer material: BT resin

48pin LQFP (Pb Free Package)



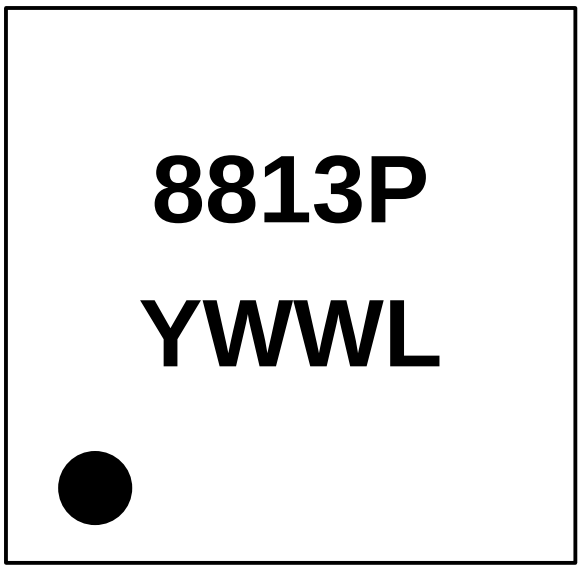
1) Asahi Kasei Logo
2) Marketing Code : AK8813
3) Date Code : XXXXXXX (7 digits)
4) Pin #1 indication

57Pin FBGA



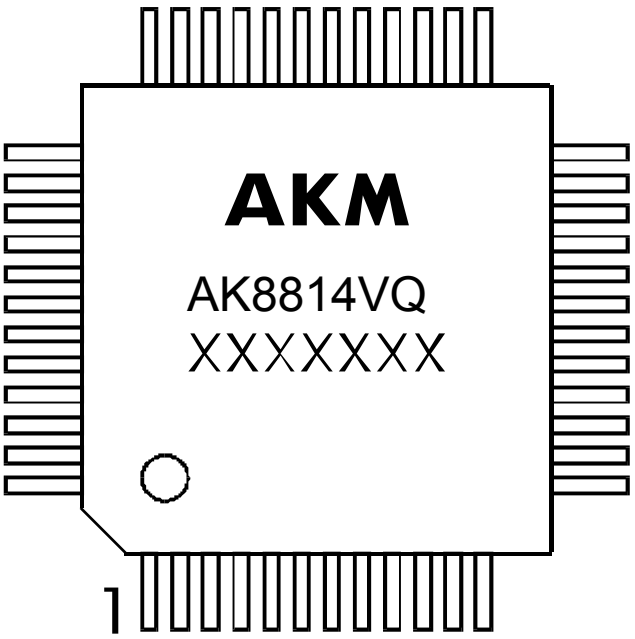
1) Pin #1 indication
2) Marketing Code : 8813
3) Date Code : YWWL (4 digits)
Y: Year
WW: week
L: Lot

57Pin FBGA (Pb Free Package)



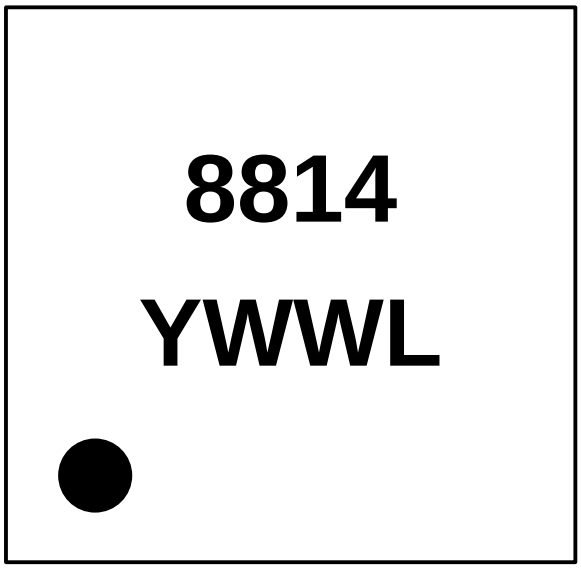
1) Pin #1 indication
2) Marketing Code : 8813P
3) Date Code : YWWL (4 digits)
Y: Year
WW: week
L: Lot

48pin LQFP (Pb Free Package)



1) Asahi Kasei Logo
2) Marketing Code : AK8814
3) Date Code : XXXXXXX (7 digits)
4) Pin #1 indication

57Pin FBGA (Pb Free Package)



1) Pin #1 indication
2) Marketing Code : 8814
3) Date Code : YWWL (4 digits)
Y: Year
WW: week
L: Lot

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