512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL, Mini-DIMM

FEATURES

- 244-pin, dual in-line memory module (Mini-DIMM)
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800, 667, 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to $3.6V$
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Auto and Self Refresh Capability (64ms: 8,192 cycle refresh)
- Gold (Au) edge contacts
- RoHS compliant
- Single Rank
- Package option
  - 244 Pin Mini-DIMM
  - PCB – 30.00mm (1.181") TYP

DESCRIPTION

The WV3HG64M72EER is a 64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of nine 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 244-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t_{RCD}-t_{RP}	3-3-3	4-4-4	5-5-5	6-6-6

*Consult factory for availability.

PIN CONFIGURATION

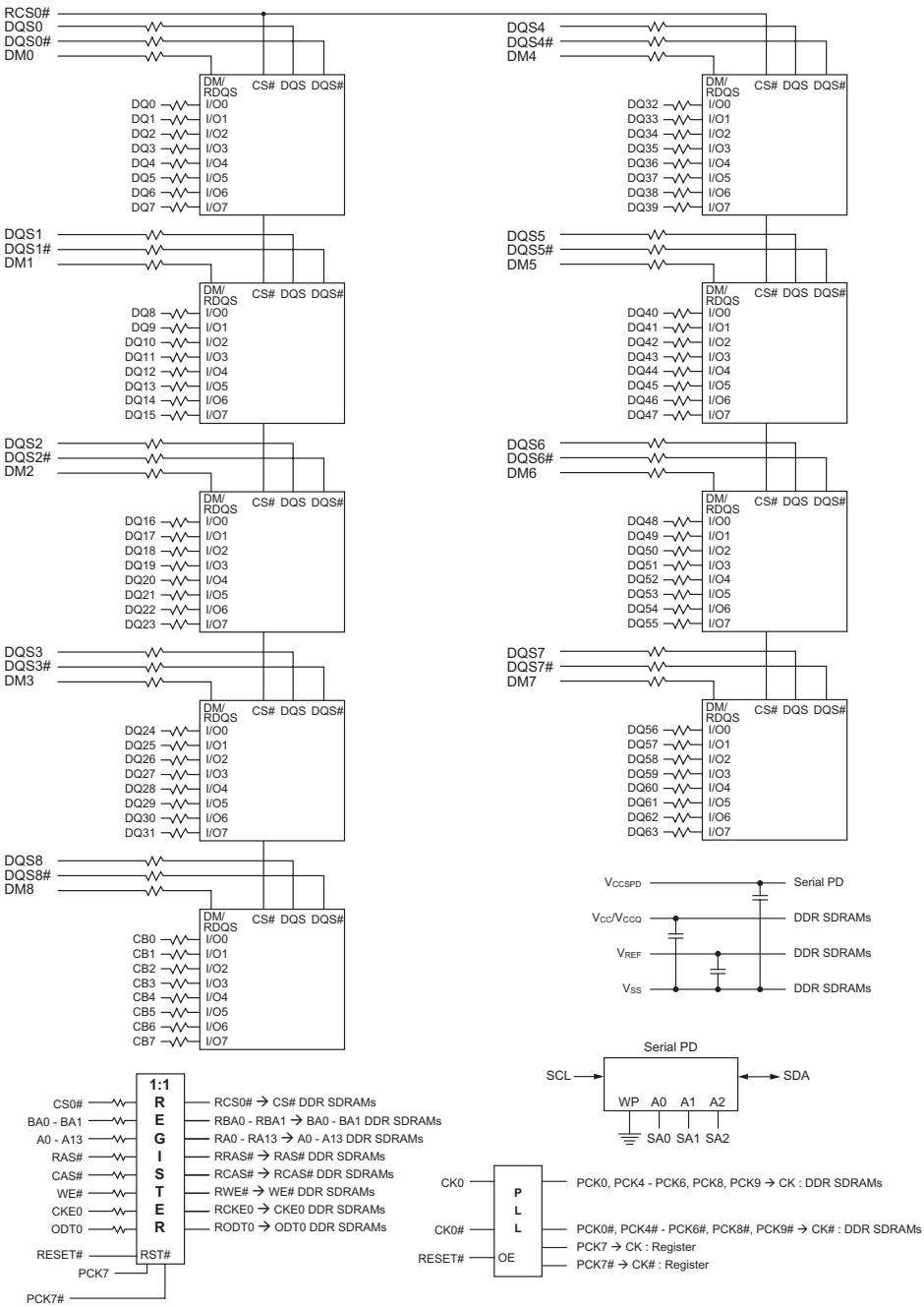
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{REF}	62	A4	123	V_{SS}	184	V_{CCQ}
2	V_{SS}	63	V_{CCQ}	124	DQ4	185	A3
3	DQ0	64	A2	125	DQ5	186	A1
4	DQ1	65	V_{CC}	126	V_{SS}	187	V_{CC}
5	V_{SS}	66	V_{SS}	127	DM0	188	CK0
6	DQS0#	67	V_{SS}	128	NC	189	CK0#
7	DQS0	68	NC	129	V_{SS}	190	V_{CC}
8	V_{SS}	69	V_{CC}	130	DQ6	191	A0
9	DQ2	70	A10/AP	131	DQ7	192	BA1
10	DQ3	71	BA0	132	V_{SS}	193	V_{CC}
11	V_{SS}	72	V_{CC}	133	DQ12	194	RAS#
12	DQ8	73	WE#	134	DQ13	195	V_{CCQ}
13	DQ9	74	V_{CCQ}	135	V_{SS}	196	CS0#
14	V_{SS}	75	CAS#	136	DM1	197	V_{CCQ}
15	DQS1#	76	V_{CCQ}	137	NC	198	ODT0
16	DQS1	77	NC	138	V_{SS}	199	A13
17	V_{SS}	78	NC	139	NC	200	V_{CC}
18	RESET#	79	V_{CCQ}	140	NC	201	NC
19	NC	80	NC	141	V_{SS}	202	V_{SS}
20	V_{SS}	81	V_{SS}	142	DQ14	203	DQ36
21	DQ10	82	DQ32	143	DQ15	204	DQ37
22	DQ11	83	DQ33	144	V_{SS}	205	V_{SS}
23	V_{SS}	84	V_{SS}	145	DQ20	206	DM4
24	DQ16	85	DQS4#	146	DQ21	207	NC
25	DQ17	86	DQS4	147	V_{SS}	208	V_{SS}
26	V_{SS}	87	V_{SS}	148	DM2	209	DQ38
27	DQS2#	88	DQ34	149	NC	210	DQ39
28	DQS2	89	DQ35	150	V_{SS}	211	V_{SS}
29	V_{SS}	90	V_{SS}	151	DQ22	212	DQ44
30	DQ18	91	DQ40	152	DQ23	213	DQ45
31	DQ19	92	DQ41	153	V_{SS}	214	V_{SS}
32	V_{SS}	93	V_{SS}	154	DQ28	215	DM5
33	DQ24	94	DQS5#	155	DQ29	216	NC
34	DQ25	95	DQS5	156	V_{SS}	217	V_{SS}
35	V_{SS}	96	V_{SS}	157	DM3	218	DQ46
36	DQS3#	97	DQ42	158	NC	219	DQ47
37	DQS3	98	DQ43	159	V_{SS}	220	V_{SS}
38	V_{SS}	99	V_{SS}	160	DQ30	221	DQ52
39	DQ26	100	DQ48	161	DQ31	222	DQ53
40	DQ27	101	DQ49	162	V_{SS}	223	V_{SS}
41	V_{SS}	102	V_{SS}	163	CB4	224	NC
42	CB0	103	SA2	164	CB5	225	NC
43	CB1	104	NC	165	V_{SS}	226	V_{SS}
44	V_{SS}	105	V_{SS}	166	DM8	227	DM6
45	DQS8#	106	DQS6#	167	NC	228	NC
46	DQS8	107	DQS6	168	V_{SS}	229	V_{SS}
47	V_{SS}	108	V_{SS}	169	CB6	230	DQ54
48	CB2	109	DQ50	170	CB7	231	DQ55
49	CB3	110	DQ51	171	V_{SS}	232	V_{SS}
50	V_{SS}	111	V_{SS}	172	NC	233	DQ60
51	NC	112	DQ56	173	V_{CCQ}	234	DQ61
52	V_{CCQ}	113	DQ57	174	*CKE1	235	V_{SS}
53	CKE0	114	V_{SS}	175	V_{CC}	236	DM7
54	V_{CC}	115	DQS7#	176	NC	237	NC
55	NC	116	DQS7	177	NC	238	V_{SS}
56	NC	117	V_{SS}	178	V_{CCQ}	239	DQ62
57	V_{CCQ}	118	DQ58	179	A12	240	DQ63
58	A11	119	DQ59	180	A9	241	V_{SS}
59	A7	120	V_{SS}	181	V_{CC}	242	SDA
60	V_{CC}	121	SA0	182	A8	243	SCL
61	A5	122	SA1	183	A6	244	V_{CCSPD}

RESET (pin 18) is connected to both OE of the PLL and Reset# of the register .

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data strobes
DQS0#-DQS8#	Data strobes complement
ODT0	On-die termination control
CK0,CK0#	Clock Inputs, positive line
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
RESET#	Register Reset Input
DM (0-8)	Data Masks
V_{CCSPD}	SPD Power
V_{CC}	Core and I/O Power (1.8V)
V_{CCQ}	I/O Power (1.8V)
A10/AP	Address Input/Auto Precharge
V_{SS}	Ground
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	Serial Presence Detect(SPD) Clock Input
NC	Spare pins, No connect
V_{REF}	Input/Output Reference

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms ±5% unless otherwise specified.

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V_{CC}	1 .7	1 .8	1 .9	V	1
I/O Supply voltage	V_{CCQ}	1 .7	1 .8	1 .9	V	4
V_{CCL} Supply voltage	V_{CCL}	1 .7	1 .8	1 .9	V	4
I/O Reference voltage	V_{REF}	0.49 x V_{CCQ}	0.50 x V_{CCQ}	0.51 x V_{CCQ}	V	2
I/O Termination voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF} + 0.04	V	3

Notes:

1. V_{CC} V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
2. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{CCQ} tracks with V_{CC}; V_{CCL} track with V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		MIN	MAX	Unit
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-1.0	2.3	V
V_{CCQ}	Voltage on V_{CCQ} pin relative to V_{SS}		-0.5	2.3	V
V_{CCL}	Voltage on V_{CCL} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage temperature		-55	100	°C
T_{CASE}	Device operating temperature		0	85	°C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; V_{REF} input 0V<V_{IN}<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-5	5	µA
		CK, CK#	-10	10	µA
		DM	-5	5	µA
I_{OZ}	Output leakage current; 0V<V_{OUT}<V_{CCQ}; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-18	18	µA

INPUT/OUTPUT CAPACITANCE

TA=25 0 C, f=1 00MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 - A13, BA0 - BA1 ,RAS#,CAS#,WE#)	C_{IN1}	6.5	7.5	pF
Input capacitance (CKE0), (ODT0)	C_{IN2}	6.5	7.5	pF
Input capacitance (CS0#)	C_{IN3}	6.5	7.5	pF
Input capacitance (CK0, CK0#)	C_{IN4}	6	7	pF
Input capacitance (DM0 - DM8), (DQS0 - DQS8)	C_{IN5}	6.5	8	pF
Input capacitance (DQ0 - DQ63), (CB0 - CB7)	C_{OUT1}	6.5	8	pF

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T_{OPER}	0 to 85	°C	1, 2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51 .2
2. At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.1 25	V_{REF} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.250	—	V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533 (DDR2-667 & DDR2-806) TBD	V_{IL}(AC)	—	V_{REF} - 0.250	V

DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only; T_A = 0°C, V_{CC} = 1.9V

Symbol	Parameter	Condition		806	665	534	403	Unit
I_{CC0}*	Operating one bank active-precharge;	$t_{CK} = t_{CK(DD)}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	1120	1120	mA
I_{CC1}*	Operating one bank active-read-precharge;	I_{OUT} = 0mA; BL = 4; CL = CL(I_{CC}); $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING; Data pattern is same as I_{CC4W}.		TBD	TBD	1255	1255	mA
I_{CC2P}**	Precharge power-down current;	All banks idle; $t_{CK} = t_{CK(I_{CC})}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	TBD	472	472	mA
I_{CC2Q}**	Precharge quite standby current;	All banks idle; $t_{CK} = t_{CK(I_{CC})}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	TBD	670	670	mA
I_{CC2N}**	Precharge standby current;	All banks idle; $t_{CK} = t_{CK(I_{CC})}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING		TBD	TBD	715	715	mA
I_{CC3P}**	Active power-down current;	All banks open; $t_{CK} = t_{CK(I_{CC})}$, CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	TBD	670	670	mA
			Slow PDN Exit MRS(12) = 1	TBD	TBD	508	508	mA
I_{CC3N}**	Active standby current;	All banks open; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	850	850	mA
I_{CC4W}*	Operating burst write current;	All banks open; Continuous burst writes; BL = 4; CL = CL(ICC); AL = 0; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	1480	1390	mA
I_{CC4R}*	Operating burst read current;	All banks open; Continuous burst reads; TOUT = 0mA; BL = 4; CL = CL(ICC); AL = 0; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RAS} = t_{RAS\ MIN(I_{CC})}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC4W}.		TBD	TBD	1525	1390	mA
I_{CC5}**	Burst auto refresh current;	$t_{CK} = t_{CK(I_{CC})}$; Refresh command at every $t_{RC(I_{CC})}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	1660	1660	mA
I_{CC6}**	Self refresh current;	CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	TBD	472	472	mA
I_{CC7}*	Operating bank interleave read current;	All bank interleaving reads; I_{OUT} = 0mA; BL = 4; CL = CL(I_{CC}); AL = $t_{RCD(I_{CC})}$ - 1*$t_{CK(I_{CC})}$; $t_{CK} = t_{CK(I_{CC})}$; $t_{RC} = t_{RC(I_{CC})}$; $t_{RRD} = t_{RRD\ MIN(I_{CC})}$ = 1*$t_{CK(I_{CC})}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING		TBD	TBD	2380	2380	mA

Notes:

I_{CC} specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS

$0°C \le T_{CASE} < +70°C$; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

	Parameter		Symbol	806		665		534		403		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Clock	Clock cycle time	CL=6	$t_{CK}(6)$	TBD	TBD	TBD	TBD					ps
		CL=5	$t_{CK}(5)$	TBD	TBD	TBD	TBD					ps
		CL=4	$t_{CK}(4)$	TBD	TBD	TBD	TBD	3,750	8,000	5,000	8,000	ps
		CL=3	$t_{CK}(3)$	TBD	TBD	TBD	TBD	5,000	8,000	5,000	8,000	ps
	CK high-level width		t_{CH}	TBD	TBD	TBD	TBD	0.45	0.55	0.45	0.55	t_{CK}
	CK low-level width		t_{CL}	TBD	TBD	TBD	TBD	0.45	0.55	0.45	0.55	t_{CK}
	Half clock period		t_{HP}	TBD	TBD	TBD	TBD	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
	Clock jitter		t_{JIT}	TBD	TBD	TBD	TBD	TBD		TBD		ps
Data	DQ output access time from CK/CK#		t_{AC}	TBD	TBD	TBD	TBD	-500	+500	-600	+600	ps
	Data-out high impedance window from CK/CK#		t_{HZ}	TBD	TBD	TBD	TBD		$t_{AC(MAX)}$		$t_{AC(MAX)}$	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	TBD	TBD	TBD	TBD	$t_{AC(MN)}$	$t_{AC(MAX)}$	$t_{AC(MN)}$	$t_{AC(MAX)}$	ps
	DQ and DM input setup time relative to DQS		t_{DS}	TBD	TBD	TBD	TBD	100		150		
	DQ and DM input hold time relative to DQS		t_{QH}	TBD	TBD	TBD	TBD	225		275		
	DQ and DM input pulse width (for each input)		t_{DIPW}	TBD	TBD	TBD	TBD	0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}	TBD	TBD	TBD	TBD		400		450	ps
	DQ-DQS hold, DQS to first DQ to go nonvalid, per access		t_{HQ}	TBD	TBD	TBD	TBD	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ps
	Data valid output window (DVW)		t_{DVW}	TBD	TBD	TBD	TBD	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	TBD	TBD	TBD	TBD	0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	TBD	TBD	TBD	TBD	0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	TBD	TBD	TBD	TBD	-450	+450	-500	+500	Ps
	DQS falling edge to CK rising - setup time		t_{DSS}	TBD	TBD	TBD	TBD	0.2		0.2		t_{CK}
	DQS falling edge from CK rising - hold time		t_{DSH}	TBD	TBD	TBD	TBD	0.2		0.2		t_{CK}
	O DQS-DQ skew, DOS to last DQ valid, per group, per access		t_{DQSQ}	TBD	TBD	TBD	TBD		300		350	ps
	DQS read preamble		t_{RPRE}	TBD	TBD	TBD	TBD	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	TBD	TBD	TBD	TBD	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	TBD	TBD	TBD	TBD	0		0		ps
	DQS write preamble		t_{WPRE}	TBD	TBD	TBD	TBD	0.35		0.35		t_{CK}
	DQS write postamble		t_{WPST}	TBD	TBD	TBD	TBD	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	TBD	TBD	TBD	TBD	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t_{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

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AC TIMING PARAMETERS (continued)

0°C ≤ T_{CASE} < +70°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

	Parameter	Symbol	806		665		534		403		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Command and Address	Address and control input pulse width for each input	t_{IPW}	TBD	TBD	TBD	TBD	0.6		0.6		t_{CK}
	Address and control input setup time	t_{IS}	TBD	TBD	TBD	TBD	250		250		ps
	Address and control input hold time	t_{IH}	TBD	TBD	TBD	TBD	375		475		ps
	CAS# to CAS# command delay	t_{CCD}	TBD	TBD	TBD	TBD	2		2		ps
	ACTIVE to ACTIVE (same bank) command	t_{RC}	TBD	TBD	TBD	TBD	60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	TBD	TBD	TBD	TBD	7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	TBD	TBD	TBD	TBD	15		15		ns
	Four Bank Activate period	t_{FAW}	TBD	TBD	TBD	TBD	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t_{RAS}	TBD	TBD	TBD	TBD	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	TBD	TBD	TBD	TBD	7.5		7.5		ns
	Write recovery time	t_{WR}	TBD	TBD	TBD	TBD	15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	TBD	TBD	TBD	TBD	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
	Internal WRITE to READ command delay	t_{WTR}	TBD	TBD	TBD	TBD	7.5		10		ns
	PRECHARGE command period	t_{RP}	TBD	TBD	TBD	TBD	15		15		ns
	PRECHARGE ALL command period	t_{RPA}	TBD	TBD	TBD	TBD	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns
	LOAD MODE command cycle time	t_{MRD}	TBD	TBD	TBD	TBD	2		2		t_{CK}
	CKE low to CK, CK# uncertainty	t_{DELAY}	TBD	TBD	TBD	TBD	4.375		4.375		ns
Self Refresh	REFRESH to Active or Refresh to Refresh command interval	t_{RFC}	TBD	TBD	TBD	TBD	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t_{REFI}	TBD	TBD	TBD	TBD		7.8		7.8	ns
	Exit self refresh to non-READ command	t_{XSNR}	TBD	TBD	TBD	TBD	$t_{RPC(MIN)}$ + 10		$t_{RFC(MIN)}$ + 10		ns
	Exit self refresh to READ	t_{XSRD}	TBD	TBD	TBD	TBD	200		200		t_{CK}
	Exit self refresh timing reference	t_{ISXR}	TBD	TBD	TBD	TBD	t_{IS}		t_{IS}		ps
ODT	ODT turn-on delay	t_{AOND}	TBD	TBD	TBD	TBD	2	2	2	2	t_{CK}
	ODT turn-on	t_{ACN}	TBD	TBD	TBD	TBD	$t_{AC(MIN)}$	$t_{AC(MAX)}$ + 1000	$t_{AC(MIN)}$	$t_{AC(MAX)}$ + 1000	ps
	ODT turn-off delay	t_{AOFD}	TBD	TBD	TBD	TBD	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	TBD	TBD	TBD	TBD	$t_{AC(MIN)}$	$t_{AC(MAX)}$ + 600	$t_{AC(MIN)}$	$t_{AC(MAX)}$ + 600	ps
	ODT turn-on (power-down mode)	t_{AONPD}	TBD	TBD	TBD	TBD	$t_{AC(MIN)}$ + 2000	2 x t_{CK} + $t_{AC(MAX)}$ + 1000 +1000	$t_{AC(MIN)}$ + 2000	2 x t_{CK} + $t_{AC(MAX)}$ + 1000	ps
	ODT turn-off (power-down mode)	t_{AOFPD}	TBD	TBD	TBD	TBD	$t_{AC(MIN)}$ + 2000	2 x t_{CK} + $t_{AC(MAX)}$ + 1000 +1000	$t_{AC(MIN)}$ + 2000	2 x t_{CK} + $t_{AC(MAX)}$ + 1000	ps
	ODT to power-down entry latency	t_{ANPD}	TBD	TBD	TBD	TBD	3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}					8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}					2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}					6-AL		6-AL		t_{CK}
	Exit precharge power-down to any non-READ command	t_{XP}					2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}					3		3		t_{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

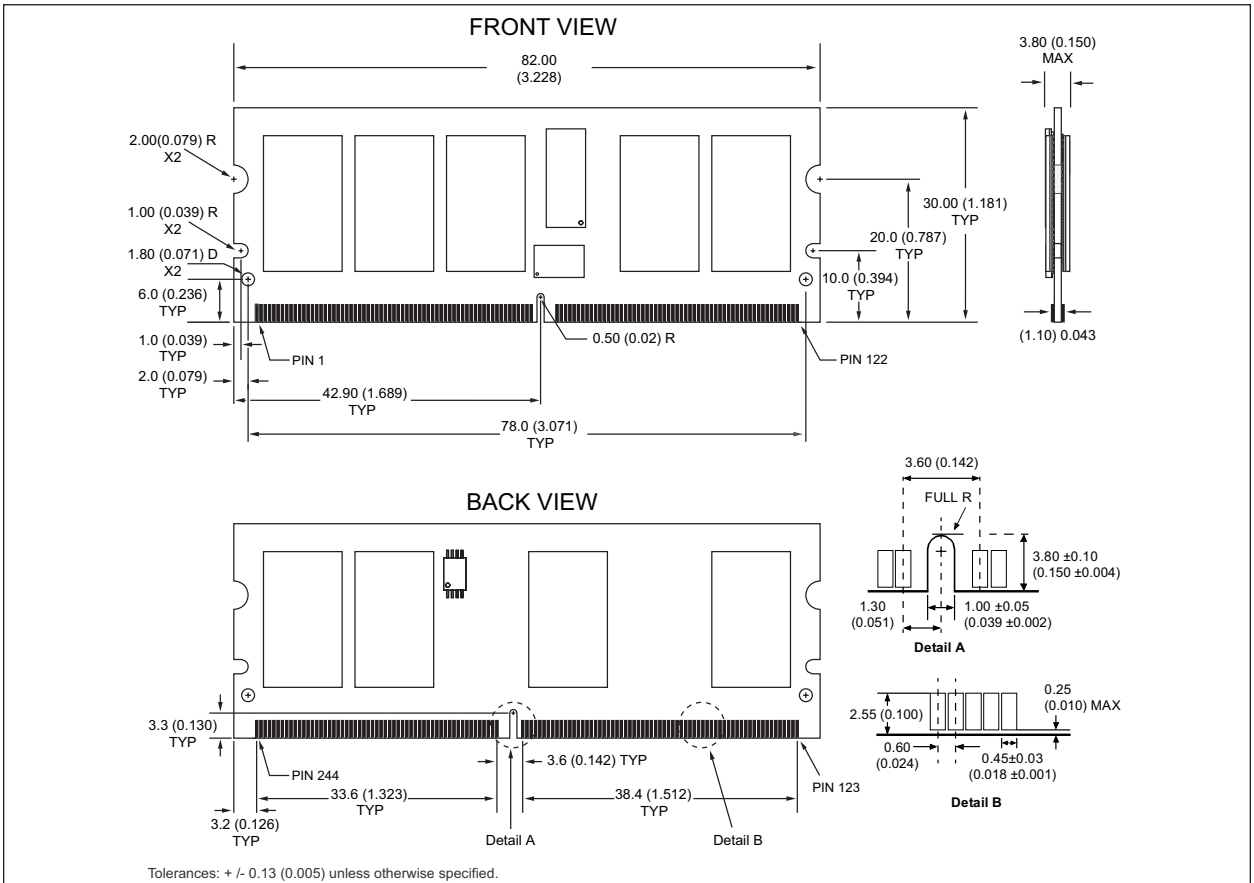
ORDERING INFORMATION FOR D7

Part Number	Clock Speed/ Data Rate	CAS Latency	t_{RCD}	t_{RP}	Height*
WV3HG64M72EER806D7xG	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG64M72EER665D7xG	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG64M72EER534D7xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG64M72EER403D7xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

NOTES:

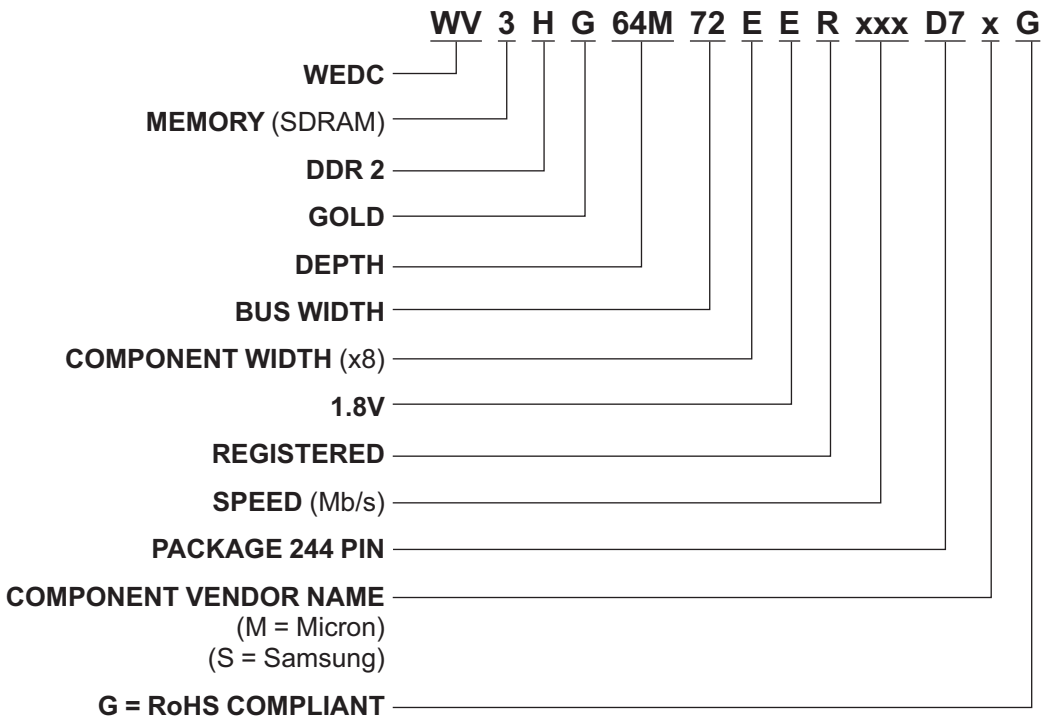
- Consult Factory for availability of RoHS products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D7



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL, Mini-DIMM

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	August 2005	Advanced
Rev 1	1.0 Updated CAP, I_{CC} and AC specs. 1.1 Changed from Advanced to Preliminary	September 2005	Preliminary
Rev 2	2.0 Update I_{CC} specs 2.1 Added DDR2-667 & DDR2-800 as TBD	February 2006	Preliminary