



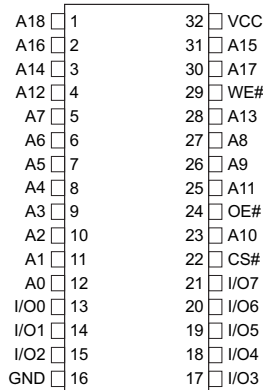
512Kx8 SRAM MODULE, SMD 5962-92078

FEATURES

- Access Times 20, 25, 35, 45ns
- Standard Microcircuit Drawing, 5962-92078
- MIL-STD-883 Compliant Devices Available
- Rad Tolerant Devices Available
- JEDEC Standard 32 pin, Hermetic Ceramic DIP (Package 300)
- Commercial, Industrial and Military Temperature Range (-55°C to +125°C)
- Organized as 512K x 8
- 5V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Battery Back-Up Operation

FIGURE 1 – PIN CONFIGURATION

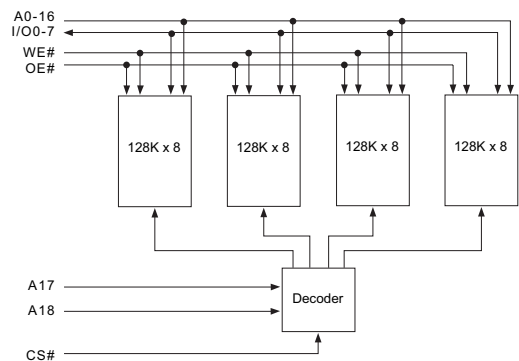
TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O 0-7	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0V Power
GND	Ground

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	45	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	45	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

Parameter	Symbol	Conditions	-20		-25		-35		-45		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10		10		10		10	μA
Operating Supply Current	I _{CC}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		210		210		210		210	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz		80		60		60		55	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4		2.4		2.4		2.4		V

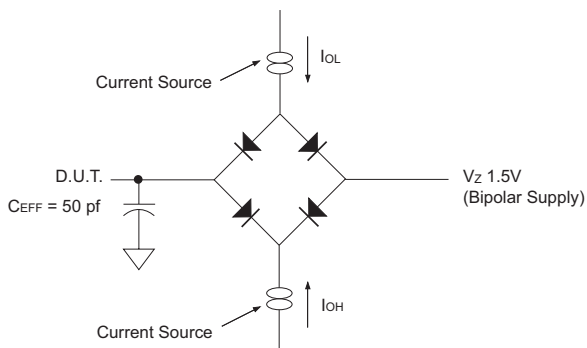
NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS FOR LOW POWER "L" VERSION

(-55°C ≤ T_A ≤ 125°C)

Parameter	Symbol	Conditions	-20			-25			-35			-45			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	CS# • V _{CC} - 0.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		8.0	12.8		8.0	12.8		8.0	12.8		8.0	12.8	mA

FIGURE 2 – AC TEST CIRCUIT

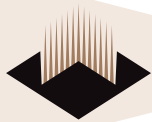


AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

Parameter Read Cycle	Symbol	-20		-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	20		25		35		45		ns
Address Access Time	t _{AA}		20		25		35		45	ns
Output Hold from Address Change	t _{OH}	3		3		3		3		ns
Chip Select Access Time	t _{ACS}		20		25		35		45	ns
Output Enable to Output Valid	t _{OE}		10		10		25		35	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		15		17		20		30	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12		15		20		25	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

Parameter Write Cycle	Symbol	-20		-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	20		25		35		45		ns
Chip Select to End of Write	t _{CW}	16		20		25		30		ns
Address Valid to End of Write	t _{AW}	16		20		25		30		ns
Data Valid to End of Write	t _{DW}	15		15		20		25		ns
Write Pulse Width	t _{WP}	16		20		25		30		ns
Address Setup Time	t _{AS}	2		2		2		2		ns
Address Hold Time	t _{AH}	2		2		2		2		ns
Output Active from End of Write	t _{OW} ¹	4		5		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		10	0	15	0	20	0	25	ns
Data Hold Time	t _{DH}	1		1		1		1		ns

1. This parameter is guaranteed by design but not tested.



FIGURE 3 – TIMING WAVEFORM - READ CYCLE

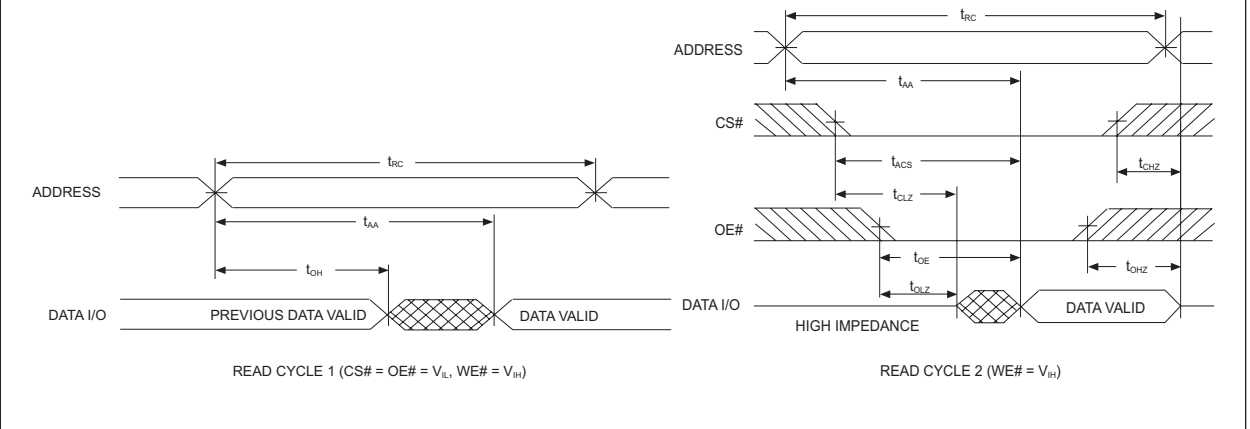


FIGURE 4 – WRITE CYCLE - WE# CONTROLLED

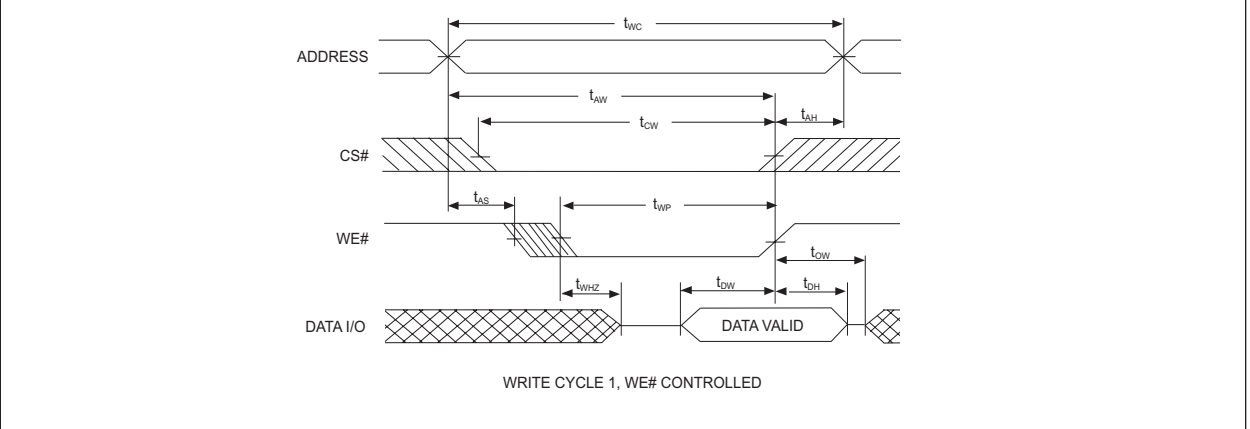
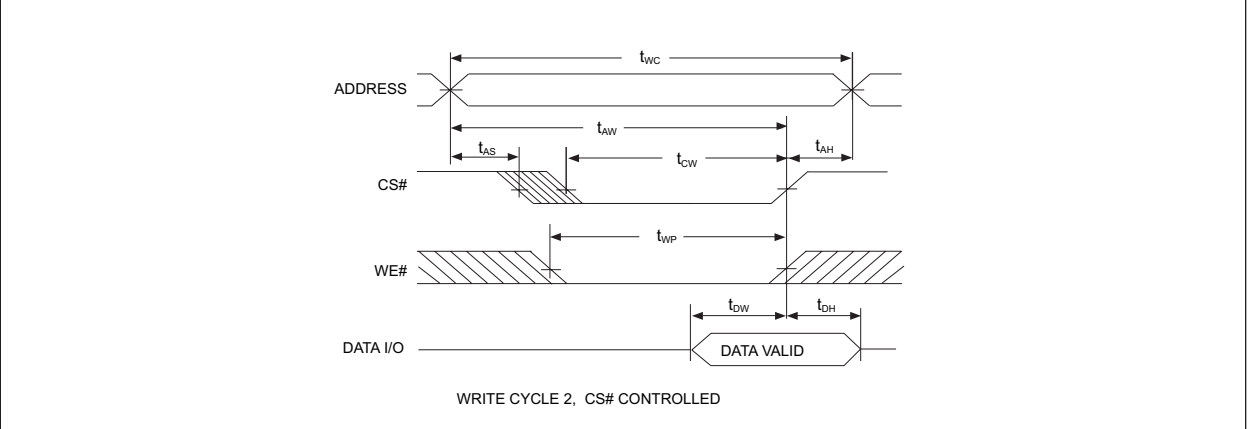
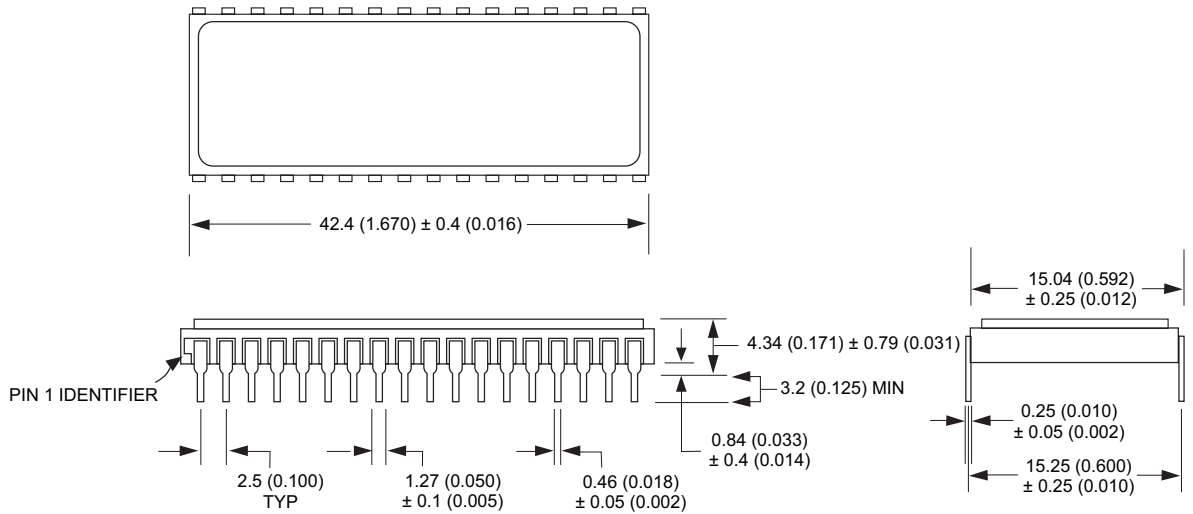


FIGURE 5 – WRITE CYCLE - CS# CONTROLLED





PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED

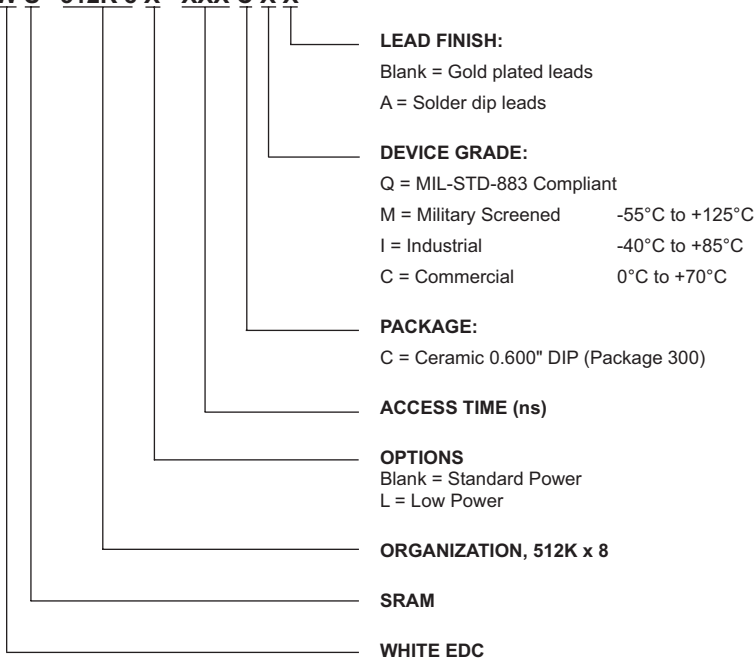


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 512K 8 X - XXX C X X



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 8 SRAM	45ns	32 pin DIP	5962-92078 06HTX
512K x 8 SRAM	35ns	32 pin DIP	5962-92078 07HTX
512K x 8 SRAM	25ns	32 pin DIP	5962-92078 08HTX
512K x 8 SRAM	20ns	32 pin DIP	5962-92078 09HTX