

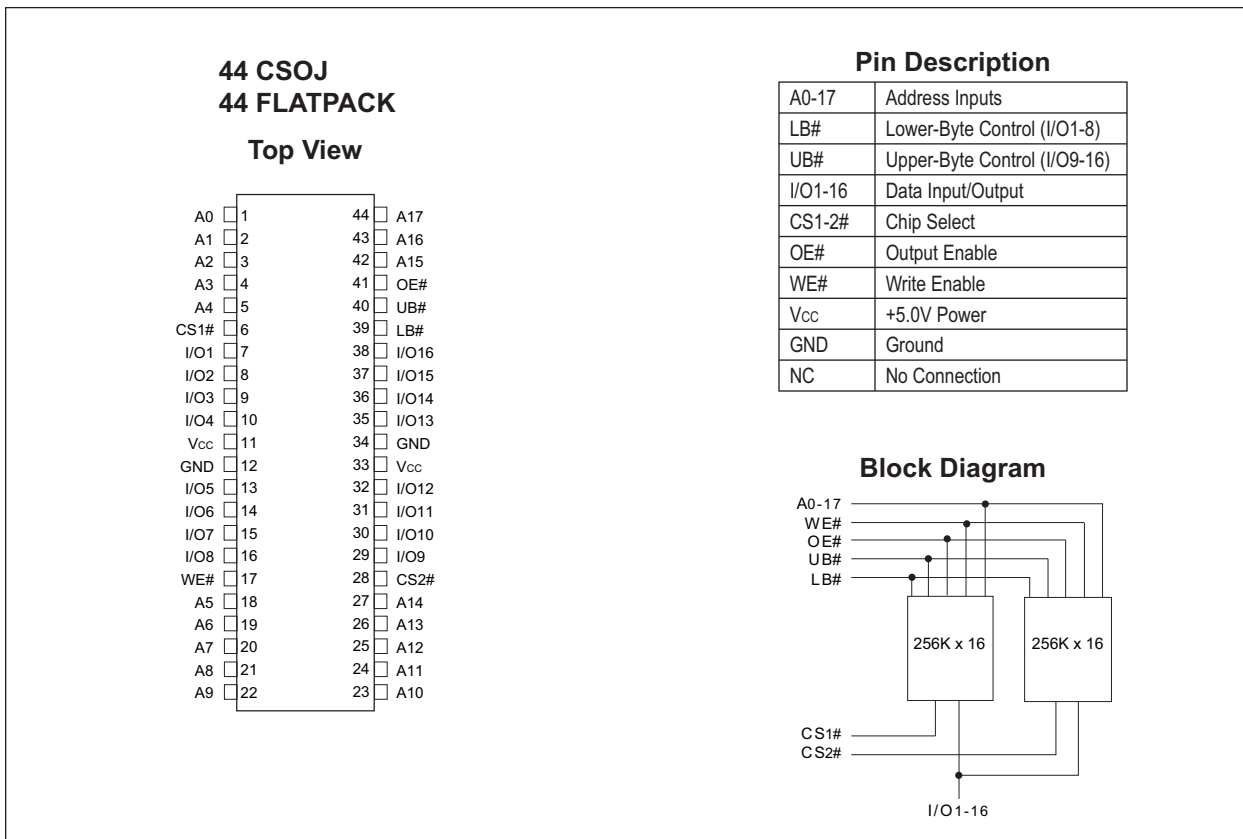
## 512Kx16 SRAM MODULE

### FEATURES

- Access Times 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 44 pin Ceramic SOJ (Package 102)
  - 44 lead Ceramic Flatpack (Package 209)
- Organized as two banks of 256Kx16
- Data Byte Control:
  - Lower Byte (LB#) = I/O1-8
  - Upper Byte (UB#) = I/O9-16
- Data I/O Compatible with 3.3V devices
- 2V Minimum Data Retention for battery back up operation
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply (3.3V parts also available)
- Low Power CMOS
- TTL Compatible Inputs and Outputs

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

### PIN CONFIGURATION FOR WS512K16-XXX





TRUTH TABLE

CS1#	CS2#	WE#	OE#	LB#	UB#	Mode	Data I/O		Power
H	H	X	X	X	X	Not Select	I/O1-8	I/O9-16	Standby
L	H	H	H	X	X	Output Disable	High Z	High Z	Active
H	L								
L	H	X	X	H	H				
H	L								
H	L	H	L	L	H	Read	Data Out	High Z	Active
L	H			H	L		High Z	Data Out	
L	L			L	L		Data Out	Data Out	
H	L	L	H	L	H	Write	Data In	High Z	Active
L	H			H	L		High Z	Data In	
L	L			L	L		Data In	Data In	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temp. (MIL)	T <sub>A</sub>	-55	+125	°C

CAPACITANCE

T<sub>A</sub> = +25°C

Parameter	Symbol	Conditions	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	25	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V, f = 1.0 MHz	25	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	µA
Operating Supply Current	I <sub>CC</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		290	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		30	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

DATA RETENTION CHARACTERISTICS

-55°C ≤ T<sub>A</sub> ≤ +125°C

Characteristic	Sym	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V <sub>DR</sub>	CS# ≥ V <sub>CC</sub> - 0.2V	2.0		5.5	µA
Data Retention Current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3V		2.0	12.0*	mA

\* Also available in Low Power version. Please call factory for information.



**AC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter Read Cycle	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	17		20		25		35		ns
Address Access Time	t <sub>AA</sub>		17		20		25		35	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		17		20		25		35	ns
Output Enable to Output Valid	t <sub>OE</sub>		10		12		15		20	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	2		5		5		5		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		9		10		12		15	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		9		10		12		15	ns
LB#, UB# Access Time	t <sub>BA</sub>		10		12		14		17	ns
LB#, UB# Enable to Low Z Output	t <sub>BLZ1</sub>	0		0		0		0		ns
LB#, UB# Disable to High Z Output	t <sub>BHZ1</sub>		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter Write Cycle	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	17		20		25		35		ns
Chip Select to End of Write	t <sub>CW</sub>	14		17		20		25		ns
Address Valid to End of Write	t <sub>AW</sub>	14		17		20		25		ns
Data Valid to End of Write	t <sub>DW</sub>	10		12		15		20		ns
Write Pulse Width	t <sub>WP</sub>	14		17		20		25		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	0		0		0		0		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		9		10		10		15	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		0		ns
LB#, UB# Valid to End of Write	t <sub>BW</sub>	14		17		20		25		ns

1. This parameter is guaranteed by design but not tested.

**AC TEST CIRCUIT**

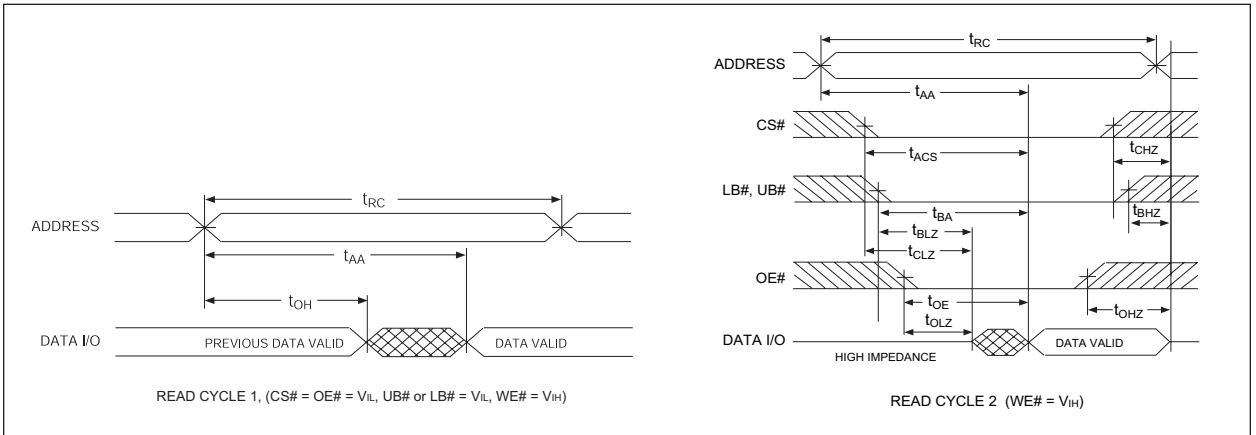
**AC Test Conditions**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

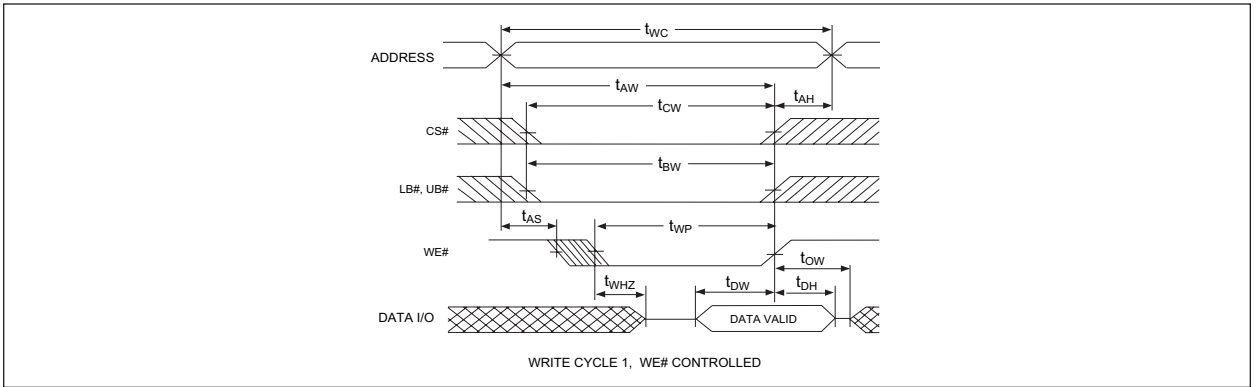
Notes:  
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



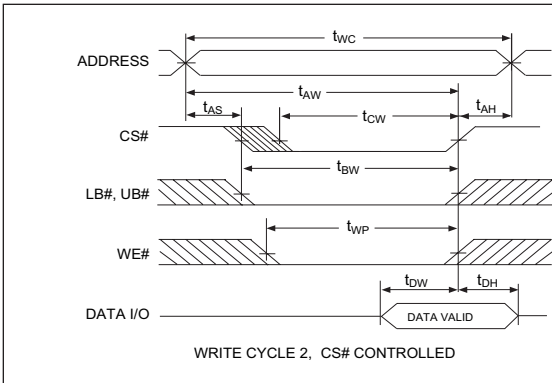
TIMING WAVEFORM – READ CYCLE



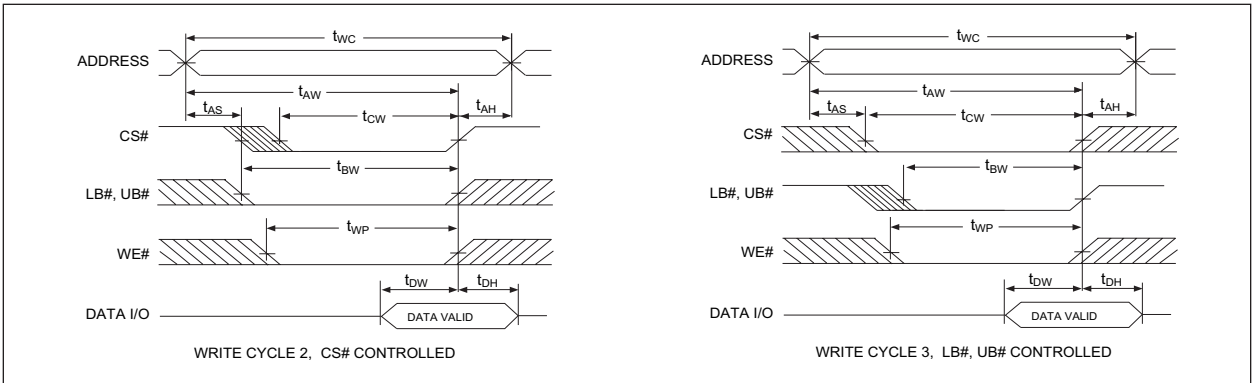
WRITE CYCLE – WE# CONTROLLED



WRITE CYCLE – CS# CONTROLLED

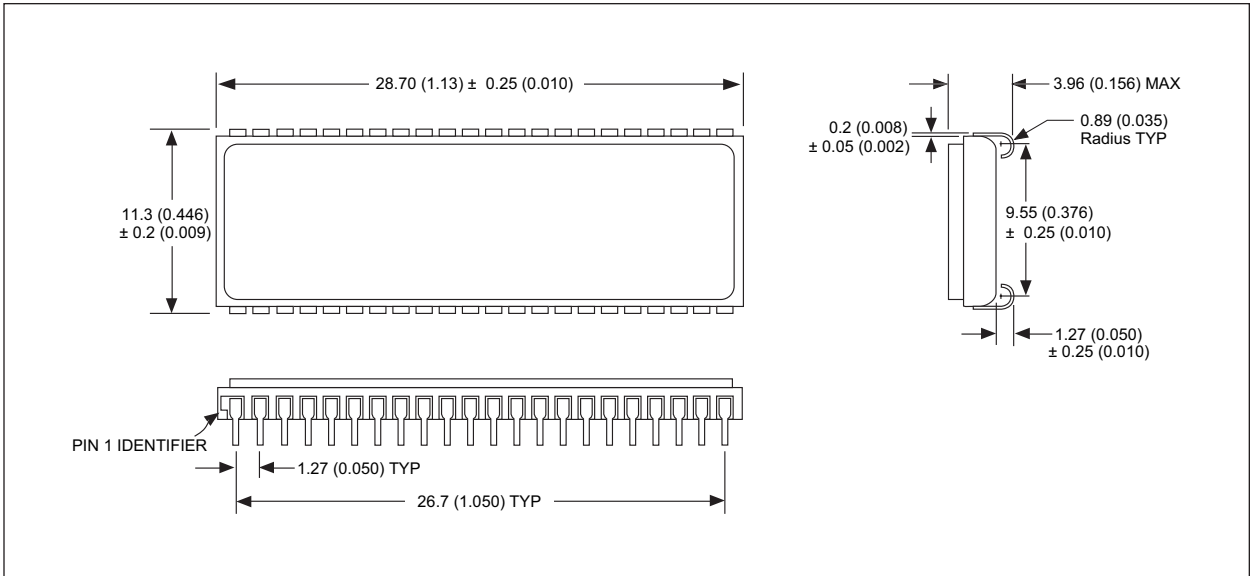


WRITE CYCLE – LB#, UB# CONTROLLED



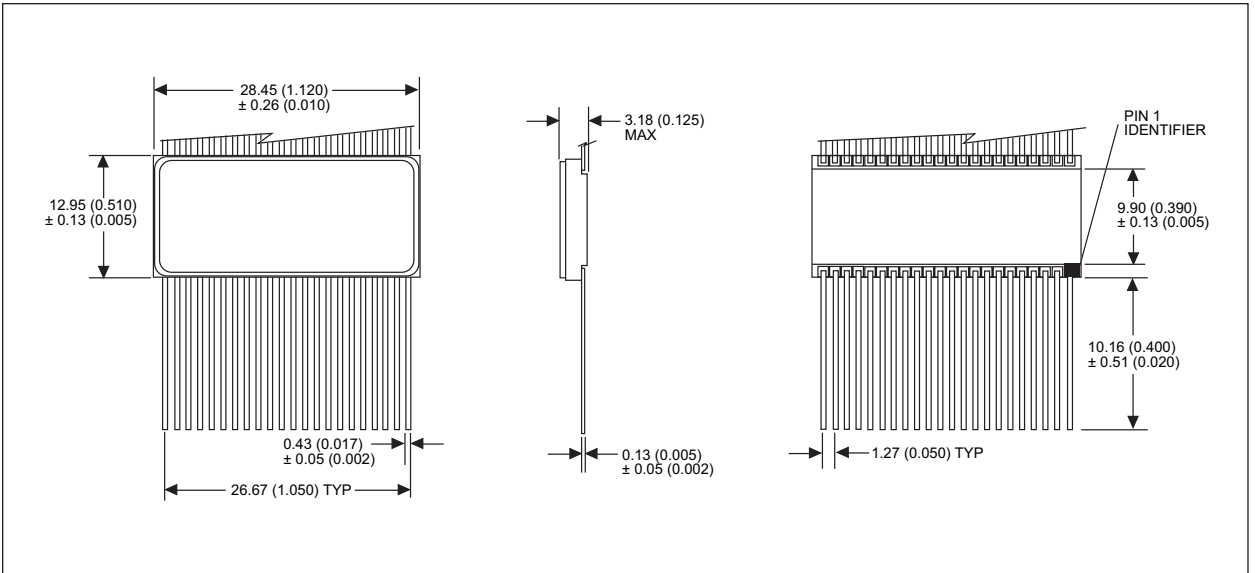


PACKAGE 102: 44 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 209: 44 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**

**W S 512K16 - XX X X X**

**LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

**DEVICE GRADE:**

M = Military Screened      -55°C to +125°C

I = Industrial                -40°C to +85°C

C = Commercial              0°C to +70°C

**PACKAGE TYPE:**

DL = 44 Lead Ceramic SOJ (Package 102)

FL = 44 Lead Ceramic Flatpack (Package 209)

**ACCESS TIME (ns)**

**ORGANIZATION, two banks of 256Kx16**

**SRAM**

**WHITE ELECTRONIC DESIGNS CORPORATION**