2Mx8 MONOLITHIC FLASH, SMD 5962-97609

FEATURES

- Access Times of 90, 120, 150ns
- Packaging:
  - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207). Fits standard 56 SSOP footprint.
  - 44 pin Ceramic LCC**
- Sector Architecture
  - 32 equal size sectors of 64KBytes each
  - Any combination of sectors can be erased. Also supports full chip erase.
- 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5V Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET# pin resets internal state machine to the read mode.
- Multiple Ground Pins for Low Noise Operation

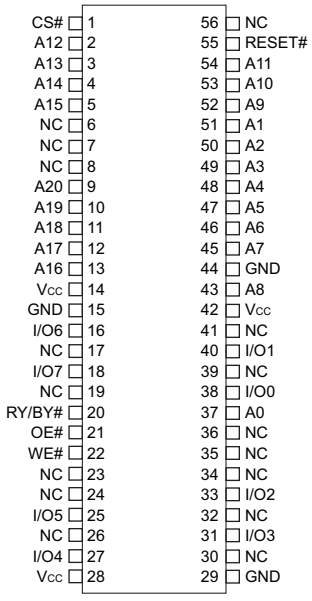
* This data sheet describes a product that is subject to change without notice.

** Package to be developed.

Note: For programming information refer to Flash Programming 16M5 Application Note.

Fig. 1 – Pin Configuration for WMF2M8-XXX5

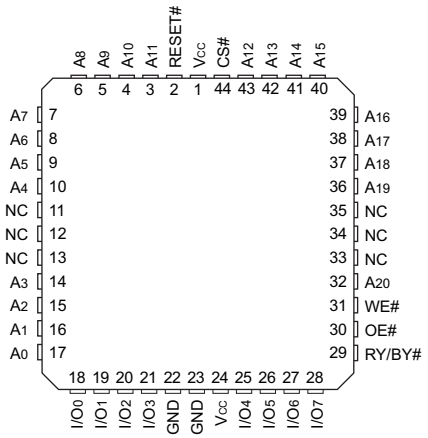
56 CSOP Top View



Pin Description

I/O0-7	Data Inputs/Outputs
A0-20	Address Inputs
WE#	Write Enable
CS#	Chip Select
OE#	Output Enable
VCC	Power Supply
GND	Ground
RY/BY#	Ready/Busy
RESET#	Reset

44 CLCC** Top View



** Package to be developed.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-2.0 to +7.0	V
Power Dissipation	P_T	8	W
Storage Temperature	T_{STG}	-65 to +125	°C
Short Circuit Output Current	I_{OS}	100	mA
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	CAD	$V_{I/O}$ = 0 V, f = 1.0MHz	12	pF
Output Enable capacitance	COE	V_{IN} = 0 V, f = 1.0MHz	12	pF
Write Enable capacitance	CWE	V_{IN} = 0 V, f = 1.0MHz	12	pF
Chip Select capacitance	CCS	V_{IN} = 0 V, f = 1.0MHz	12	pF
Data I/O capacitance	CI/O	$V_{I/O}$ = 0 V, f = 1.0MHz	12	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T_A	-55	-	+125	°C
Operating Temperature (Ind.)	T_A	-40	-	+85	°C

DC CHARACTERISTICS — CMOS COMPATIBLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz		40	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		60	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, CS# = V_{IH}, f = 5MHz, RESET# = Vcc ± 0.3V		2.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85xV_{CC}		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:
1. The Icc current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V_{IH}.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns
RESET# Pulse Width		t_{RP}	500		500		500		ns

NOTES:
1. Typical value for tWHWH1 is 7µs.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Read Cycle Time	t_{AVAV}	t_{RC}	90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		90		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Output Enable Hold Time	Read	t_{OEH}	0		0		0		ns
	Toggle & Data Polling		10		10		10		ns
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns
RESET# Low to Read Mode (1)		t_{Ready}		20		20		20	µs

1. Guaranteed by design, not tested.

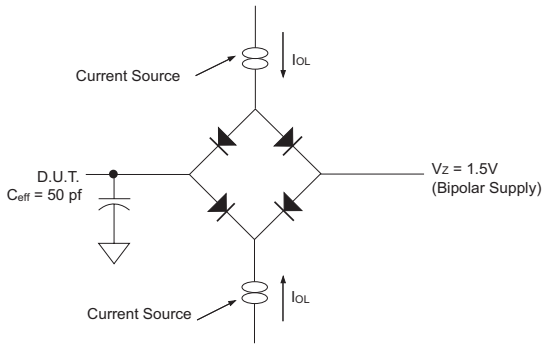
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT



AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

HARDWARE RESET (RESET#)

Parameter				
Std	Description	Test Setup	All Speed Options	Unit
t_{READY}	RESET Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	µs
t_{READY}	RESET Pin Low (Not During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
t_{RP}	RESET Pulse Width	Min	500	ns
t_{RH}	RESET High Time Before Read (See Note)	Min	50	ns
t_{RB}	RY/BY Recovery Time	Min	0	ns

FIGURE 3 – RESET# TIMING

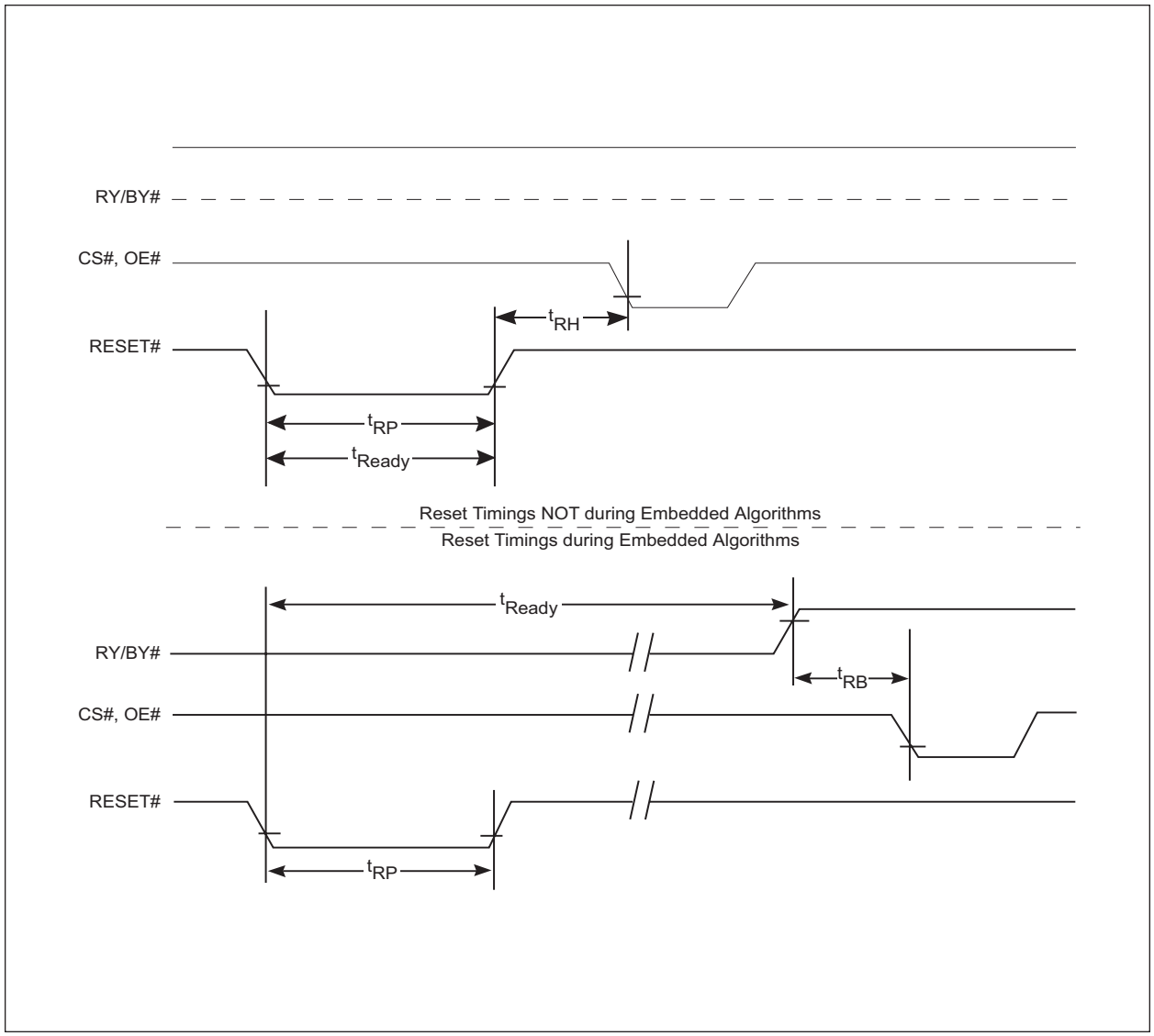


FIGURE 4 – AC WAVEFORMS FOR READ OPERATIONS

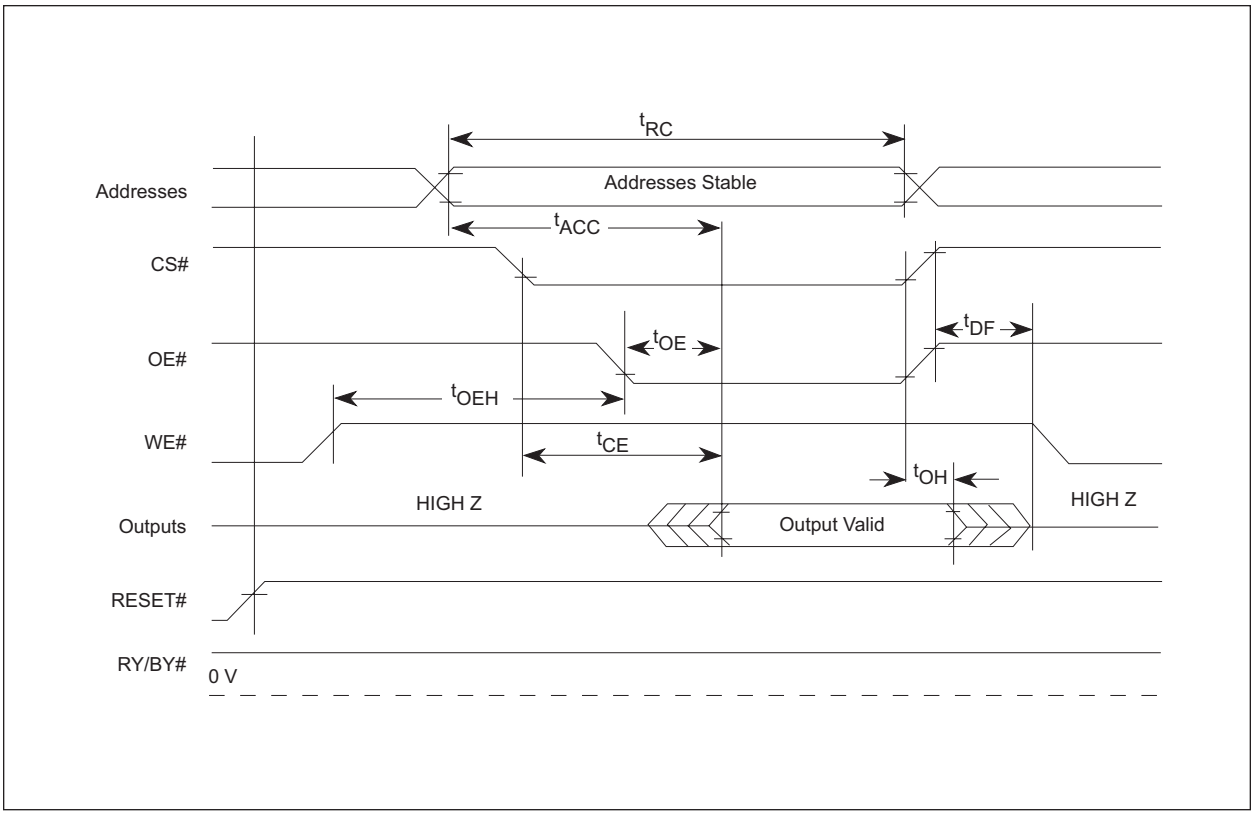
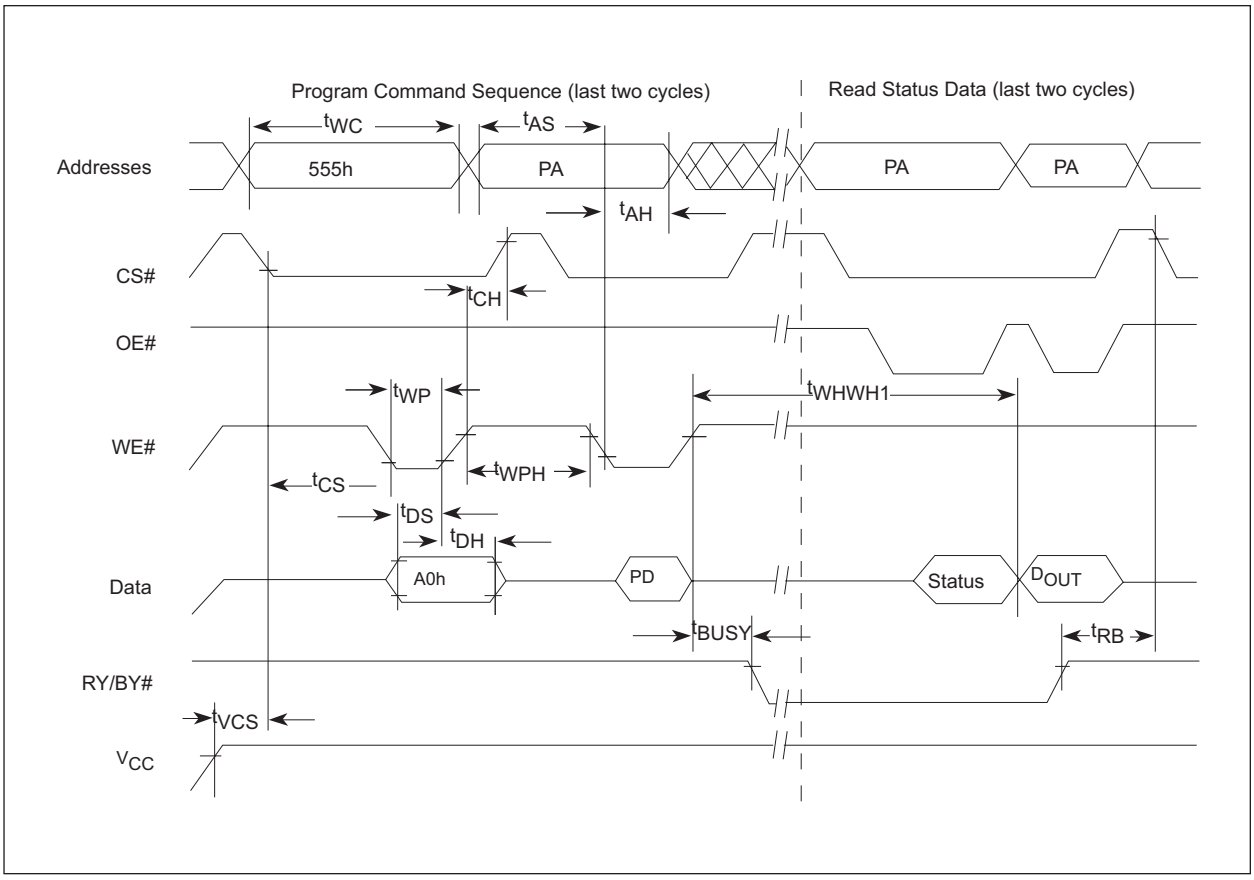
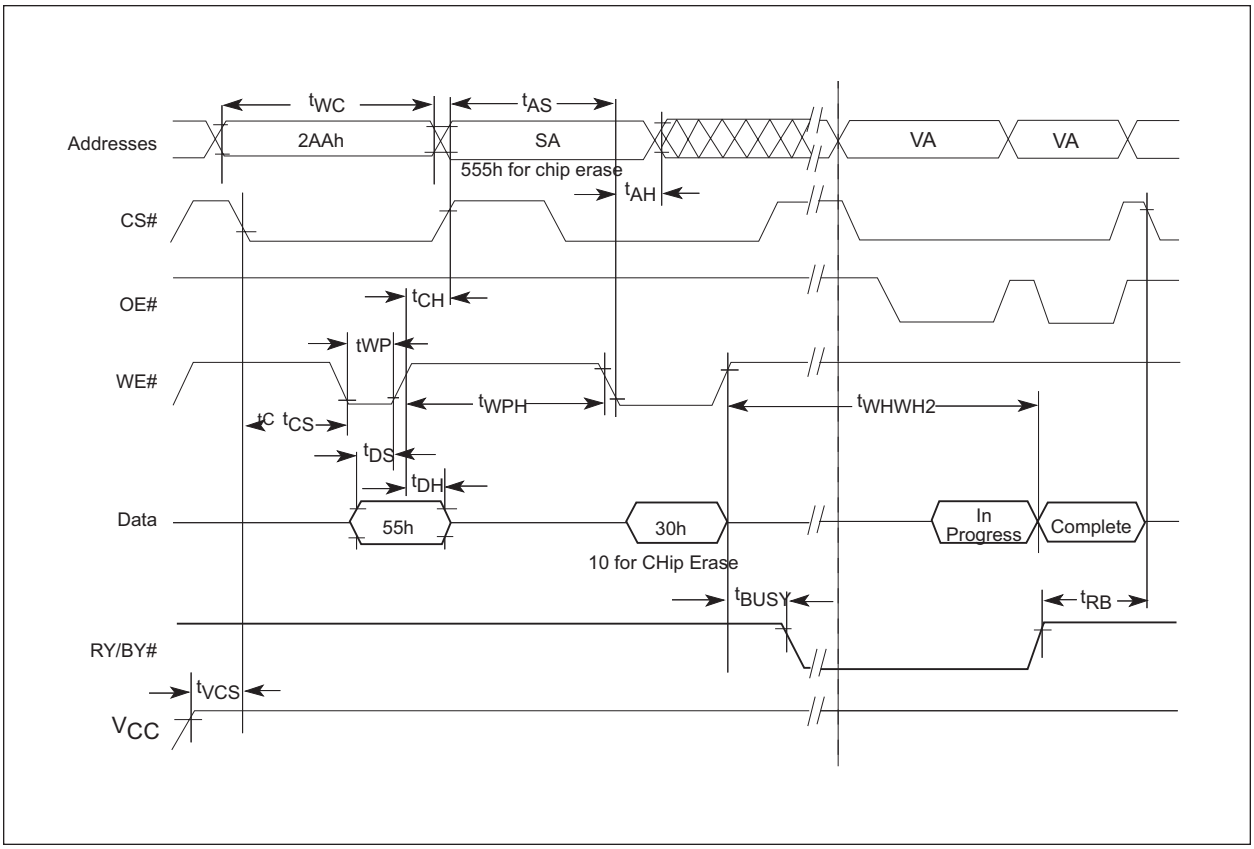


FIGURE 5 – WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



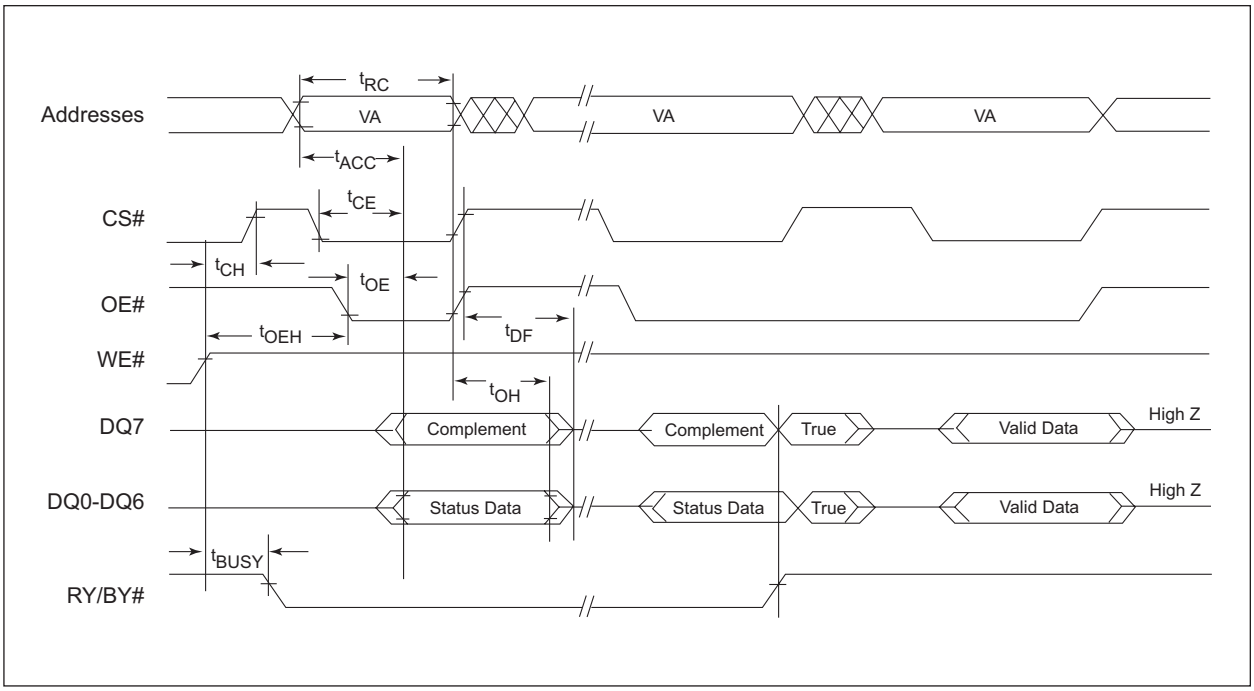
Notes:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of a four bus cycle sequence.

FIGURE 6 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



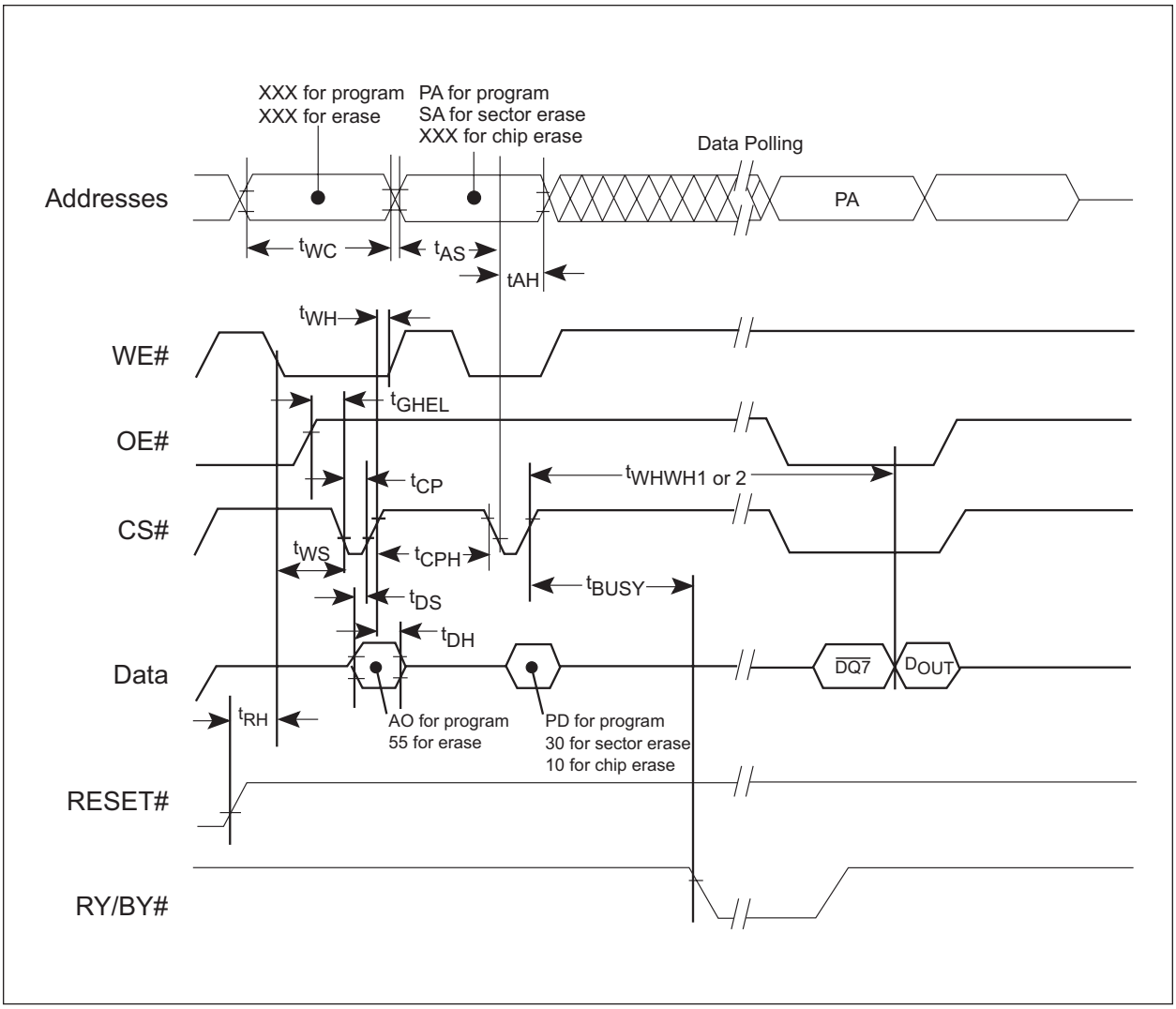
Notes: SA is the sector address for Sector Erase.

FIG. 7 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALIGORITHM OPERATIONS



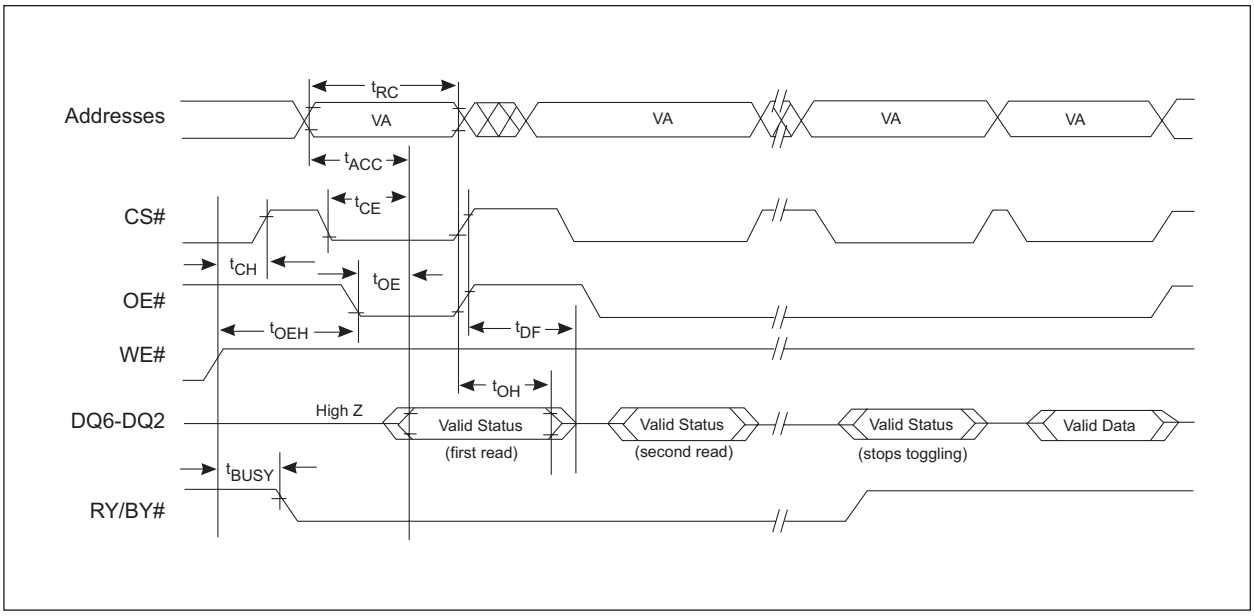
Notes: VA = Valid Address. Illustration shows first status cycle after command sequence, last status read cycle and array data read cycle.

FIGURE 8 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



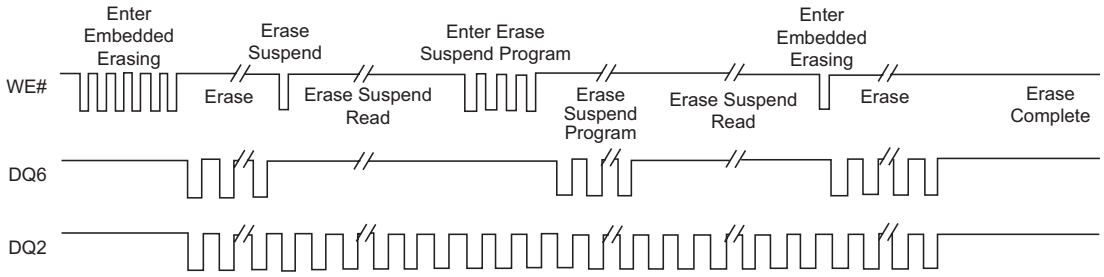
Notes:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of a four bus cycle sequence.

FIGURE 9 – TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



Notes:
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle and array data read cycle.

FIGURE 10 – DQ2 VS. DQ6



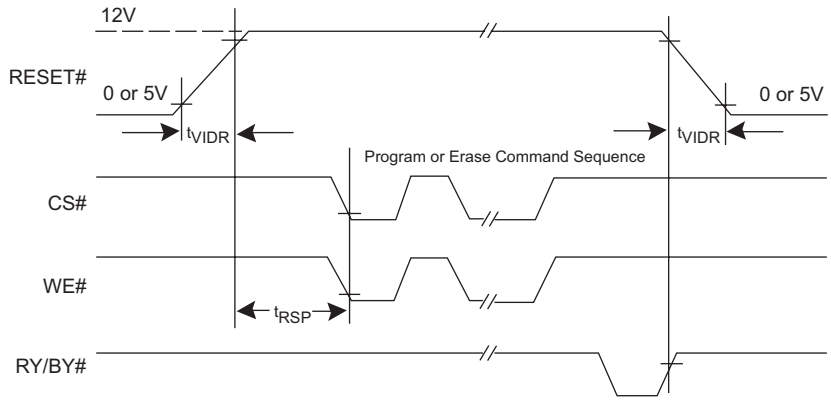
Note:
The system may use OE# or CS# to toggle DQ2 and DQ6. DQ6 toggles only when read at an address within the erase-suspended sector.

TEMPORARY SECTOR UNPROTECTED

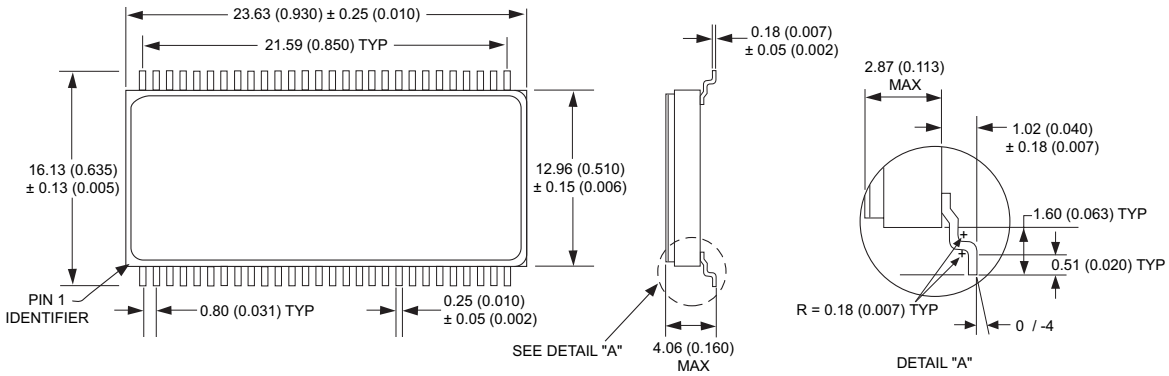
Parameter				
Std	**Description**		**All Speed Options**	**Unit**
t_{VIDR}	V_{ID} Rise and Fall time (see notes)	Min	500	ns
t_{RSP}	RESET# setup time for temporary sector unprotect	Min	4	ms

Note:
Not 100% tested.

FIGURE 11 – TEMPORARY SECTOR GROUP UNPROTECTED TIMINGS

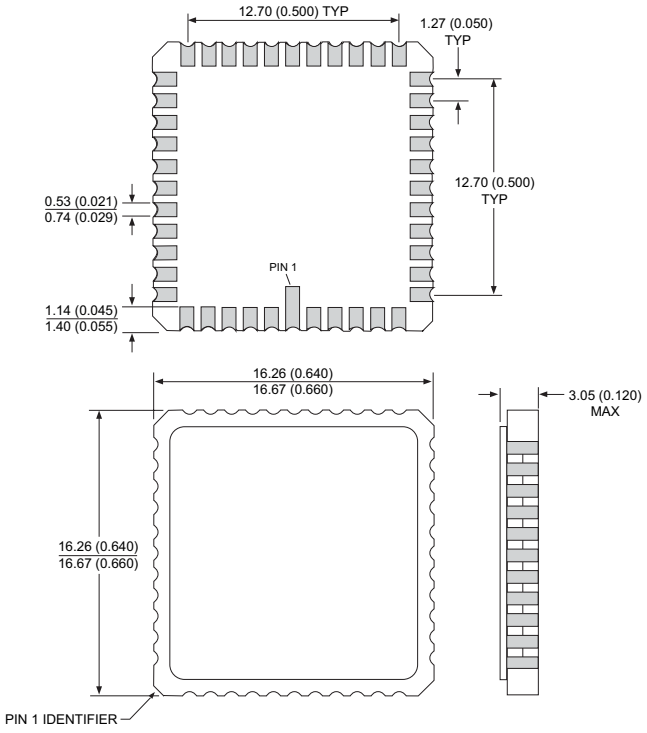


PACKAGE 207: 56 LEAD, CERAMIC SOP



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

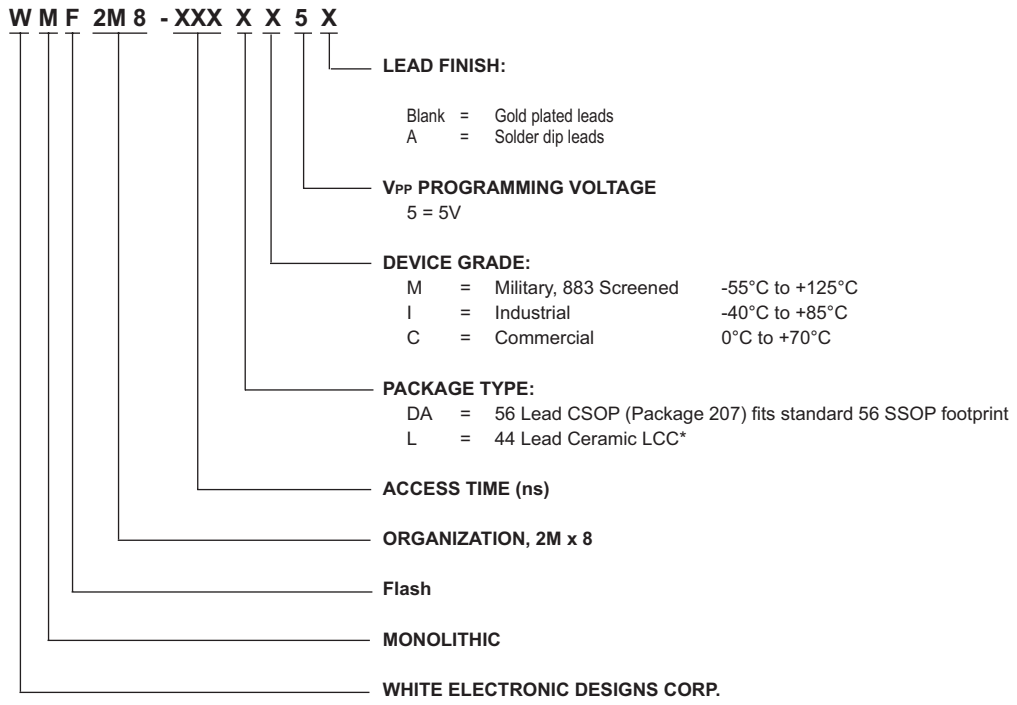
PACKAGE DIMENSION: 44 LEAD, CERAMIC LCC**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.

ORDERING INFORMATION



** Package to be developed.*

Device Type	Sector Size	Speed	Package	SMD No.
2M x 8 Flash Monolithic	64KByte	150ns	56 lead CSOP (DA)	5962-97609 01HXX
2M x 8 Flash Monolithic	64KByte	120ns	56 lead CSOP (DA)	5962-97609 02HXX
2M x 8 Flash Monolithic	64KByte	90ns	56 lead CSOP (DA)	5962-97609 03HXX