2Mx64 3.3V Simultaneous Operation Flash Multi-Chip Package

FEATURES

- Access Times of 90, 100, 120ns
- Packaging
  - 159 PBGA, 13x22mm - 1.27mm pitch
- 1,000,000 Erase/Program Cycles
- Sector Architecture
  - Bank 1 (4Mb): eight 4K word, eight 32K word
  - Bank 2 (12Mb): twenty-four 32K word
  - Bank 3 (12Mb): twenty-four 32K word
  - Bank 4 (4Mb): eight 32K word
- Bottom boot block
- Zero Power Operation
- Organized as 2Mx64 or 2x2Mx32
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Simultaneous Read/Write Operation:
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency between read and write operations
- Erase Suspend/Resume
  - Suspends erase operations to allow programming in same bank
- Data# Polling and Toggle Bits
  - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
  - Reduces overall programming time when issuing multiple program command sequences
- Ready/Busy# output (RY/BY#)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method of resetting the internal state machine to the read mode
- WP#/A_{CC} input pin
  - Write protect (WP#) function allows protection two outermost boot sectors, regardless of sector protect status
  - Acceleration (A_{CC}) function accelerates program timing
- Sector Protection
  - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

Note: For programming information refer to Flash Programming W72M64V-XBX Application Note.

This product is subject to change without notice.

FIGURE 1: PIN CONFIGURATION FOR W72M64V-XBX

Top View

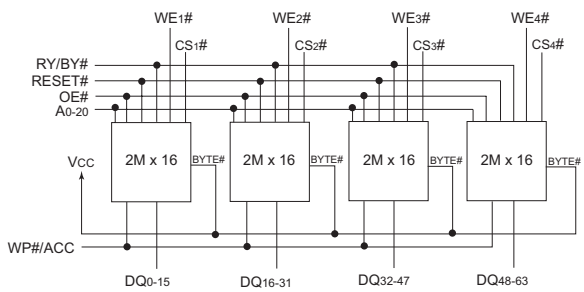
	1	2	3	4	5	6	7	8	9	10
A		GND	GND	GND	Vcc	Vcc	GND	GND	GND	Vcc
B	Vcc	GND	DQ41	WE3#	Vcc	DQ57	DNU	WE4#	Vcc	Vcc
C	Vcc	DQ33	DQ43	DQ45	DQ47	DQ49	DQ59	DQ61	DQ63	Vcc
D	Vcc	DQ40	DQ35	DQ37	DQ39	DQ56	DQ51	DQ53	DQ55	Vcc
E	Vcc	DQ32	DQ42	DQ44	DQ46	DQ48	DQ58	DQ60	DQ62	Vcc
F	GND	CS3#	DQ34	DQ36	DQ38	CS4#	DQ50	DQ52	DQ54	GND
G	GND	OE#	A0	DNU*	Vcc	A12	A16	DNU*	A20	GND
H	GND	A2	WP#/Acc	A11	GND	Vcc	A7	A10	A15	GND*
J	GND	A3	A6	A9	Vcc	GND	A1	RESET#	A13	GND
K	GND	A4	A17	RY/BY#	GND	A14	A5	A18	A8	GND
L	GND	DQ17	WE2#	DQ29	DNU	DQ9	DQ4	WE1#	A19	GND
M	Vcc	DQ24	DQ19	DQ21	DQ31	DQ1	DQ11	DQ6	DQ15	Vcc
N	Vcc	DQ16	DQ26	DQ28	DQ23	DQ8	DQ3	DQ13	DQ7	Vcc
P	Vcc	CS2#	DQ18	DQ20	DQ30	DQ0	DQ10	DQ5	DQ14	Vcc
R	Vcc	Vcc	DQ25	DQ27	DQ22	CS1#	DQ2	DQ12	GND	Vcc
T	Vcc	GND	GND	GND	Vcc	Vcc	GND	GND	GND	Vcc

* Ball G8 is reserved for A_{21} and ball G4 is reserved for A_{22} on W78M64V-XSBX.

Pin Description

DQ0-63	Data Inputs/Outputs
A0-20	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
RESET#	Hardware Reset
WP#/ACC	Hardware Write Protect/Acceleration
RY/BY#	Ready/Busy Output
Vcc	Power Supply
GND	Ground
DNU	Do Not Use

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to Vcc +0.5	V
Storage Temperature Range	-55 to +150	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

CAPACITANCE

T_A = +25°C, F = 1.0MHz

Parameter	Symbol	Max	Unit
WE1-4# capacitance	C_{WE}	8	pF
CS1-4# capacitance	C_{CS}	8	pF
Data I/O capacitance	$C_{I/O}$	10	pF
Address input capacitance	C_{AD}	30	pF
RESET# capacitance	C_{RS}	26	pF
RY/BY# capacitance	C_{RB}	26	pF
OE# capacitance	C_{OE}	32	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS – CMOS COMPATIBLE

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 3.6V, V_{IN} = GND to V_{CC}		-10	10	µA
Output Leakage Current	I_{LO}	V_{CC} = 3.6V, V_{OUT} = GND to V_{CC}		-10	10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}#, OE = V_{IH}, f = 5MHz			65	mA
V_{CC} Active Current for Program or Erase (2,3)	I_{CC2}	CS# = V_{IL}#, OE = V_{IH}, WE# = V_{IL}			120	mA
V_{CC} Standby Current (2)	I_{CC3}	CS# = RESET# = V_{CC} ± 0.3V			400	µA
Automatic Sleep Mode (2,4,5)	I_{CC5}	V_{IH} = V_{CC} ± 0.3V; V_{IL} = V_{SS} ± 0.3V			400	µA
V_{CC} Active Read-While-Program Current (1,2)	I_{CC6}	CS# = V_{IL}#, OE = V_{IH}			180	mA
V_{CC} Active Program-While-Erase Current (1,2)	I_{CC7}	CS# = V_{IL}#, OE = V_{IH}			180	mA
V_{CC} Active Program-While-Erase-Suspended Current (2,5)	I_{CC8}	CS# = V_{IL}#, OE = V_{IH}			140	mA
A_{CC} Accelerated Program Current	I_{ACC}	CS# = V_{IL}#, OE = V_{IH}	ACC Pin		40	mA
			VCC Pin		120	
Input Low Voltage	V_{IL}			-0.5	0.8	V
Input High Voltage	V_{IH}	V_{CC} = min		2.1	V_{CC} + 0.3	V
Voltage for WP#/A_{CC} Sector Protect/Unprotect and Program Acceleration	V_{HH}	V_{CC} = 3.0V + 0.3V		8.5	9.5	V
Voltage for Autoselect and Temporary Sector Unprotect	V_{ID}	V_{CC} = 3.0V + 0.3V		8.5	12.5	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA, V_{CC} = 3.0V			0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{CC} = 3.0V		2.55		V
Low V_{CC} Lock-Out Voltage (5)	V_{LKO}			2.3	2.5	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with OE# at V_{IH}.
2. Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} MAX
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns.
5. Not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – CS# CONTROLLED

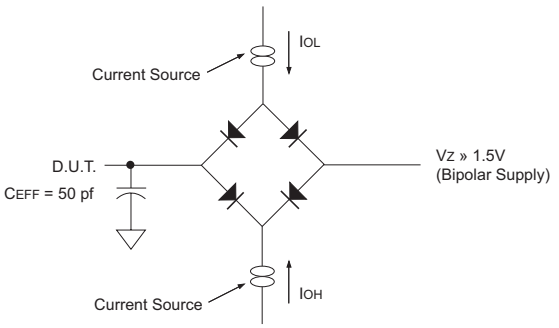
V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-100 Min	-100 Max	-120 Min	-120 Max	Unit
Write Cycle Time (3)	t_{AVAV}	t_{WC}	90		100		120		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	35		45		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		45		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		50		ns
Chip Select Pulse Width High (3)	t_{EHEL}	t_{CPH}	30		30		30		ns
Duration of Word Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			5		5		5	sec
Read Recovery Time Before Write (3)	t_{GHEL}		0		0		0		ns
Chip Programming Time (4)				42		42		42	sec

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 0.4 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

FIGURE 2

AC Test Circuit



AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75W.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90		-100		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (3)	t_{AVAV}	t_{WC}	90		100		120		ns
Chip Select Setup Time (3)	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	35		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High (3)	t_{WHWL}	t_{WPH}	30		30		30		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase (2)	t_{WHWH2}			5		5		5	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		0		ns
VCC Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time (4)				42		42		42	sec
Address Setup Time to OE# low during toggle bit polling		t_{ASO}	15		15		15		ns
Write Recovery Time from RY/BY# (3)		t_{RB}	0		0		0		ns
Program/Erase Valid to RY/BY#		t_{BUSY}	90		90		90		ns

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 0.4 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

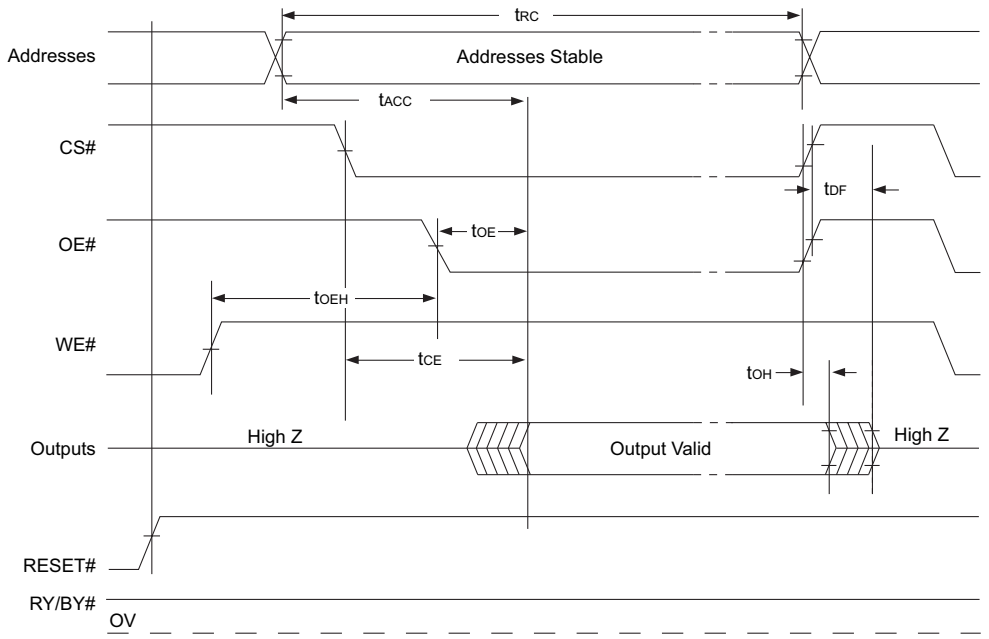
AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter		Symbol		-90		-100		-120		Unit
				Min	Max	Min	Max	Min	Max	
Read Cycle Time (1)		t_{AVAV}	t_{RC}	90		100		120		ns
Address Access Time		t_{AVQV}	t_{ACC}		90		100		120	ns
Chip Select Access Time		t_{ELQV}	t_{CE}		90		100		120	ns
Output Enable to Output Valid		t_{GLQV}	t_{OE}		40		40		50	ns
Chip Select High to Output High Z		t_{EHQZ}	t_{DF}		20		20		20	ns
Output Enable High to Output High Z		t_{GHQZ}	t_{DF}		20		20		20	ns
Output Hold from Addresses, CS# or OE# Change, Whichever occurs first		t_{AXQX}	t_{OH}	0		0		0		ns
Output Enable Hold Time (1)	Read		t_{OEH}	0		0		0		
	Toggle and Data# Polling			10		10		10		

1. Guaranteed by design, not tested.

FIGURE 3: AC WAVEFORMS FOR READ OPERATIONS



AC CHARACTERISTICS – HARDWARE RESET (RESET#)

Parameter	Symbol	-90 Min	-90 Max	-100 Min	-100 Max	-120 Min	-120 Max	Unit
RESET# Pin Low (During Embedded Algorithms) to Read Mode (1)	t_{ready}		20		20		20	µs
RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (1)	t_{ready}		500		500		500	ns
RESET# Pulse Width	t_{RP}	500		500		500		ns
RESET# High Time Before Read (1)	t_{RH}	50		50		50		ns
RESET# Low to Standby Mode (1)	t_{RPD}	20		20		20		µs

NOTE: 1. Not tested.

FIGURE 4: RESET TIMINGS NOT DURING EMBEDDED ALGORITHMS

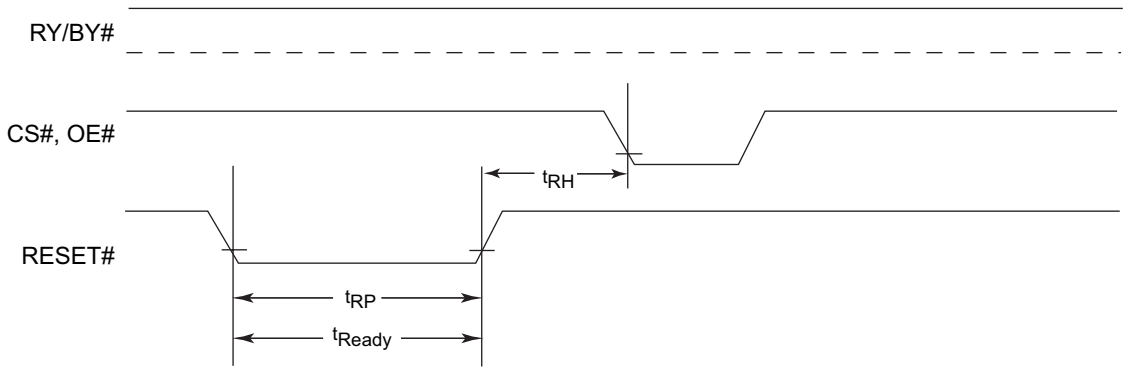


FIGURE 5: RESET TIMINGS DURING EMBEDDED ALGORITHMS

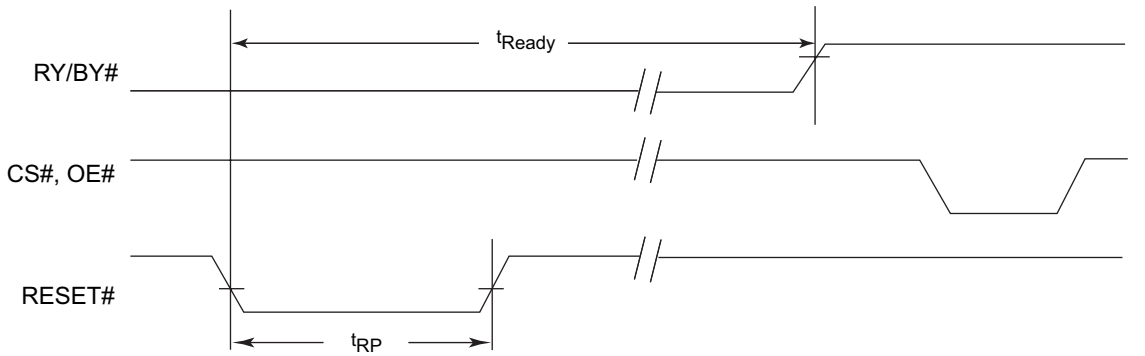
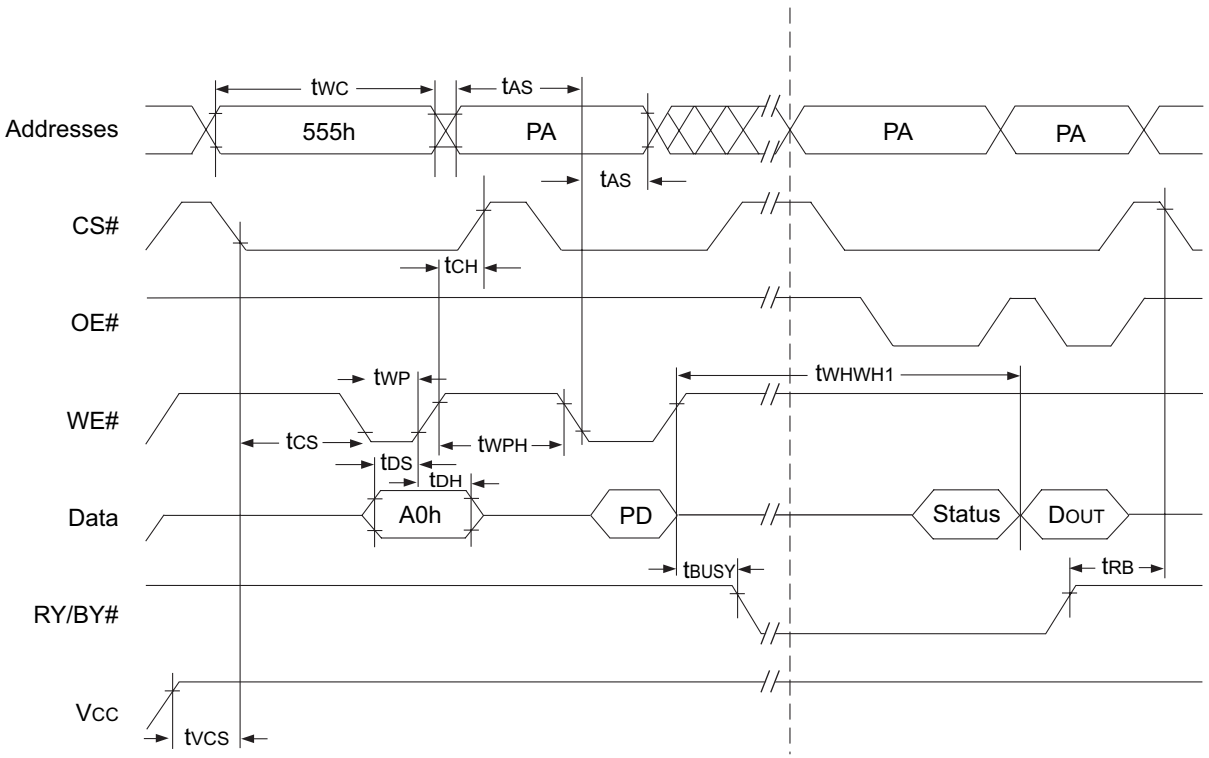


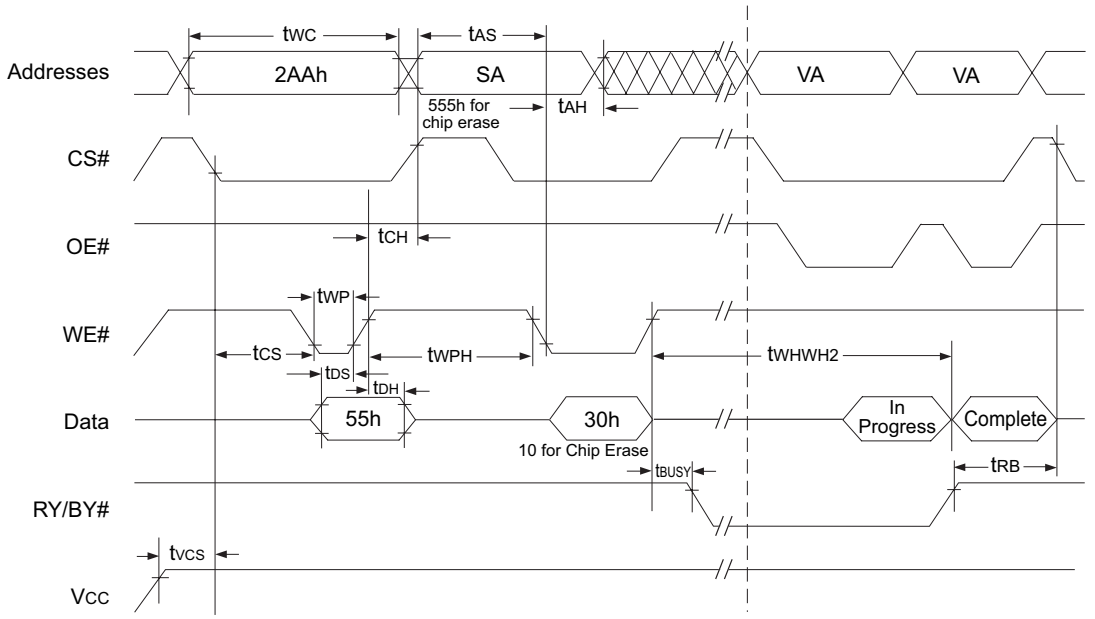
FIGURE 6: PROGRAM OPERATIONS



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. DOUT is the output of the data written to the device.
4. Figure indicates last two bus cycles of four bus cycle sequence.

FIGURE 7: ACCELERATED PROGRAM TIMING DIAGRAM

FIGURE 8: CHIP/SECTOR ERASE OPERATION TIMINGS



NOTES: 1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data

FIGURE 9: BACK TO BACK READ/WRITE CYCLE TIMINGS

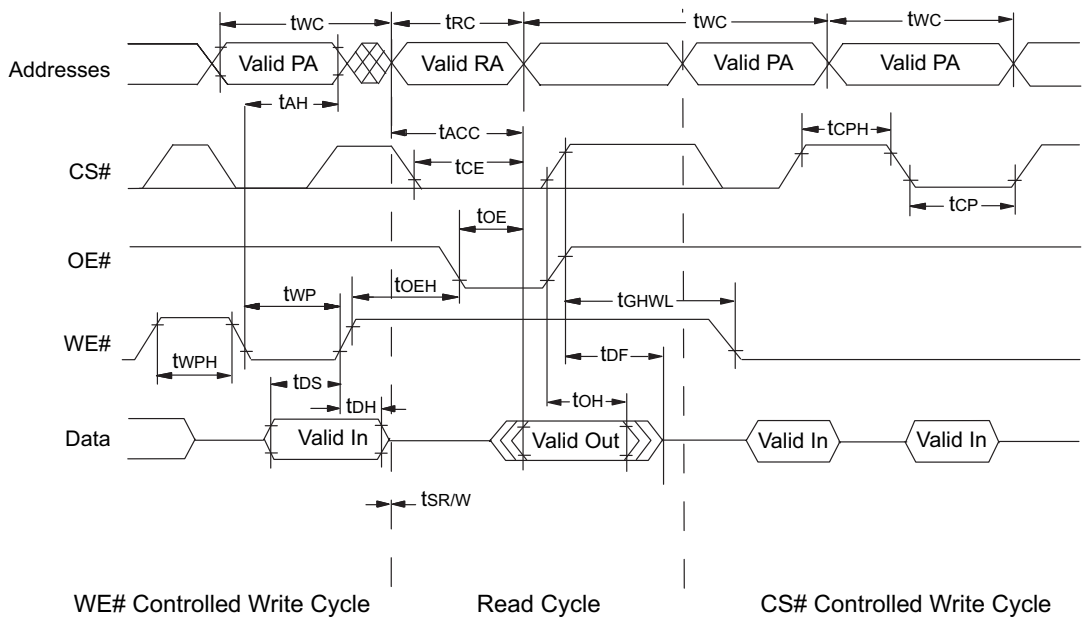
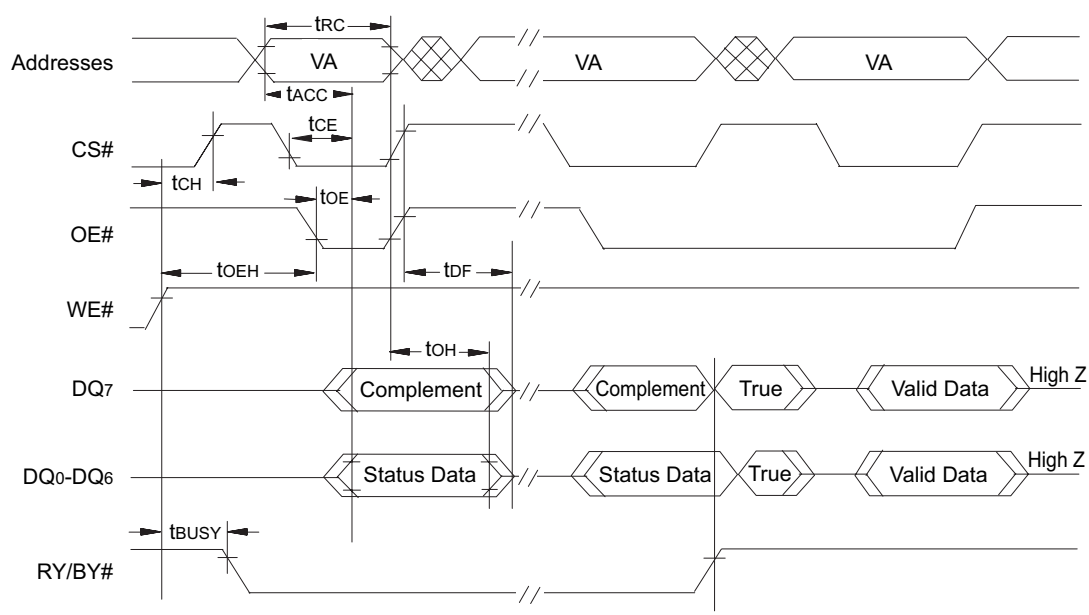
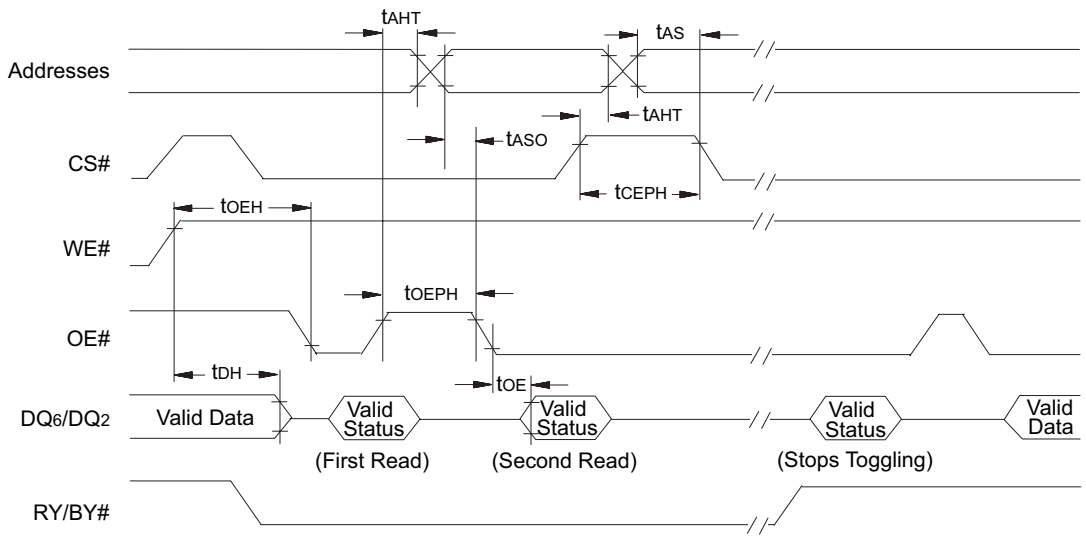


FIGURE 10: DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



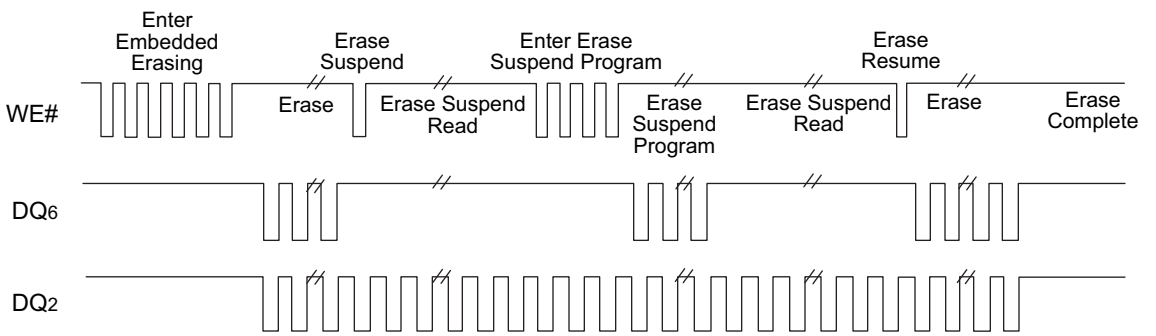
NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

FIGURE 11: TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



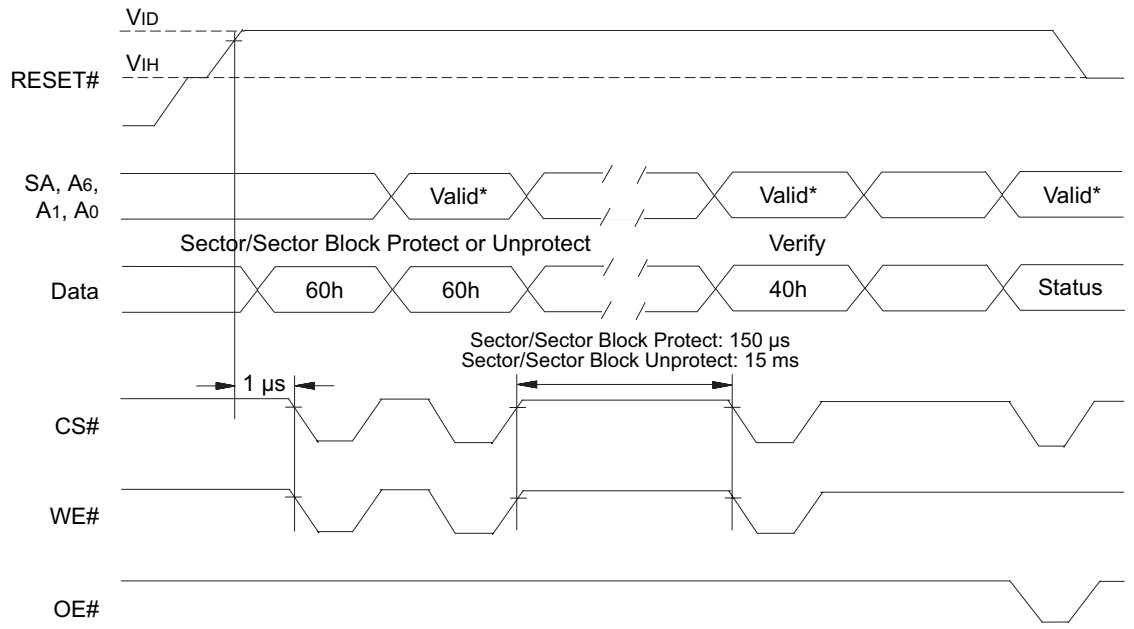
NOTE: VA = Valid address, not required for DQ_6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

FIGURE 12: DQ2 Vs. DQ6



NOTE: DQ_2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CS# to toggle DQ_2 and DQ_6.

FIGURE 13: SECTOR/SECTOR BLOCK PROTECT AND UNPROTECT TIMING DIAGRAM



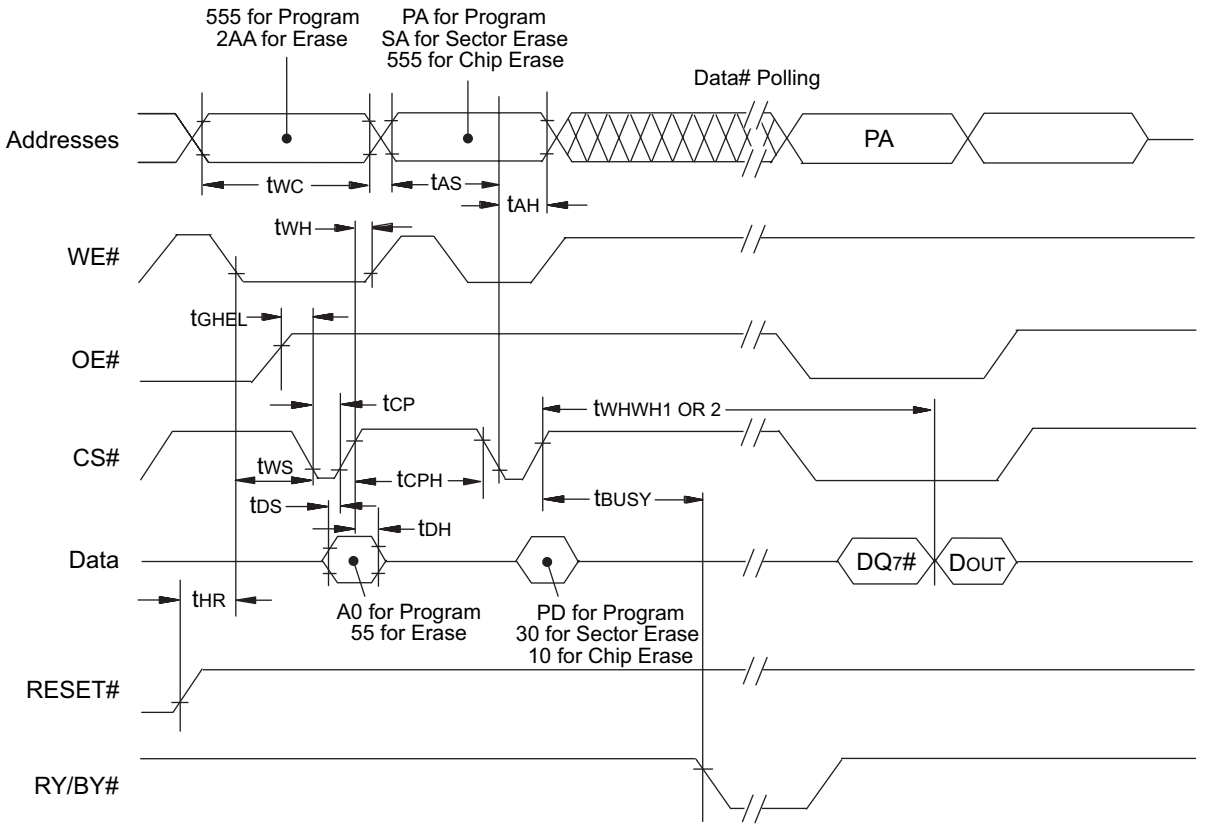
NOTE: VA = Valid address, not required for DQ_6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

AC CHARACTERISTICS – ALTERNATE CS# CONTROLLED ERASE AND PROGRAM OPERATIONS

Parameter				Speed Options			
JEDEC	Std	Description		90	100	120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (1)	Min	90	100	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	45	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	0	0	ns
t_{WLEL}	T_{WS}	WE# Setup Time	Min	0	0	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	0	0	ns
t_{ELEH}	t_{CP}	CS# Pulse Width	Min	35	45	50	ns
t_{EHEL}	t_{CPH}	CS# Pulse Width High	Min	30	30	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Typ	7	7	7	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation	Typ	4	4	4	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Typ	0.4	0.4	0.4	sec

NOTE: 1. Not tested.

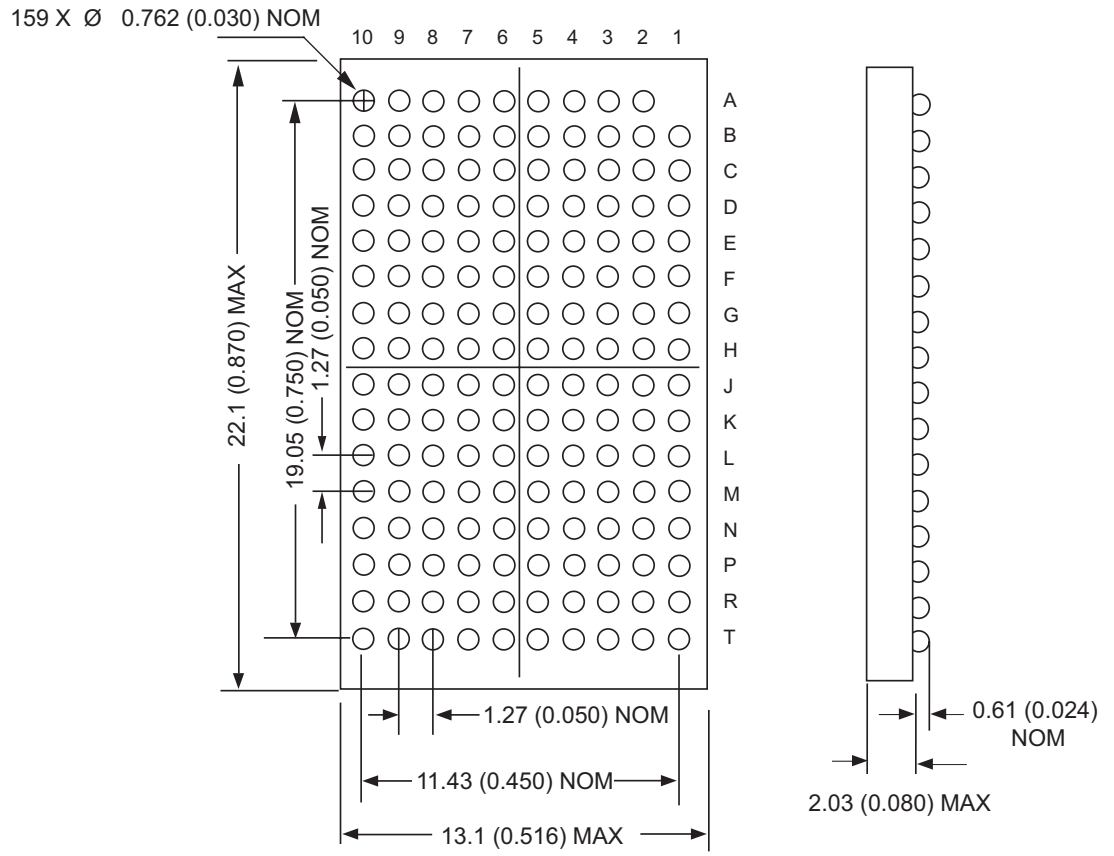
FIGURE 14: ALTERNATE CS# CONTROLLED WRITE (ERASE/PROGRAM) OPERATION TIMINGS



NOTES:
1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. DQ7 is the complement of the data written to the device. D_{OUT} is the data written to the device.

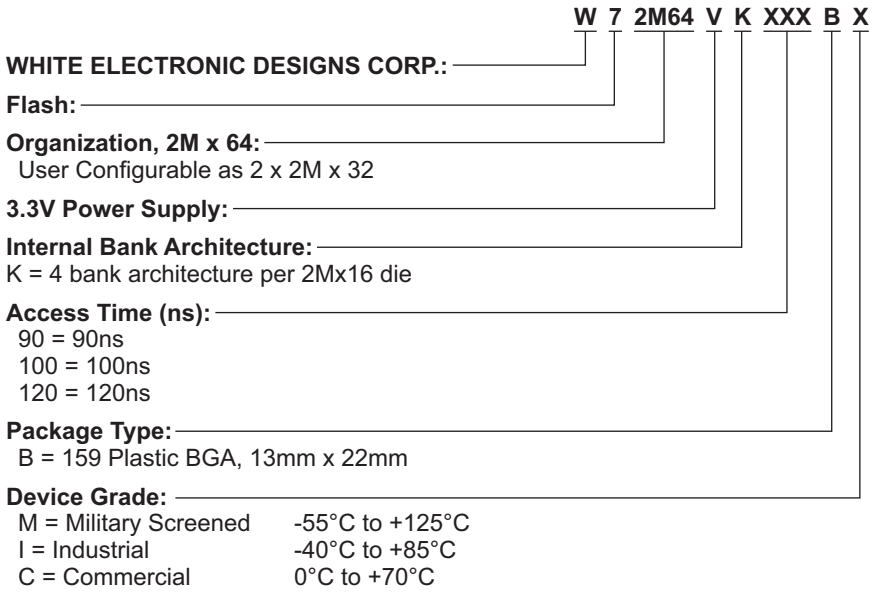
PACKAGE: 159 PBGA

Bottom View



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

PACKAGE: 159 PBGA



Document Title

2M x 64 Simultaneous Operation Flash Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	April 2005	Final