1GB – 128Mx72 DDR SDRAM UNBUFFERED ECC w/PLL

FEATURES

- Double-data-rate architecture
- DDR200, DDR266, DDR333 and DDR400
  - JEDEC design specification
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Power supply:
  - V_{CC} = V_{CCQ} = +2.5V ± 0.2V (100, 133 and 166MHz)
  - V_{CC} = V_{CCQ} = +2.6V ± 0.1V (200MHz)
- JEDEC standard 184 pin DIMM package
  - Package height options:
    JD3: 30.48 mm (1.20")
    AJD3: 28.70 mm (1.13")

NOTE: Consult factory for availability of:
- Lead-free products
- Vendor source control option
- Industrial temperature option

DESCRIPTION

The W3EG128M72ETSU is a 128Mx72 Double Data Rate SDRAM memory module based on 1Gb DDR SDRAM components. The module consists of nine 128Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	DDR400@CL=3	DDR333@CL=2.5	DDR266@CL=2	DDR266@CL=2.5	DDR200@CL=2
Clock Speed	200MHz	166MHz	133MHz	133MHz	100MHz
CL-t_{RCD}-t_{RP}	3-3-3	2.5-3-3	2-2-2	2.5-3-3	2-2-2

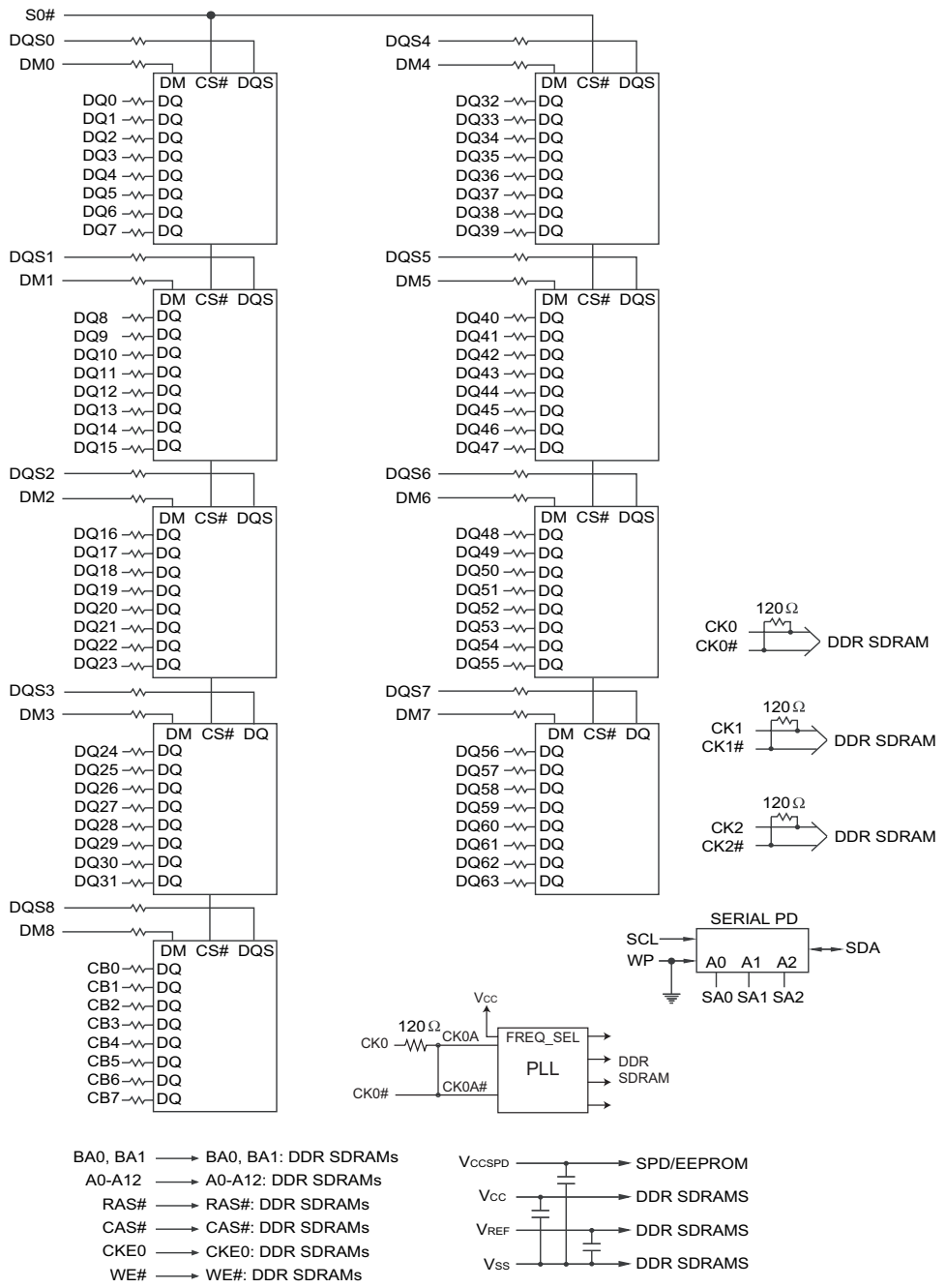
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	47	DQS8	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	DQS17
3	V_{SS}	49	CB2	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	CB6
5	DQS0	51	CB3	97	DQS9	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	RESET#	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DQS13
12	DQ8	58	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DQS10	153	DQ44
16	NC	62	V_{CCQ}	108	V_{CC}	154	RAS#
17	NC	63	WE#	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	CAS#	111	CKE1	157	CS0#
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	CS1#
21	CKE0	67	DQS5	113	NC	159	DQS14
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	V_{CCQ}	76	NC	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DQS15
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	CB4	180	$V_{CC}Q$
43	A1	89	V_{SS}	135	CB5	181	SA0
44	CB0	90	NC	136	V_{CCQ}	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V_{CC}	92	SCL	138	CK0#	184	V_{CCSPD}

PIN NAMES

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check bits
DQS0-DQS17	Data Strobe Input/Output
CK0	Clock Input
CK0#	Clock input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
V_{CC}	Power Supply
V_{CCQ}	Power Supply for DQS
V_{SS}	Ground
V_{REF}	Power Supply for Reference
V_{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V_{CCID}	V_{CC} Indentification Flag
NC	No Connect
RESET#	Reset Enable

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5 ~ 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	–1.0 ~ 3.6	V
Storage Temperature	T_{STG}	– 55 ~ +150	°C
Power Dissipation	P_D	9	W
Short Circuit Current	I_{OS}	50	mA

Note:
Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC CHARACTERISTICS

$0°C \le T_A \le 70°C$, V_{CC} = 2.5V ± 0.2V (100, 133 and 166MHz), V_{CCQ} = 2.6V ± 0.1V (200MHz)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	2.3	2.7	V
Supply Voltage	V_{CCQ}	2.3	2.7	V
Reference Voltage	V_{REF}	1.15	1.35	V
Termination Voltage	V_{TT}	1.15	1.35	V
Input High Voltage	V_{IH}	V_{REF} + 0.15	V_{CCQ} + 0.3	V
Input Low Voltage	V_{IL}	– 0.3	V_{REF} – 0.15	V
Output High Voltage	V_{OH}	V_{TT} + 0.76	—	V
Output Low Voltage	V_{OL}	—	V_{TT} – 0.76	V

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 2.5V ± 0.2V (100, 133 and 166MHz), V_{CCQ} = 2.6V ± 0.1V (200MHz)

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	29	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	29	pF
Input Capacitance (CKE0,CKE1)	C_{IN3}	29	pF
Input Capacitance (CK0,CK0#)	C_{IN4}	5.5	pF
Input Capacitance (CS0#,CS1#)	C_{IN5}	29	pF
Input Capacitance (DQM0-DQM8)	C_{IN6}	8	pF
Input Capacitance (BA0-BA1)	C_{IN7}	29	pF
Data input/output Capacitance (DQ0-DQ63)(DQS)	C_{OUT}	8	pF
Data input/output Capacitance (CB0-CB7)	C_{OUT}	8	pF

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

0°C ≤ T_A ≤ 70°C, V_{CC} = V_{CCQ} = 2.5V ± 0.2V (100, 133, 166MHz), V_{CC} = V_{CCQ} = +2.6V ± 0.1V (200MHz)

Parameter	Symbol	Conditions	DDR400@ CL=3	DDR333@ CL=2.5	DDR266@ CL=2, 2.5	DDR200@ CL=2	Units
			Max	Max	Max	Max	
Operating Current	I_{DD0}	One device bank; Active - Precharge; (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles. T_{RC}=T_{RC}(MIN); T_{CK}=T_{CK}	TBD	TBD	TBD	TBD	mA
Operating Current	I_{DD1}	One device bank; Active-Read-Precharge; Burst = 2; T_{RC}=T_{RC}(MIN);T_{CK}=T_{CK} (MIN); Iout = 0mA; Address and control inputs changing once per clock cycle.	TBD	TBD	TBD	TBD	mA
Precharge Power-Down Standby Current	I_{DD2P}	All device banks idle; Power-down mode; T_{CK}=T_{CK}(MIN); CKE=(low)	TBD	TBD	TBD	TBD	mA
Idle Standby Current	I_{DD2F}	CS# = High; All device banks idle; T_{CK}=T_{CK}(MIN); CKE = high; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS and DM.	TBD	TBD	TBD	TBD	mA
Active Power-Down Standby Current	I_{DD3P}	One device bank active; Power-down mode; T_{CK}(MIN); CKE=(low)	TBD	TBD	TBD	TBD	mA
Active Standby Current	I_{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; T_{RC}=T_{RAS}(MAX); T_{CK}=T_{CK}(MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	TBD	TBD	TBD	TBD	mA
Operating Current	I_{DD4R}	Burst = 2; Reads; Continous burst; One device bank active;Address andcontrol inputs changing once per clock cycle; T_{CK}=T_{CK}(MIN); I_{OUT} = 0mA.	TBD	TBD	TBD	TBD	mA
Operating Current	I_{DD4W}	Burst = 2; Writes; Continous burst; One device bank active; Address and control inputs changing once per clock cycle; T_{CK}=T_{CK}(MIN); DQ,DM and DQS inputs changing twice per clock cycle.	TBD	TBD	TBD	TBD	mA
Auto Refresh Current	I_{DD5}	T_{RC}=T_{RC}(MIN)	TBD	TBD	TBD	TBD	mA
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	TBD	TBD	TBD	TBD	mA
Operating Current	I_{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with T_{RC}=T_{RC} (MIN); T_{CK}=T_{CK}(MIN); Address and control inputs change only during Active Read or Write commands	TBD	TBD	TBD	TBD	mA

DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RCD}=2*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL=2, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RCD}=10*t_{CK}, t_{RAS}=7*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR400 (200MHz, CL=3) : t_{CK}=5ns, BL=4, t_{RCD}=15*t_{CK}, t_{RAS}=7*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

Legend : A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3
R (0-3) = Read Bank 0-3

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout=0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}
     Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL2=2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=2*t_{CK}
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR400 (200MHz, CL=3) : t_{CK}=5ns, BL=4, t_{RRD}=10*t_{CK}, t_{RCD}=15*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

DDR400: V_{CC} = V_{CCQ} = +2.6V ± 0.1V

AC CHARACTERISTICS			403		335		262		265		202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#		t_{AC}	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	0.75	-0.8	0.8	ns	
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	25
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	25
Clock cycle time	CL = 3	$t_{CK\ (3)}$	5	7.5	6	13	7.5	13	7.5	13	8	13	ns	38, 43
	CL = 2.5	$t_{CK\ (2.5)}$	6	13	7.5	13	7.5	13	7.5/10	13	10	13	ns	38, 43
	CL = 2	$t_{CK\ (2)}$	7.5	13									ns	37, 42
DQ and DM input hold time relative to DQS		t_{DH}	0.4		0.45		0.5			0.6			ns	22, 26
DQ and DM input setup time relative to DQS		t_{DS}	0.4		0.45		0.5			0.6			ns	22, 26
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		1.75			2			ns	26
Access window of DQS from CK/CK#		t_{DQSCK}	-0.6	+0.6	-0.60	+0.60	-0.75	+0.75	+0.75	-0.8	+0.8		ns	
DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35			0.35			t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35			0.35			t_{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.40		0.45		0.5		0.5		0.6	ns	22
Write command to first DQS latching transition		t_{DQSS}	0.72	1.28	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		0.2		0.2		0.2		t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		0.2		0.2		0.2		t_{CK}	
Half clock period		t_{HP}	t_{CH},t_{CL}		t_{CH},t_{CL}		t_{CH},t_{CL}		t_{CH},t_{CL}		t_{CH},t_{CL}		ns	29
Data-out high-impedance window from CK/CK#		t_{HZ}		+0.70		+0.70		+0.75		+0.75		+0.8	ns	16, 36
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.70		-0.70		-0.75		-0.75		-0.8		ns	16, 36
Address and control input hold time (1 V/ns)		t_{IHF}	0.6		0.75		0.90		0.90	1.1	ns	12	ns	12
Address and control input setup time (1 V/ns)		t_{ISF}	0.6		0.75		0.90		0.90		1.1		ns	12
Address and control input hold time (0.5 V/ns)		t_{IHS}	0.6		0.80		1		1		1.1		ns	12
Address and control input setup time (0.5 V/ns)		t_{ISS}	0.6		0.80		1		1		1.1		ns	12
Address and Control input pulse width (for each input)		t_{IPW}	2.20		2.2		2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time		t_{MRD}	2		12		15		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns	22
Data hold skew factor		t_{QHS}		0.50		0.60		0.75		0.75		1	ns	
ACTIVE to PRECHARGE command		t_{RAS}	40	70,000	42	70,000	40	120,000	40	120,000	40	120,000	ns	30
ACTIVE to READ with Auto precharge command		t_{RAP}	15		15		15		20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		t_{RC}	55		60		60		65		70		ns	
AUTO REFRESH command period		t_{RFC}	70		72		75		72		75		ns	41
ACTIVE to READ or WRITE delay		t_{RCD}	15		15		15		20		20		ns	
PRECHARGE command period		t_{RP}	15		15		15		20		20		ns	
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	36
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	36
ACTIVE bank a to ACTIVE bank b command		t_{RRD}	10		12		15		15		15		ns	
DQS write preamble		t_{WPRE}	0.25		0.25		0.25		0.25		0.25		t_{CK}	
DQS write preamble setup time		t_{WPRES}	0		0		0		0		0		ns	17, 19

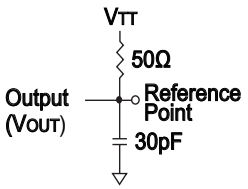
DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

DDR400: V_{CC} = V_{CCQ} = +2.6V ± 0.1V

AC CHARACTERISTICS		403		355		262		265		202			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	17
Write recovery time	t_{WR}	15		15		15		15		15		ns	
Internal WRITE to READ command delay	t_{WTR}	2		1		1		1		1		t_{CK}	
Data valid output window	na	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		tQH - tDQSQ		tQH - tDQSQ		ns	22
REFRESH to REFRESH command interval	t_{REFC}		70.3		70.3		70.3		70.3		70.3	µs	21
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8		7.8		7.8	µs	21
Terminating voltage delay to V_{CC}	t_{VTD}	0		0		0		0		0		ns	
Exit SELF REFRESH to non-READ command	t_{XSNR}	75		75		75		75		80		ns	
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		200		200		t_{CK}	

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The mini-mum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL} (AC) and V_{IH} (AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal $V_{CCQ/2}$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from $V_{CCQ/2}$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with mini-mum cycle time at CL = 2 for 262 and 202, CL = 2.5 for 265, 335 and CL = 3 for 403 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = $V_{CCQ/2}$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates < 1 V/ns and ≥ to 0.5 Vns. If the slew rate is < 0.5V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100 mV/ns reduction in slew rate from 500 mV/ns, while t_{IH} is unaffected. If the slew rate exceeds 4.5 V/ns, functionality is uncertain. For 403, slew rates must be 0.5 V/ns.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE < 0.3 x V_{CCQ} is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. t_{HZ} and t_{LZ} transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low, or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions high [above V_{IHDC} (MIN)] then it must not transition low (below V_{IHDC}) prior to t_{DQSH} (MIN).
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{DQSS}.
20. MIN (t_{RC} or t_{RFC}) for I_{DD} measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RAS} (MAX) for I_{DD} measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS}.
21. The refresh period 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be as-serted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The data valid window is derived by achieving other specifications: t_{HP} ($t_{CK/2}$), t_{DQSQ}, and t_{QH} (t_{QH} = t_{HP} - t_{QHS}). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain. Figure 7, Derating Data Valid Window, shows derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (t_{RFC} [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL}(AC) or V_{IH}(AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, V_{IL}(DC) or V_{IH}(DC).
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/ DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain. For 403, slew rates must be ≥ 0.5 V/ns.
28. V_{CC} must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. t_{HP} min is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until t_{RAS}(MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch in the nominal voltage must be less than 1/3 of the clock and not more than +400mV or 2.9V maximum, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V mini-mum, whichever is more positive.

33. The voltage levels used are derived from a mini-mum V_{CC} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
34. V_{IH} overshoot: V_{IH} (MAX) = V_{CCQ} + 1.5V for a pulse width < 3ns and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
35. V_{CC} and V_{CCQ} must track each other.
36. t_{HZ} (MAX) will prevail over t_{DQSCK} (MAX) + t_{RPST} (MAX) condition. t_{LZ} (MIN) will prevail over t_{DQSCK} (MIN) + t_{RPRE} (MAX) condition.
37. t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}).
38. During initialization, V_{CCQ}, V_{TT}, and V_{REF} must be equal to or less than V_{CC} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{CC}/V_{CCQ} are 0V, provided a minimum of 42 0 of series resistance is used between the V_{TT} supply and the input pin.
39. The current part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
40. Random addressing changing and 50 percent of data changing at every transfer.
41. Random addressing changing and 100 percent of data changing at every transfer.
42. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{REF} later.
43. I_{DD2N} specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. I_{DD2Q} is similar to I_{DD2F} except I_{DD2Q} specifies the address and control inputs to remain stable. Although I_{DD2F}, I_{DD2N}, and I_{DD2Q} are similar, I_{DD2F} is “worst case.”
44. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).
45. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
46. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.
47. The 403 speed grade will operate with t_{RAS} (MIN) = 40 ns and t_{RAS} (MAX) = 120,000ns at any slower frequency.

ORDERING INFORMATION FOR JD3

Part Number	Speed	Height*	Commercial Operating Range
W3EG128M72ETSU403JD3	200MHz/400Mbps, CL=3	30.48 (1.20")	0°C to 70°C
W3EG128M72ETSU335JD3	166MHz/333Mbps, CL=2.5	30.48 (1.20")	0°C to 70°C
W3EG128M72ETSU262JD3	133MHz/266Mbps, CL=2	30.48 (1.20")	0°C to 70°C
W3EG128M72ETSU265JD3	133MHz/266Mbps, CL=2.5	30.48 (1.20")	0°C to 70°C
W3EG128M72ETSU202JD3	100MHz/200Mbps, CL=2	30.48 (1.20")	0°C to 70°C

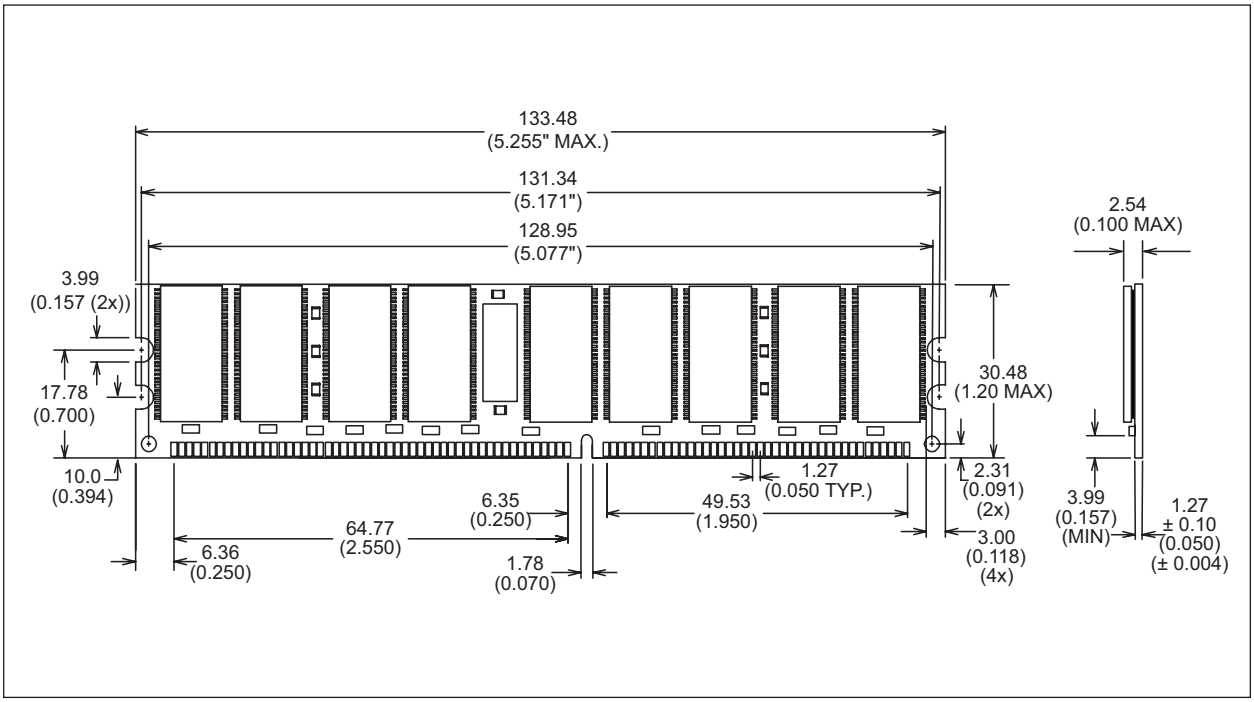
NOTE:

1 * Consult Factory for availability of lead-free products. (F = Lead-Free, G = RoHS Compliant)

2 * Product specific part numbers are available for source control if needed, please consult factory for the correct part number if a specific component vendor is preferred.

3 * Consult factory for availability for industrial temperature (-40°C to 85°C) options

PACKAGE DIMENSIONS FOR JD3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION FOR AJD3

Part Number	Speed	Height*	Commercial Operating Range
W3EG128M72ETSU403AJD3	200MHz/400Mbps, CL=3	28.70 (1.13") MAX	0°C to 70°C
W3EG128M72ETSU335AJD3	166MHz/333Mbps, CL=2.5	28.70 (1.13") MAX	0°C to 70°C
W3EG128M72ETSU262AJD3	133MHz/266Mbps, CL=2	28.70 (1.13") MAX	0°C to 70°C
W3EG128M72ETSU265AJD3	133MHz/266Mbps, CL=2.5	28.70 (1.13") MAX	0°C to 70°C
W3EG128M72ETSU202AJD3	100MHz/200Mbps, CL=2	28.70 (1.13") MAX	0°C to 70°C

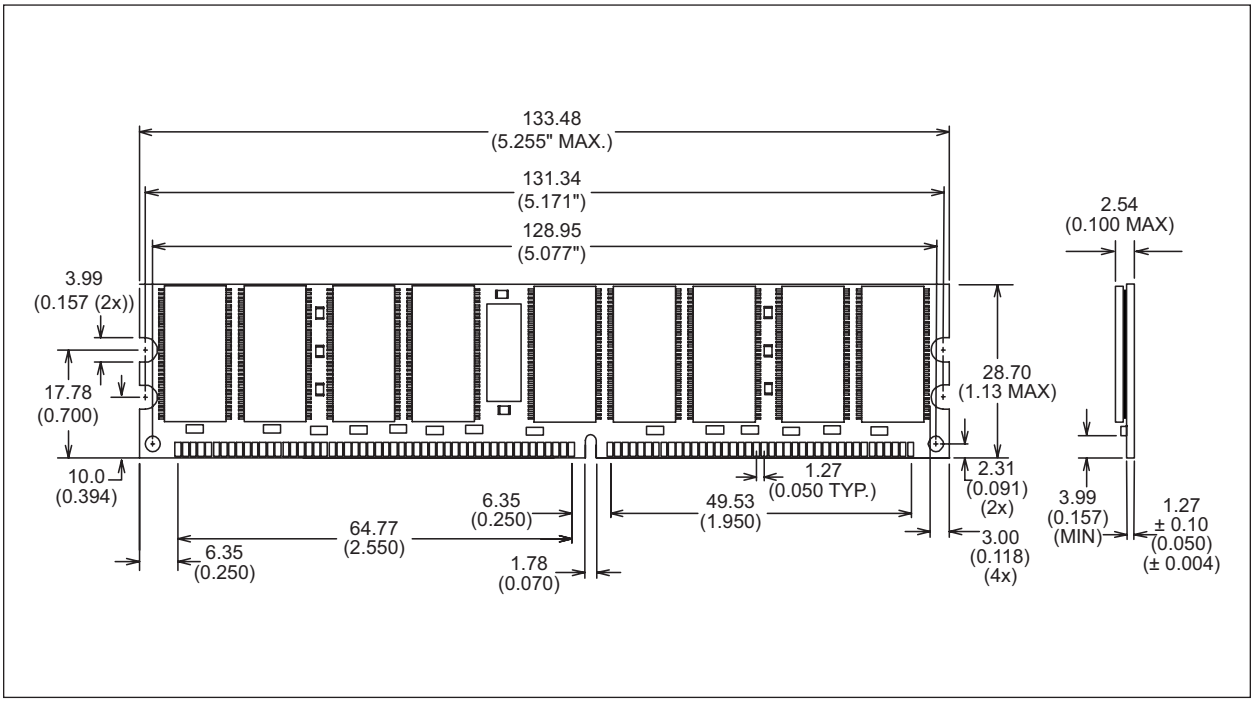
NOTE:

1 * Consult Factory for availability of lead-free products. (F = Lead-Free, G = RoHS Compliant)

2 * Product specific part numbers are available for source control if needed, please consult factory for the correct part number if a specific component vendor is preferred.

3 * Consult factory for availability for industrial temperature (-40°C to 85°C) options

PACKAGE DIMENSIONS FOR AJD3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

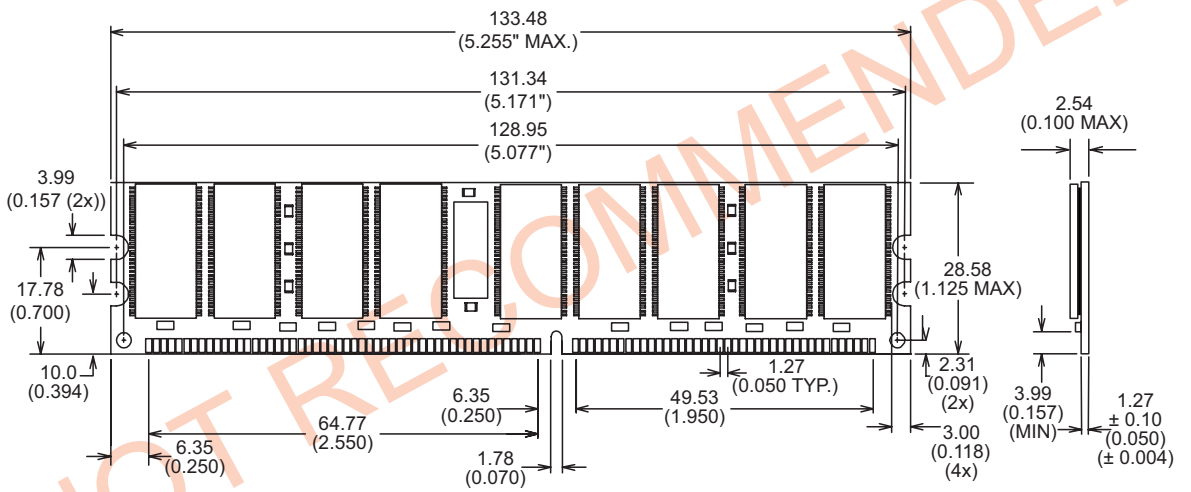
ORDERING INFORMATION FOR D3

Part Number	Speed	Height*	Commercial Operating Range
W3EG128M72ETSU403D3	200MHz/400Mbps, CL=3	28.58 (1.125") MAX	0°C to 70°C
W3EG128M72ETSU335D3	166MHz/333Mbps, CL=2.5	28.58 (1.125") MAX	0°C to 70°C
W3EG128M72ETSU262D3	133MHz/266Mbps, CL=2	28.58 (1.125") MAX	0°C to 70°C
W3EG128M72ETSU265D3	133MHz/266Mbps, CL=2.5	28.58 (1.125") MAX	0°C to 70°C
W3EG128M72ETSU202D3	100MHz/200Mbps, CL=2	28.58 (1.125") MAX	0°C to 70°C

NOTE:
1 * Consult Factory for availability of lead-free products. (F = Lead-Free, G = RoHS Compliant)
2 * Product specific part numbers are available for source control if needed, please consult factory for the correct part number if a specific component vendor is preferred.
3 * Consult factory for availability for industrial temperature (-40°C to 85°C) options

PACKAGE DIMENSIONS FOR D3

Note: D3 Not Recommended For New Designs



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

Document Title

1GB – 128Mx72, DDR, SDRAM Unbuffered ECC, w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	1-04-05	Advanced