

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

16,777,216-WORD BY 1-BIT CMOS STATIC RAM

DESCRIPTION

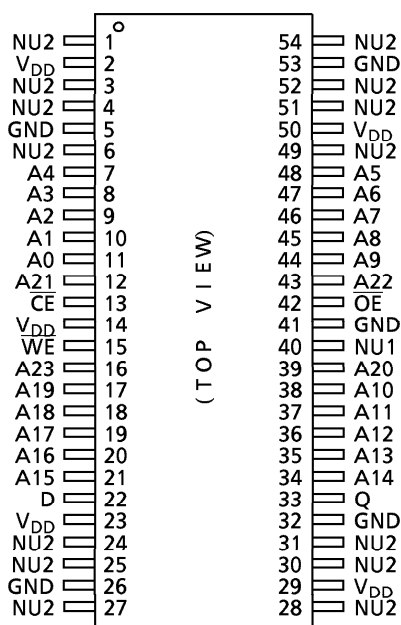
The TC55V11601FT is a 16,777,216-bit high speed static random access memory (SRAM) organized as 16,777,216 words by 1 bit. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable (\overline{CE}) can be used to place the device in a low-power mode, and output enable (\overline{OE}) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are isolated and directly LVTTL compatible. The TC55V11601FT is available in a plastic 54-pin TSOP package with 400 mil width for high density surface assembly.

FEATURES

- Fast access time (the following are maximum values)
 - TC55V11601FT-15 : 15 ns
- Low-power dissipation
- Standby : 4mA(max)
- Single power supply voltage of $3.3V \pm 0.3V$
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Separate data input and output
- Output buffer control using \overline{OE}
- Package :
 - TSOP II 54-P-400-0.80B (FT) (Weight : 0.55 g typ)

Cycle Time	15	30	ns
Operation (max)	200	130	mA

PIN ASSIGNMENT



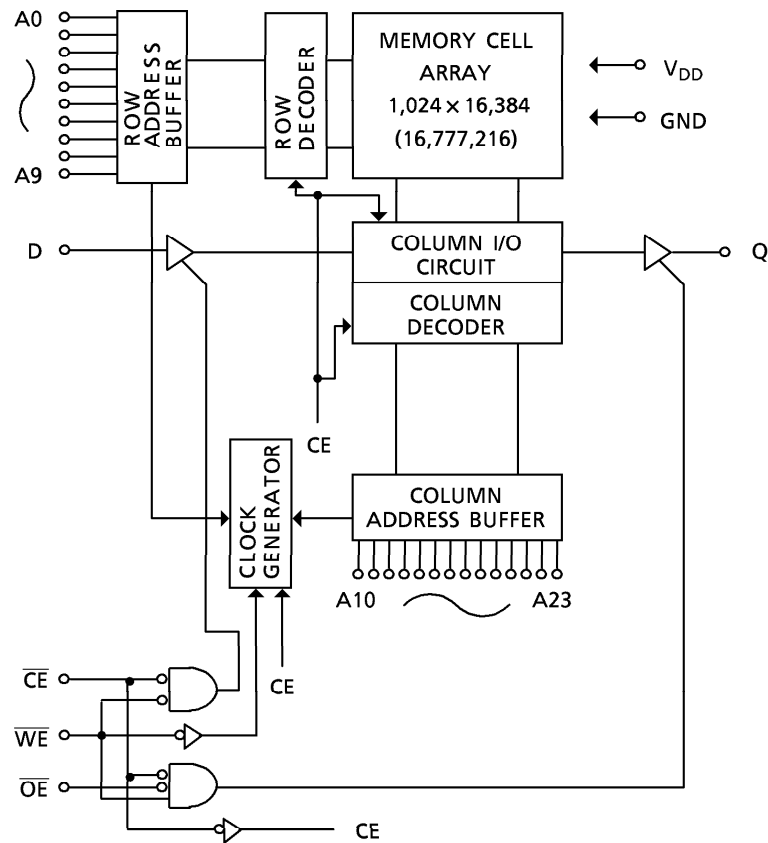
PIN NAMES

A0 to A23	Address Inputs
D	Data Input
Q	Data Output
\overline{CE}	Chip Enable Input
WE	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+ 3.3 V)
GND	Ground
NU1, NU2	Not Usable

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.5 to 4.6	V
V_{IN}	Input Terminal Voltage	- 0.5* to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	- 0.5* to $V_{DD} + 0.5^{**}$	V
P_D	Power Dissipation	1.8	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	- 65 to 150	°C
T_{opr}	Operating Temperature	- 10 to 85	°C

* : -1.5V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : $V_{DD} + 1.5V$ with a pulse width of 20% · t_{RC} min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0^\circ$ to $70^\circ C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	$V_{DD} + 0.3^{**}$	V
V_{IL}	Input Low Voltage	- 0.3*	-	0.8	V

* : -1.0V with a pulse width of 20% · t_{RC} min (4ns max)
 ** : $V_{DD} + 1.0V$ with a pulse width of 20% · t_{RC} min (4ns max)

DC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I_{IL}	Input Leakage Current (Except NU1 pin)	$V_{IN} = 0$ to V_{DD}	-1	-	1	μA	
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0$ to V_{DD}	-1	-	1	μA	
I_I (NU1)	Input Current (NU1 pin)	$V_{IN} = 0$ to 0.8V	-1	-	20	μA	
		$V_{IN} = 0$ to 0.2V	-1	-	1		
V_{OH}	Output High Voltage	$I_{OH} = -2\text{mA}$	2.4	-	-	V	
		$I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2$	-	-		
V_{OL}	Output Low Voltage	$I_{OL} = 2\text{mA}$	-	-	0.4		
		$I_{OL} = 100\mu\text{A}$	-	-	0.2		
I_{DDO}	Operating Current	$\overline{CE} = V_{IL}$, $I_{out} = 0\text{mA}$ $\overline{OE} = V_{IH}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	tcycle = 15ns	-	-	200	mA
			tcycle = 30ns	-	-	130	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V_{IH} or V_{IL}	-	-	65	mA	
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ Other Inputs = $V_{DD} - 0.2\text{V}$ or 0.2V	-	-	4		

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	D	Q	POWER
Read	L	L	H	X	Dout	I_{DDO}
Write	L	X	L	Din	High-Z	I_{DDO}
Outputs Disable	L	H	H	X	High-Z	I_{DDO}
Standby	H	X	X	X	High-Z	I_{DDS}

X : Don't care

Note: The NU1 and NU2 pins must be left unconnected or tied to GND or a voltage level of less than 0.8 V. You must not apply a voltage of more than 0.8 V to the NU1 and NU2.

AC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C (Note 1), $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

READ CYCLE

SYMBOL	PARAMETER	TC55V11601FT-15		UNIT
		MIN	MAX	
t_{RC}	Read Cycle Time	15	–	ns
t_{ACC}	Address Access Time	–	15	
t_{CO}	Chip Enable Access Time	–	15	
t_{OE}	Output Enable Access Time	–	8	
t_{OH}	Output Data Hold Time from Address Change	3	–	
t_{COE}	Output Enable Time from Chip Enable	3	–	
t_{OEE}	Output Enable Time from Output Enable	1	–	
t_{COD}	Output Disable Time from Chip Enable	–	8	
t_{ODO}	Output Disable Time from Output Enable	–	8	

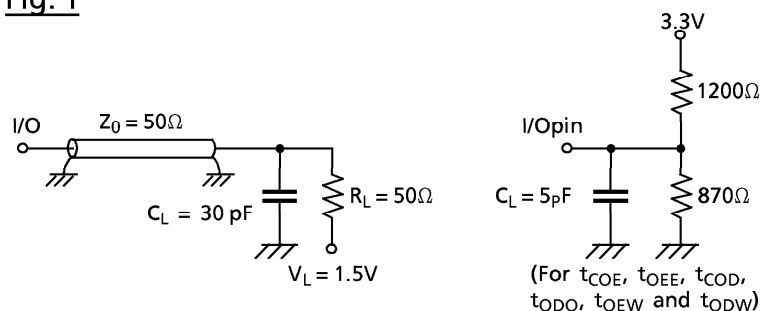
WRITE CYCLE

SYMBOL	PARAMETER	TC55V11601FT-15		UNIT
		MIN	MAX	
t_{WC}	Write Cycle Time	15	–	ns
t_{WP}	Write Pulse Width	10	–	
t_{CW}	Chip Enable to End of Write	11	–	
t_{AW}	Address Valid to End of Write	11	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{DS}	Data Setup Time	8	–	
t_{DH}	Data Hold Time	0	–	
t_{OEw}	Output Enable Time from Write Enable	1	–	
t_{ODw}	Output Disable Time from Write Enable	–	8	

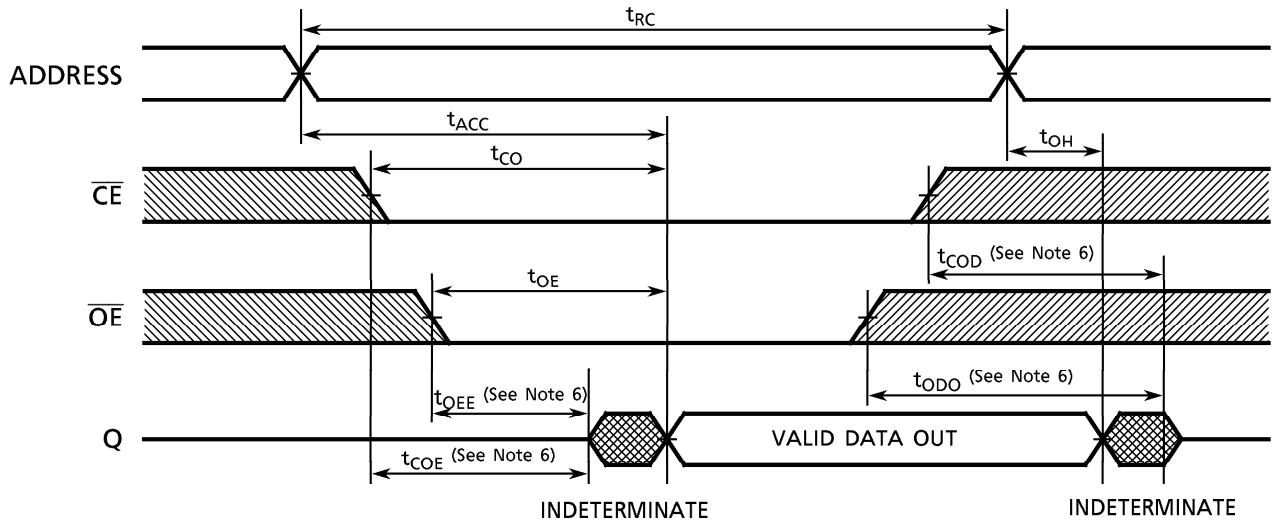
AC TEST CONDITIONS

Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

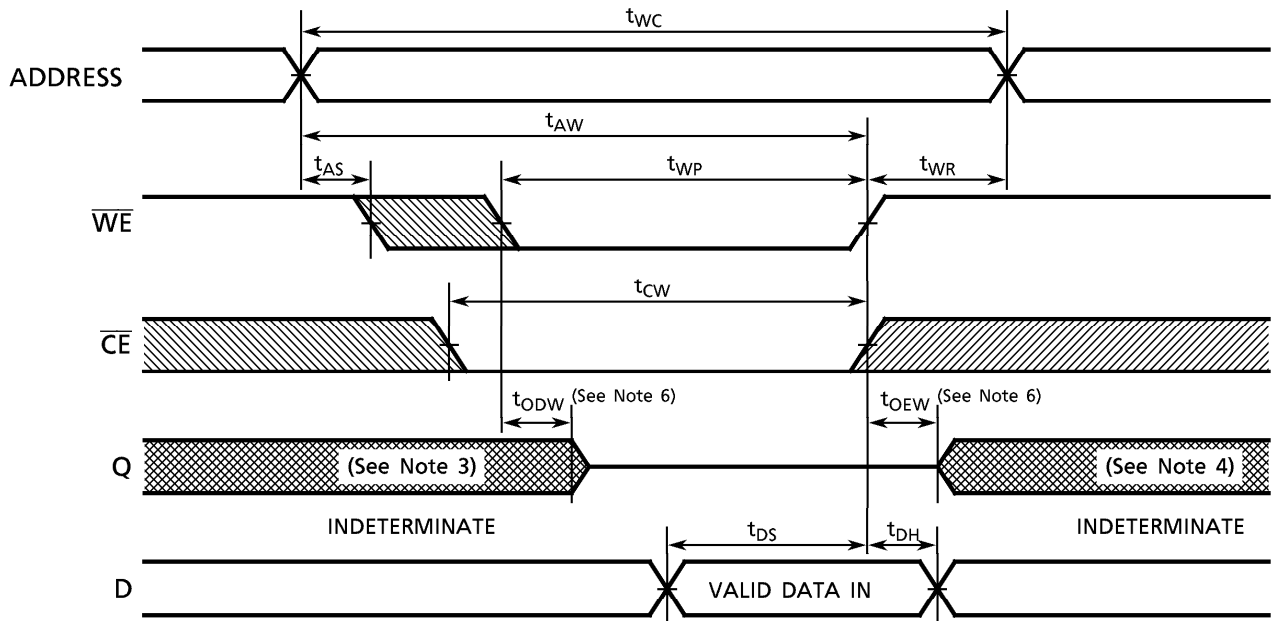
Fig. 1



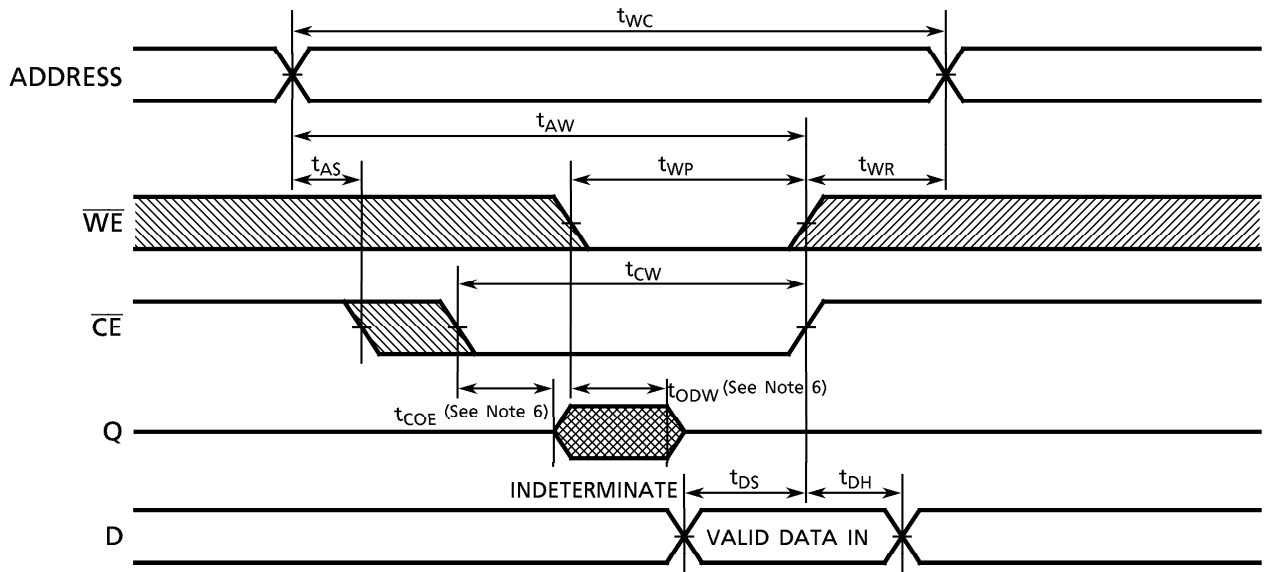
TIMING DIAGRAMS
READ CYCLE (See Note 2)



WRITE CYCLE 1 (\overline{WE} CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 5)



Note: (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) \overline{WE} remains HIGH for Read Cycle.

(3) If \overline{CE} goes LOW coincident with or after \overline{WE} goes LOW, the outputs will remain at high impedance.

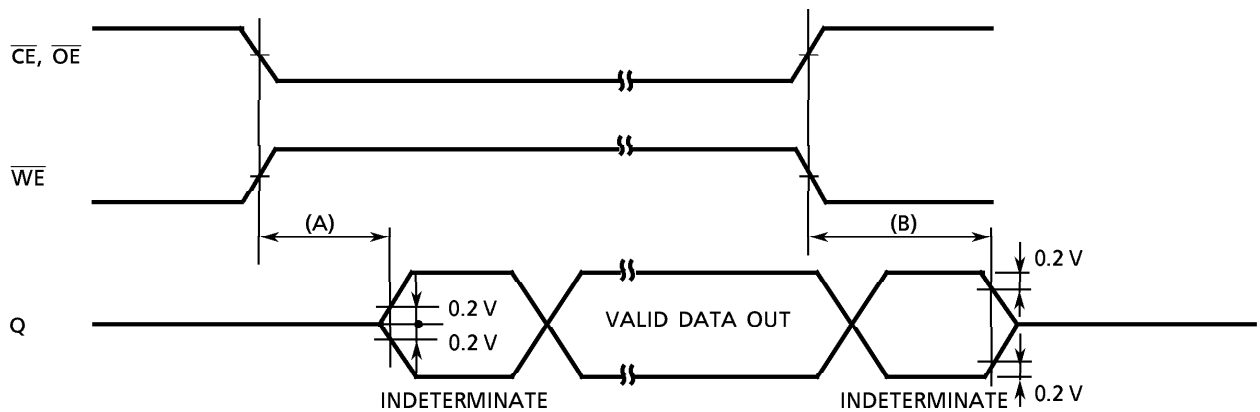
(4) If \overline{CE} goes HIGH coincident with or before \overline{WE} goes HIGH, the outputs will remain at high impedance.

(5) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{OE\overline{W}}$ Output Enable Time

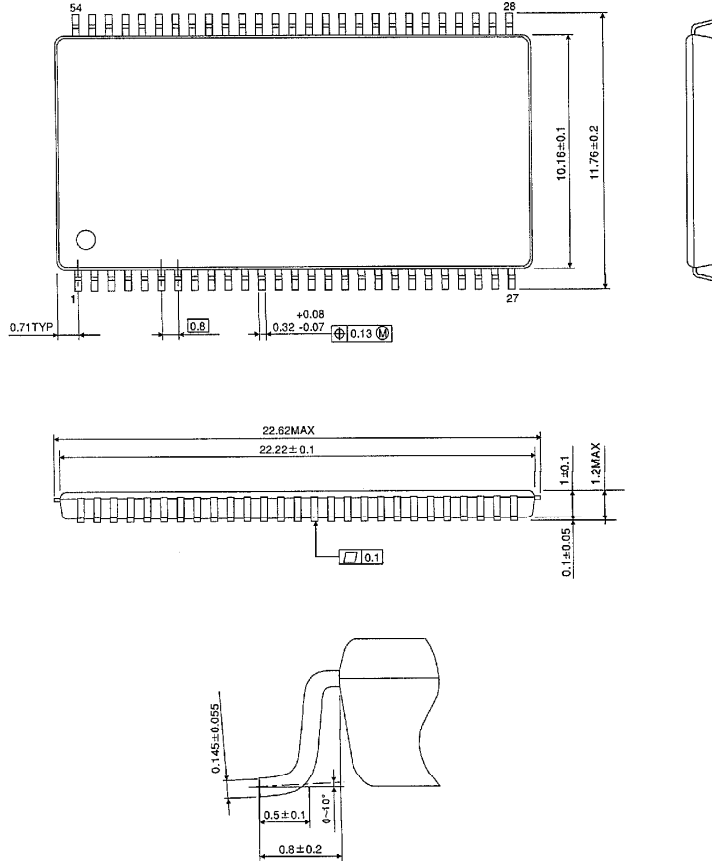
(B) $t_{COD}, t_{ODO}, t_{OD\overline{W}}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 54-P-400-0.80B)

Unit in mm



Weight : 0.55g (Typ)