

256K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC SRAM

PRELIMINARY INFORMATION
JUNE 2006

FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
 - 36 mW (typical) operating
 - 9 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
 - 1.65V--2.2V V_{DD} (65WV25616ALL)
 - 2.5V--3.6V V_{DD} (65WV25616BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- TEMPERATURE OFFERINGS:
 - Option A1: -40°C to +85°C
 - Option A2: -40°C to +105°C
 - Option A3: -40°C to +125°C
- Lead-free available

DESCRIPTION

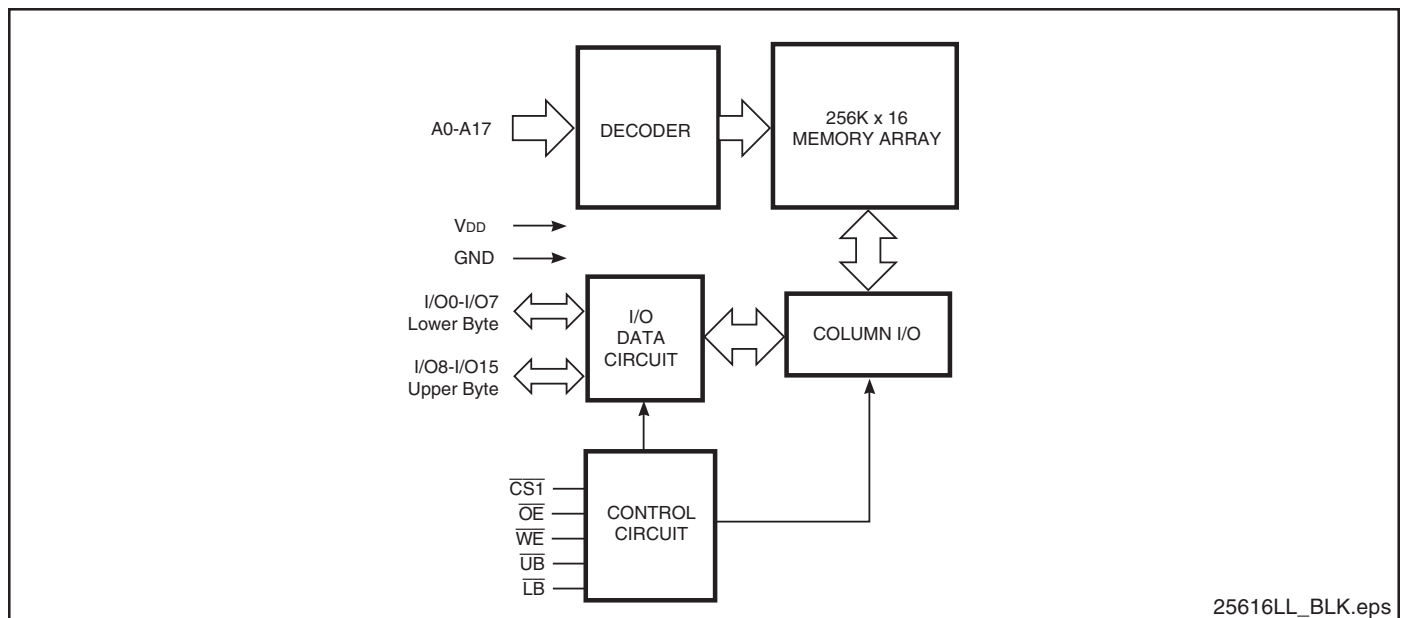
The *ISSI* IS65WV25616ALL/IS65WV25616BLL are high-speed, low power, 4M bit SRAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when $\overline{CS1}$ is LOW, and both \overline{LB} and \overline{UB} are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS65WV25616BALL/65WV25616BLL are packaged in the JEDEC standard 44-Pin TSOP (TYPE II).

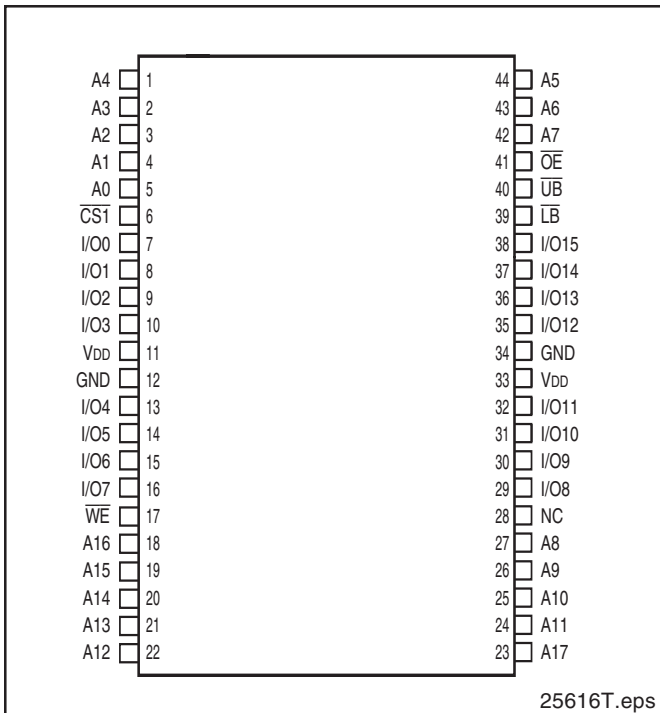
FUNCTIONAL BLOCK DIAGRAM



25616LL_BLK.eps

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**44-Pin mini TSOP (Type II)
(Package Code T)**



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$	Chip Enable Input
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
\overline{LB}	Lower-byte Control (I/O0-I/O7)
\overline{UB}	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

TRUTH TABLE

Mode	I/O PIN					I/O PIN		VDD Current
	\overline{WE}	$\overline{CS1}$	\overline{OE}	\overline{LB}	\overline{UB}	I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	ISB1, ISB2
	X	X	X	X	X	High-Z	High-Z	ISB1, ISB2
	X	X	X	H	H	High-Z	High-Z	ISB1, ISB2
Output Disabled	H	L	H	L	X	High-Z	High-Z	Icc
	H	L	H	X	L	High-Z	High-Z	Icc
Read	H	L	L	L	H	Dout	High-Z	Icc
	H	L	L	H	L	High-Z	Dout	
	H	L	L	L	L	Dout	Dout	
Write	L	L	X	L	H	Din	High-Z	Icc
	L	L	X	H	L	High-Z	Din	
	L	L	X	L	L	Din	Din	

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.2 to V _{DD} +0.3	V
V _{DD}	V _{DD} Related to GND	-0.2 to V _{DD} +0.3	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS65WV25616ALL	IS65WV25616BLL
A1	-40°C to +85°C	1.65V - 2.2V	2.5V-3.6V
A2	-40°C to +105°C	1.65V - 2.2V	2.5V-3.6V
A3	-40°C to +125°C	1.65V - 2.2V	2.5V-3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V _{DD}	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I _{OH} = -1 mA	2.5-3.6V	2.2	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I _{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V _{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V _{DD} + 0.2	V
			2.5-3.6V	2.2	V _{DD} + 0.3	V
V _{IL} ⁽¹⁾	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}		-2	2	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled		-2	2	μA

Notes:

1. V_{IL} (min.) = -1.0V for pulse width less than 10 ns.

IS65WV25616ALL, POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70	Unit
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} =Max.,	A1	25	mA
		I _{OUT} =0 mA, f=f _{MAX}	A2, A3	30	
I _{CC1}	Operating Supply Current	V _{DD} =Max., $\overline{CS1}=0.2V$	A1	10	mA
		$\overline{WE}=V_{DD}-0.2V$ f=1MHz	A2, A3	15	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} =Max.,	A1	0.5	mA
		V _{IN} =V _{IH} or V _{IL} $\overline{CS1}=V_{IH}$, f=1 MHz	A2, A3	0.6	
OR					
	ULB Control	V _{DD} =Max., V _{IN} =V _{IH} or V _{IL} $\overline{CS1}=V_{IL}$, f=0, $\overline{UB}=V_{IH}$, $\overline{LB}=V_{IH}$			
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} =Max.,	A1	15	μA
		$\overline{CS1} \geq V_{DD}-0.2V$, V _{IN} ≥ V _{DD} -0.2V, or V _{IN} ≤ 0.2V, f=0	A2 A3	30 50	
OR					
	ULB Control	V _{DD} = Max., $\overline{CS1} = V_{IL}$, V _{IN} ≤ 0.2V, f=0; $\overline{UB}/\overline{LB}=V_{DD}-0.2V$			

IS65WV25616BLL, POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Unit
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} =Max.,	A1	40	—	mA
		I _{OUT} =0 mA, f=f _{MAX}	A2, A3	—	40	
I _{CC1}	Operating Supply Current	V _{DD} =Max., $\overline{CS1}=0.2V$	A1	15	—	mA
		$\overline{WE}=V_{DD}-0.2V$, f=1MHz	A2, A3	—	20	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} =Max.,	A1	0.45	—	mA
		V _{IN} =V _{IH} or V _{IL} $\overline{CS1}=V_{IH}$, f=1 MHz	A2, A3	—	0.45	
OR						
	ULB Control	V _{DD} =Max., V _{IN} =V _{IH} or V _{IL} $\overline{CS1}=V_{IL}$, f=0, $\overline{UB}=V_{IH}$, $\overline{LB}=V_{IH}$				
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} =Max.,	A1	20	—	μA
		$\overline{CS1} \geq V_{DD}-0.2V$, V _{IN} ≥ V _{DD} -0.2V, or V _{IN} ≤ 0.2V, f=0	A2 A3	— —	55 90	
OR						
	ULB Control	V _{DD} = Max., $\overline{CS1} = V_{IL}$, V _{IN} ≤ 0.2V, f=0; $\overline{UB}/\overline{LB}=V_{DD}-0.2V$				

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	10	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	IS65WV25616ALL (Unit)	IS65WV25616BLL (Unit)
Input Pulse Level	0.4V to V _{DD} -0.2V	0.4V to V _{DD} -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V _{REF}	V _{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	IS65WV25616ALL 1.65V-2.2V	IS65WV25616BLL 2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V _{REF}	0.9V	1.5V
V _{TM}	1.8V	2.8V

AC TEST LOADS

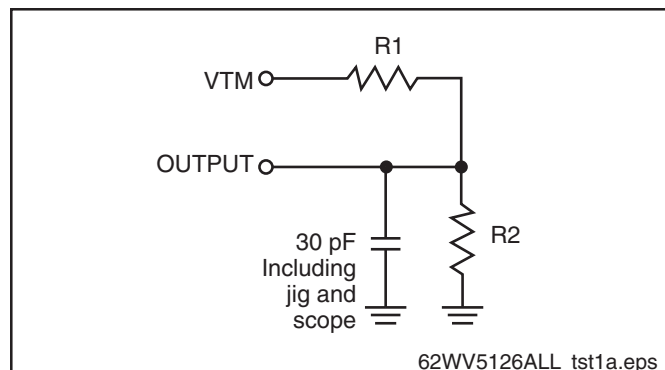


Figure 1

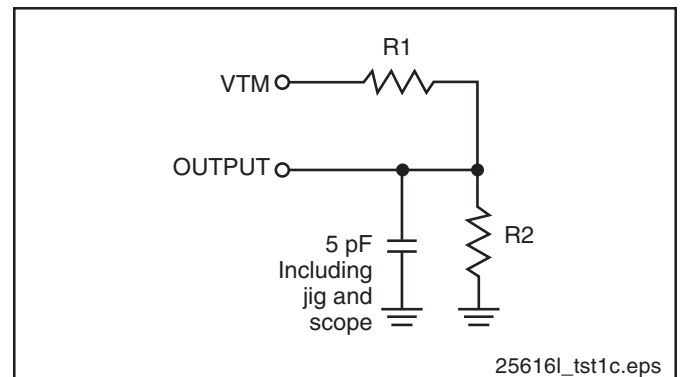


Figure 2

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

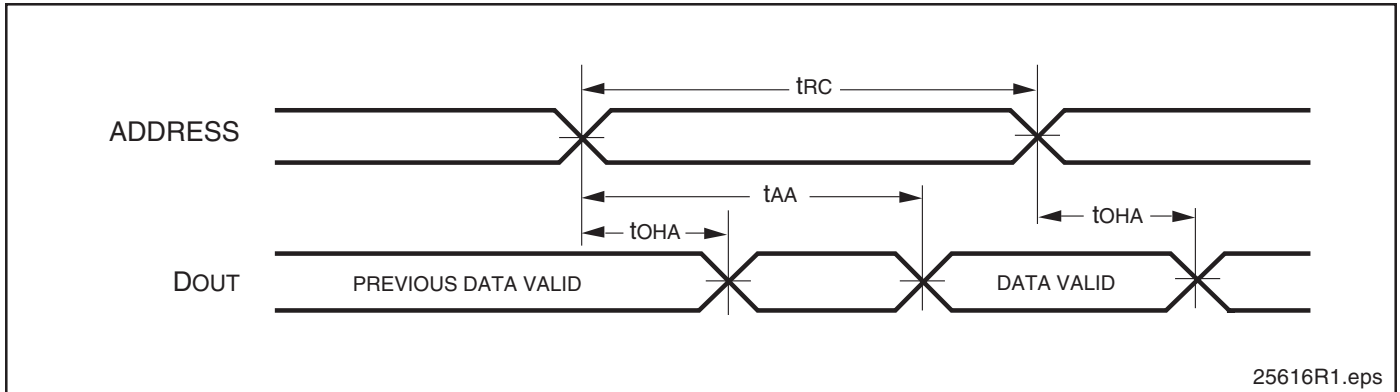
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	55	—	70	—	ns
t _{AA}	Address Access Time	—	55	—	70	ns
t _{OHA}	Output Hold Time	10	—	10	—	ns
t _{ACS1}	$\overline{CS1}$ Access Time	—	55	—	70	ns
t _{DOE}	\overline{OE} Access Time	—	25	—	35	ns
t _{HZOE} ⁽²⁾	\overline{OE} to High-Z Output	—	20	—	25	ns
t _{LZOE} ⁽²⁾	\overline{OE} to Low-Z Output	5	—	5	—	ns
t _{HZCS1}	$\overline{CS1}$ to High-Z Output	0	20	0	25	ns
t _{LZCS1}	$\overline{CS1}$ to Low-Z Output	10	—	10	—	ns
t _{BA}	\overline{LB} , \overline{UB} Access Time	—	55	—	70	ns
t _{HZB}	\overline{LB} , \overline{UB} to High-Z Output	0	20	0	25	ns
t _{LZB}	\overline{LB} , \overline{UB} to Low-Z Output	0	—	0	—	ns

Notes:

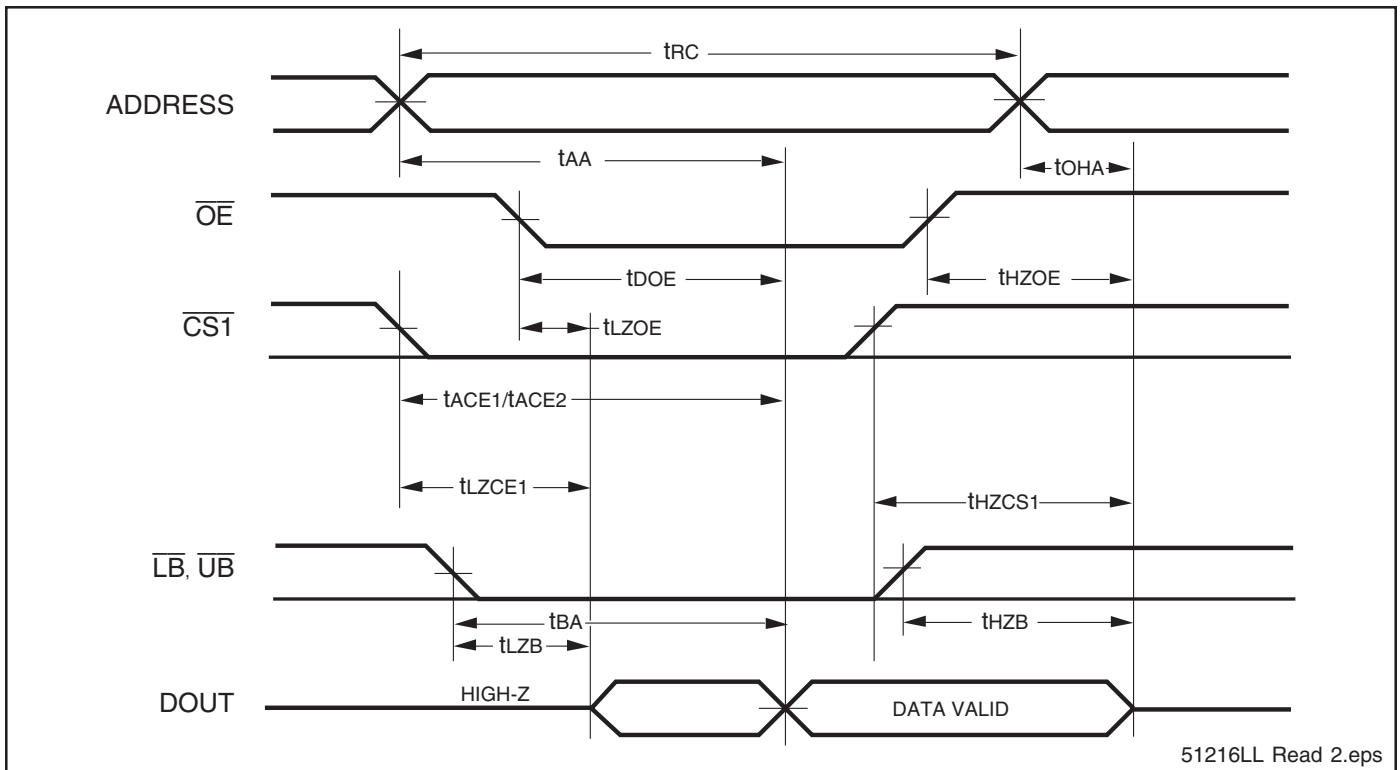
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CS1} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, \overline{OE} , AND $\overline{UB/LB}$ Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CS1}$, \overline{UB} , or $\overline{LB} = V_{IL}$. $\overline{WE} = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

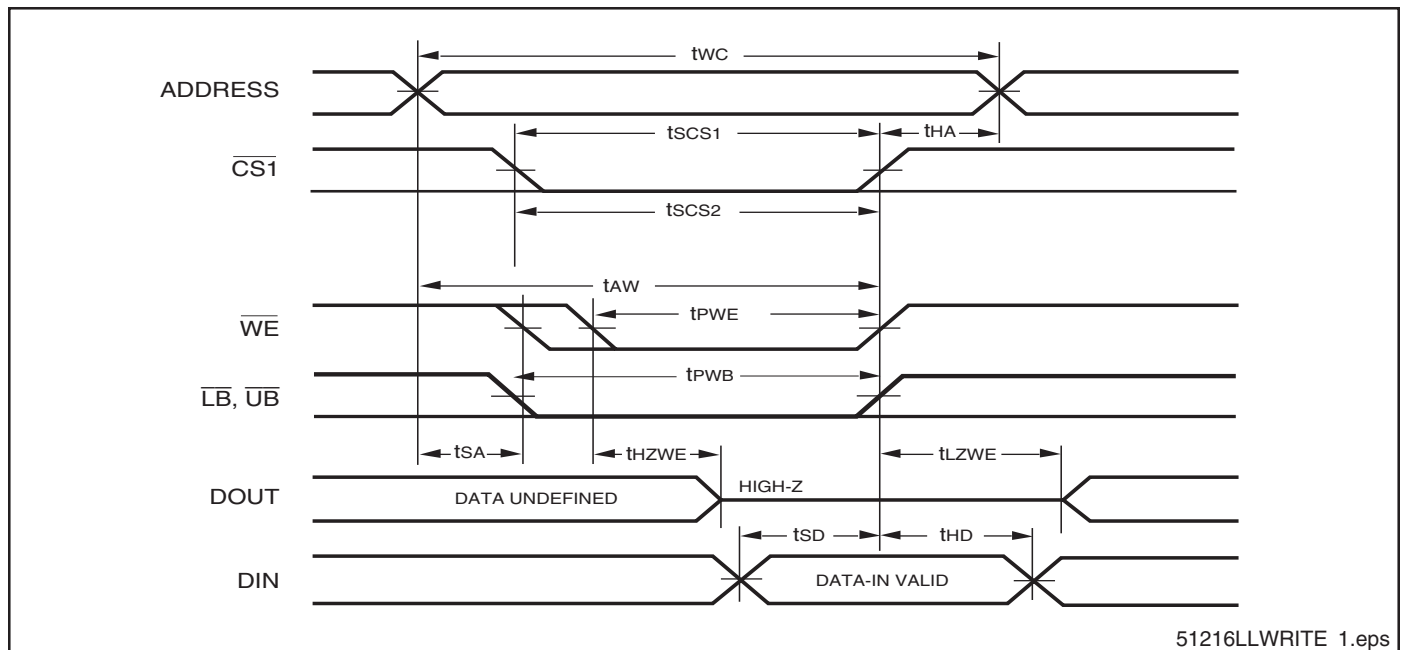
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	55	—	70	—	ns
t _{SCS1}	$\overline{\text{CS1}}$ to Write End	45	—	60	—	ns
t _{AW}	Address Setup Time to Write End	45	—	60	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	ns
t _{PWB}	$\overline{\text{LB}}$, $\overline{\text{UB}}$ Valid to End of Write	45	—	60	—	ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	40	—	50	—	ns
t _{SD}	Data Setup to Write End	25	—	30	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	ns
t _{HZWE} ⁽³⁾	$\overline{\text{WE}}$ LOW to High-Z Output	—	20	—	20	ns
t _{LZWE} ⁽³⁾	$\overline{\text{WE}}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{\text{CS1}}$ LOW and $\overline{\text{UB}}$ or $\overline{\text{LB}}$, and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

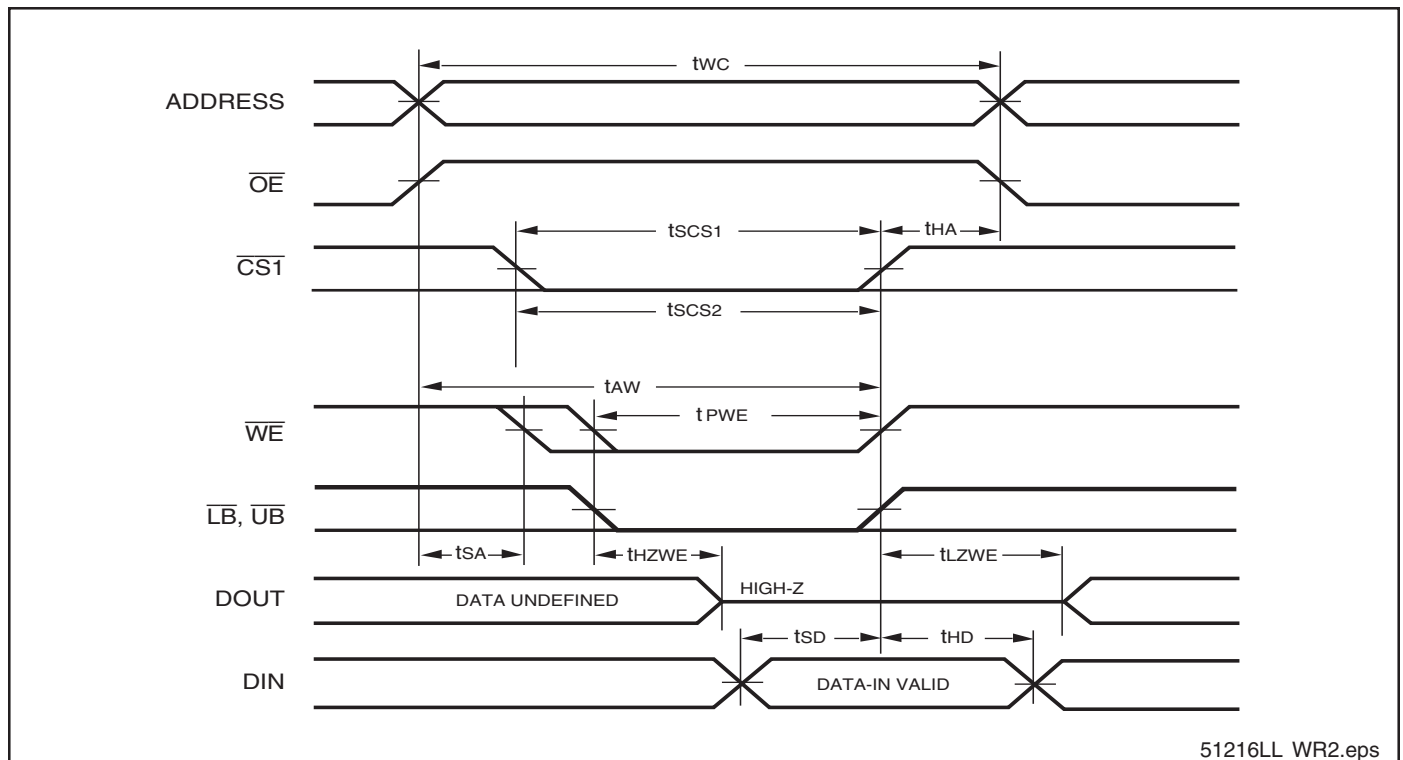
WRITE CYCLE NO. 1^(1,2) ($\overline{CS1}$ Controlled, \overline{OE} = HIGH or LOW)



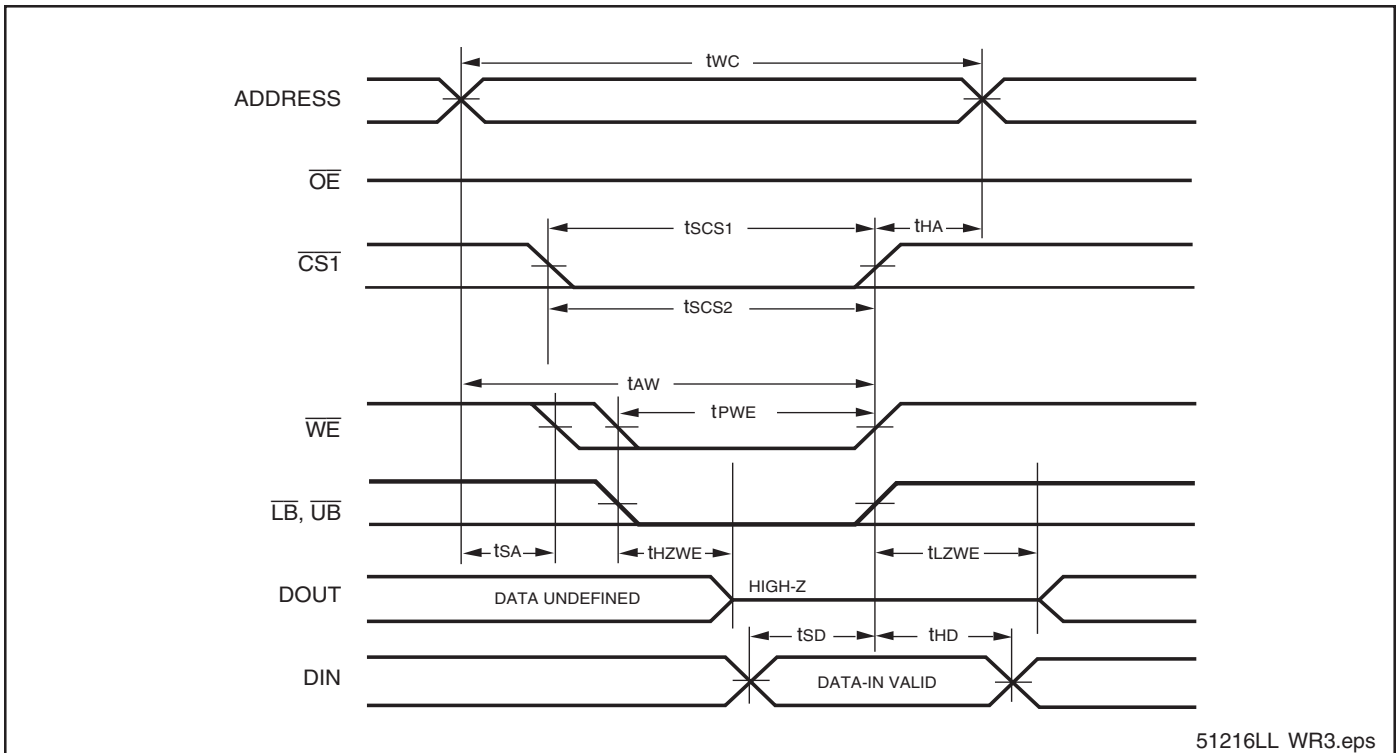
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, \overline{WE} inputs and at least one of the \overline{LB} and \overline{UB} inputs being in the LOW state.
2. $WRITE = (\overline{CS1}) [(\overline{LB}) = (\overline{UB})] (\overline{WE})$.

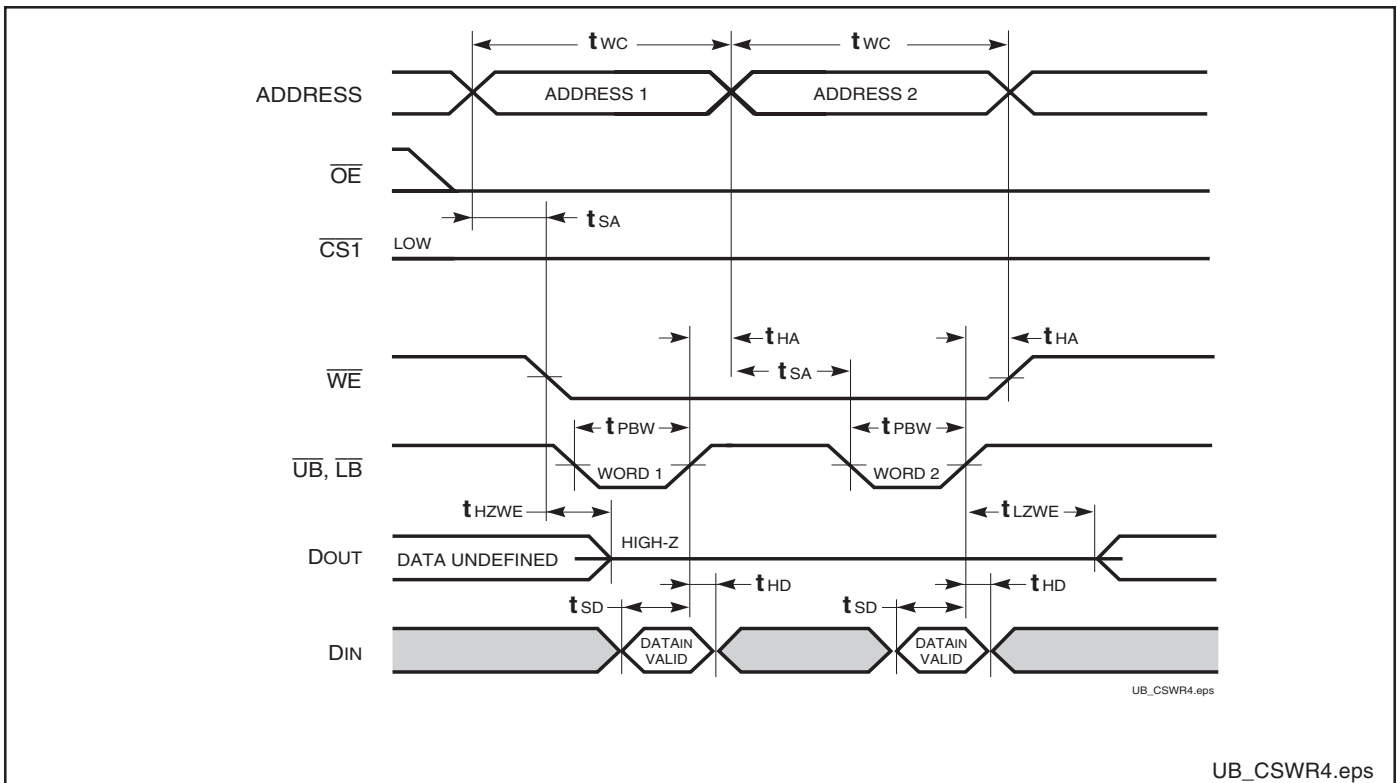
WRITE CYCLE NO. 2 (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)



WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)

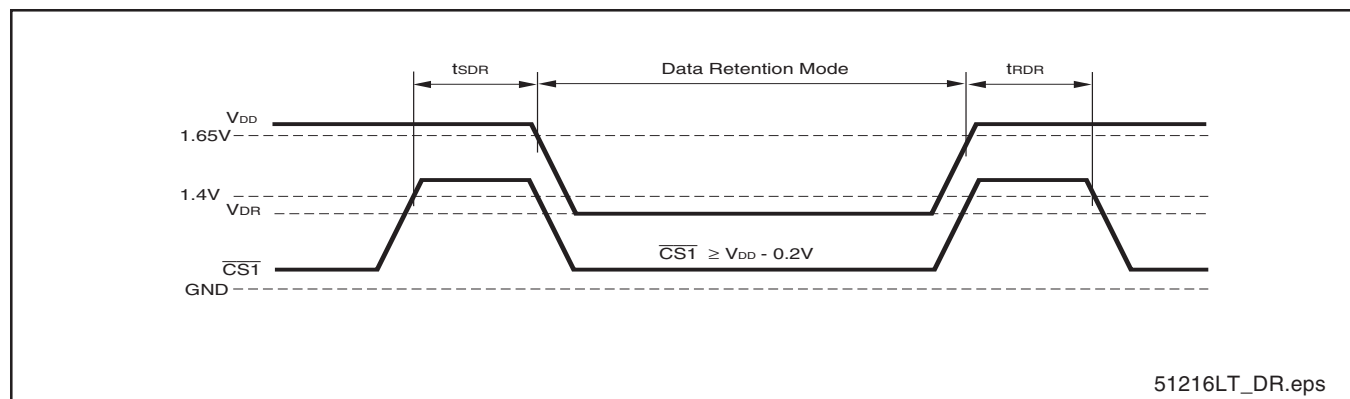


WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Controlled)



DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform	1.2	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 1.2V, $\overline{\text{CS1}} \geq V_{\text{DD}} - 0.2\text{V}$	A1 A2 A3	— 20 40 60	μA μA μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform	t _{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{\text{CS1}}$ Controlled)

ORDERING INFORMATION: IS65WV25616ALL (1.65V-2.2V)

Temperature Range (A1): -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616ALL-70TA1	44-pin TSOP-II

Temperature Range (A2): -40°C to +105°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616ALL-70TA2	44-pin TSOP-II

Temperature Range (A3): -40°C to +125°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616ALL-70TA3	44-pin TSOP-II

ORDERING INFORMATION: IS65WV25616BLL (2.5V-3.6V)

Temperature Range (A1): -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS65WV25616BLL-55TA1	44-pin TSOP-II
	IS65WV25616BLL-55TLA1	44-pin TSOP-II, Lead-free

Temperature Range (A2): -40°C to +105°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616BLL-70TA2	44-pin TSOP-II

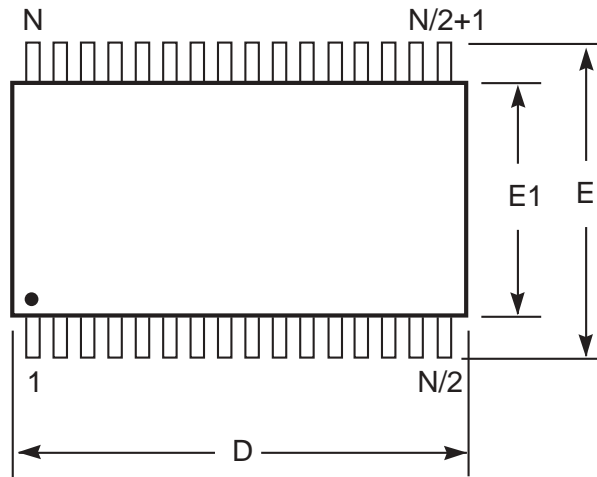
Temperature Range (A3): -40°C to +125°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616BLL-70TA3	44-pin TSOP-II

PACKAGING INFORMATION

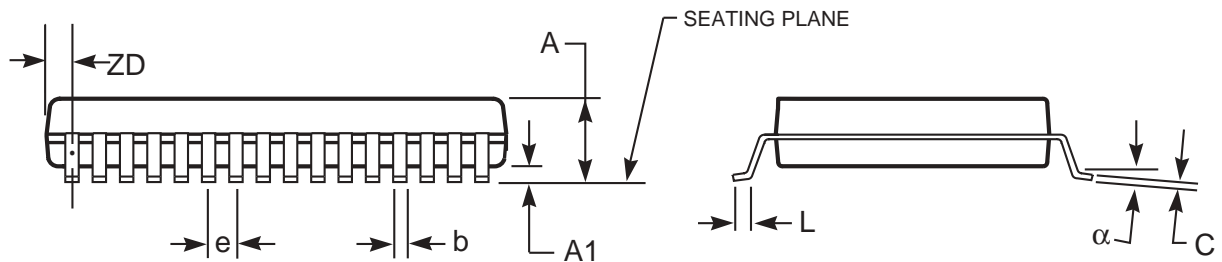


Plastic TSOP Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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