

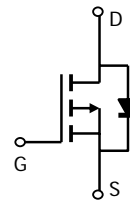
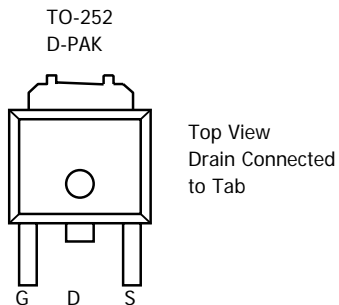
**AOD419**  
**P-Channel Enhancement Mode Field Effect Transistor**

**General Description**

The AOD419 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications. *Standard Product AOD419 is Pb-free (meets ROHS & Sony 259 specifications). AOD419L is a Green Product ordering option. AOD419 and AOD419L are electrically identical.*

**Features**

$V_{DS} (V) = -40V$   
 $I_D = -20A \quad (V_{GS} = -10V)$   
 $R_{DS(ON)} < 40m\Omega \quad (V_{GS} = -10V)$   
 $R_{DS(ON)} < 65m\Omega \quad (V_{GS} = -4.5V)$


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B,G</sup>	$T_A=25^\circ C$ <sup>G</sup>	-20	A
	$T_A=100^\circ C$	-18	
Pulsed Drain Current	$I_{DM}$	-60	
Avalanche Current <sup>C</sup>	$I_{AR}$	-20	A
Repetitive avalanche energy $L=0.3mH$ <sup>C</sup>	$E_{AR}$	60	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ C$	50	W
	$T_C=100^\circ C$	25	
Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	2.5	W
	$T_A=70^\circ C$	1.6	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	16.7	25	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	40	50
Maximum Junction-to-Case <sup>C</sup>	$R_{\theta JL}$	2.5	3	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-10mA, V <sub>GS</sub> =0V	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-2.2	-3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-60			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A T <sub>J</sub> =125°C		33 45	40 54	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A		52	65	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A		16		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.75	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-20	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-20V, f=1MHz		657	850	pF
C <sub>oss</sub>	Output Capacitance			143	185	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			63	90	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		6.5		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge (10V)	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-20A		14.1		nC
Q <sub>g</sub> (4.5V)	Total Gate Charge (4.5V)			7		nC
Q <sub>gs</sub>	Gate Source Charge			2.2		nC
Q <sub>gd</sub>	Gate Drain Charge			4.1		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω		8		ns
t <sub>r</sub>	Turn-On Rise Time			12.2		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			24		ns
t <sub>f</sub>	Turn-Off Fall Time			12.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =-20A, dI/dt=100A/μs		23.2	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-20A, dI/dt=100A/μs		18.2		nC

A: The value of R θJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation PDSM is based on R θJA and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation PD is based on T<sub>J</sub>(MAX)=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J</sub>(MAX)=175°C.

D: The R θJA is the sum of the thermal impedance from junction to case R θJC and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J</sub>(MAX)=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

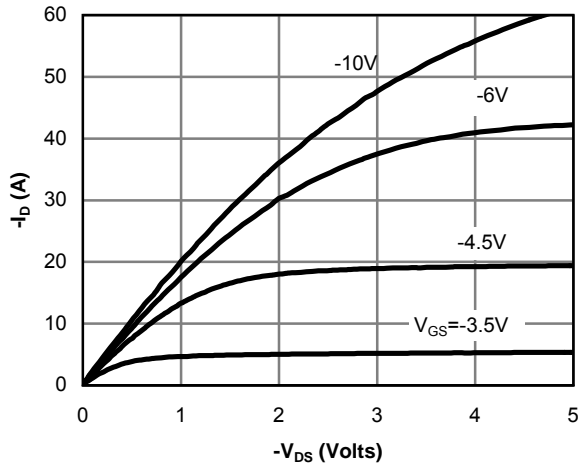


Figure 1: On-Region Characteristics

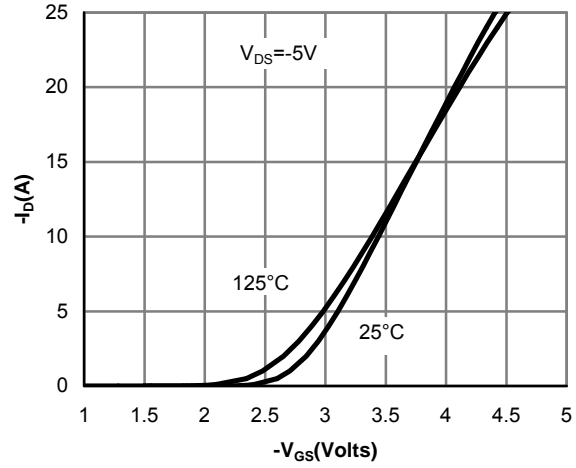


Figure 2: Transfer Characteristics

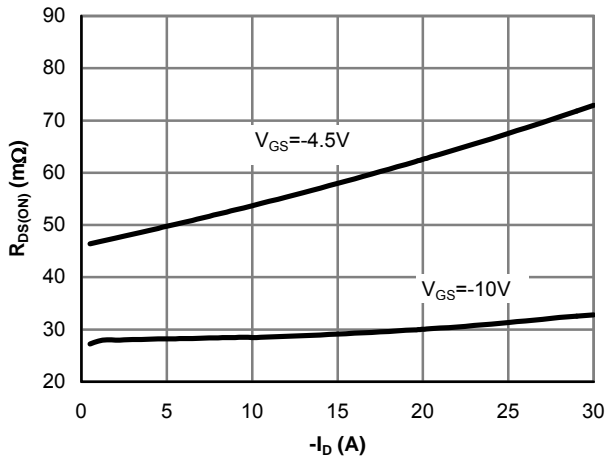


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

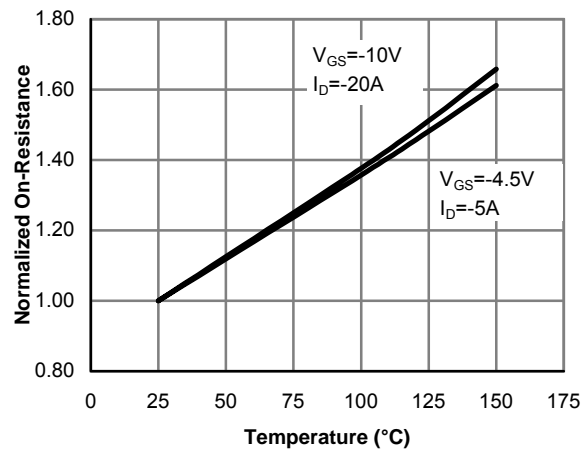


Figure 4: On-Resistance vs. Junction Temperature

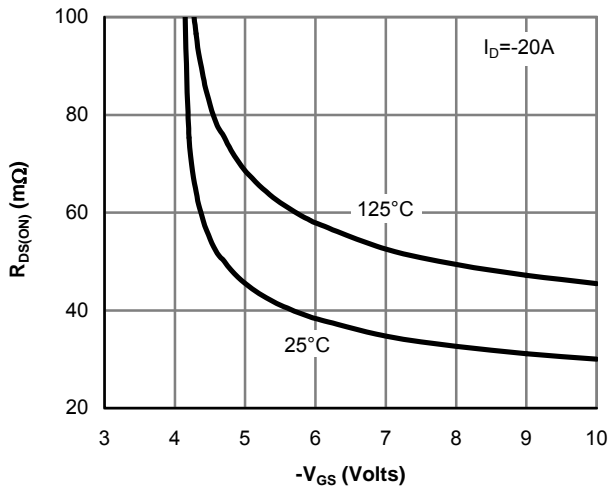


Figure 5: On-Resistance vs. Gate-Source Voltage

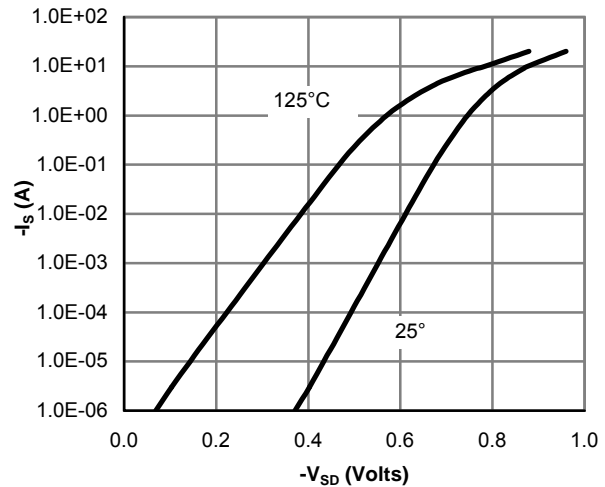


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

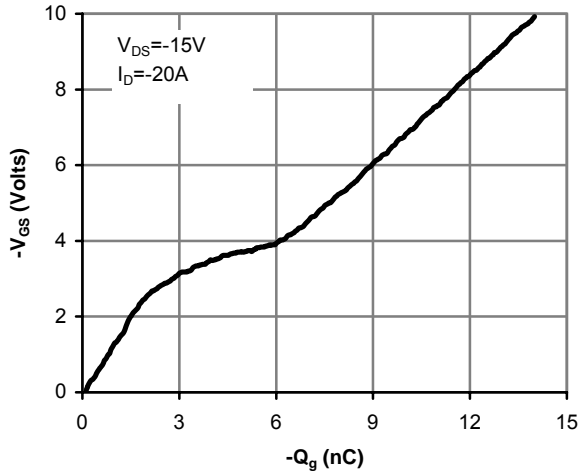


Figure 7: Gate-Charge Characteristics

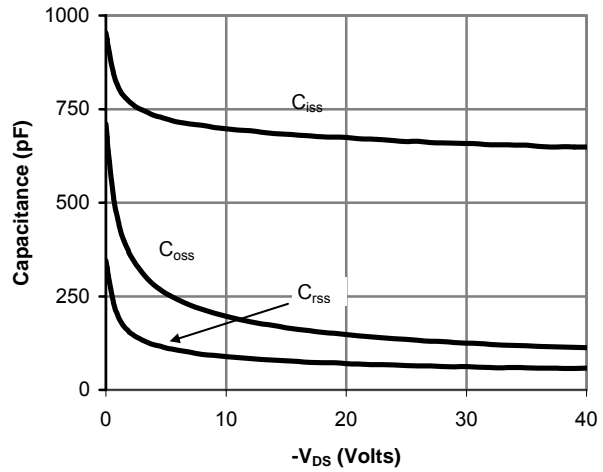


Figure 8: Capacitance Characteristics

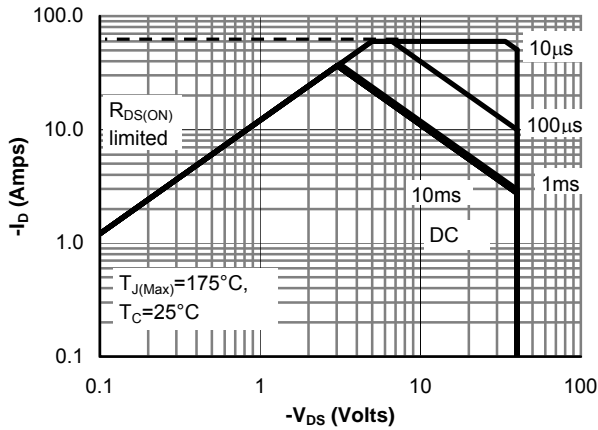


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

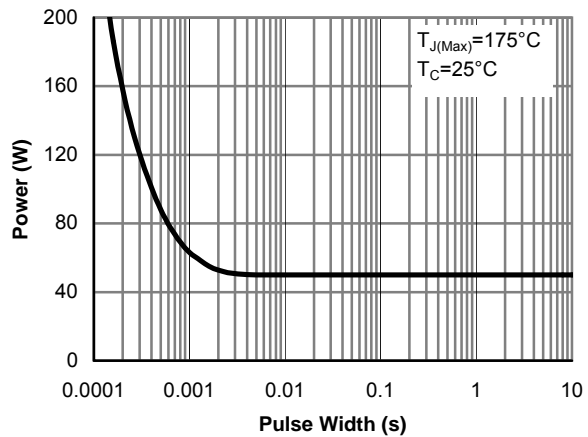


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

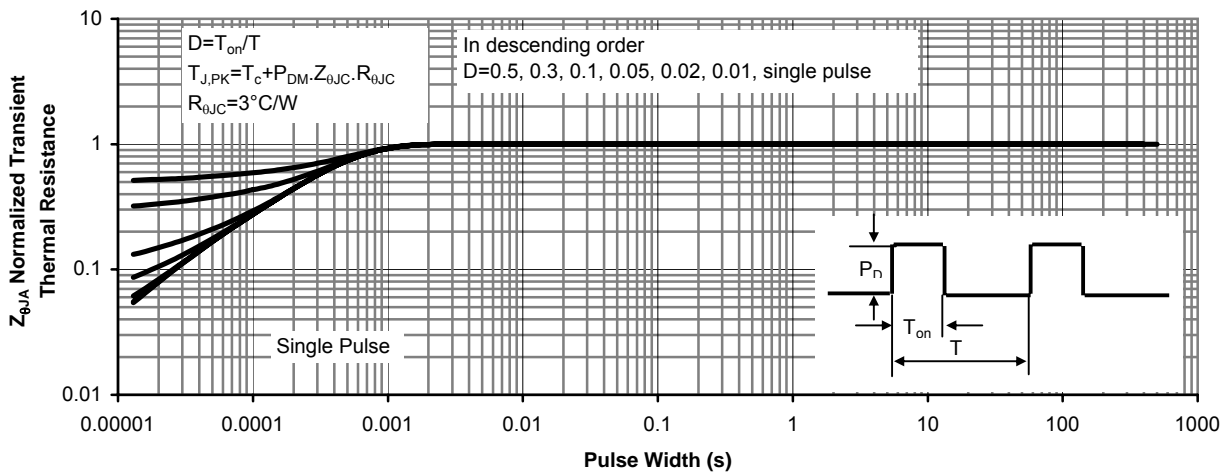


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

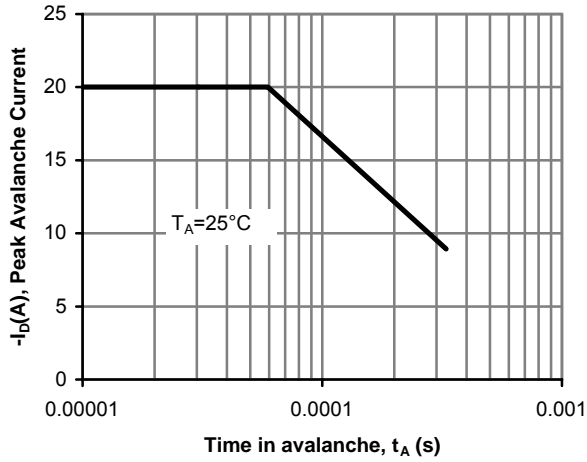


Figure 12: Single Pulse Avalanche capability

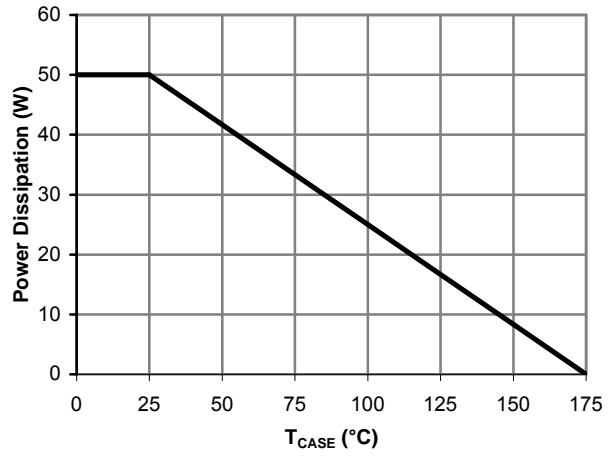


Figure 13: Power De-rating (Note B)

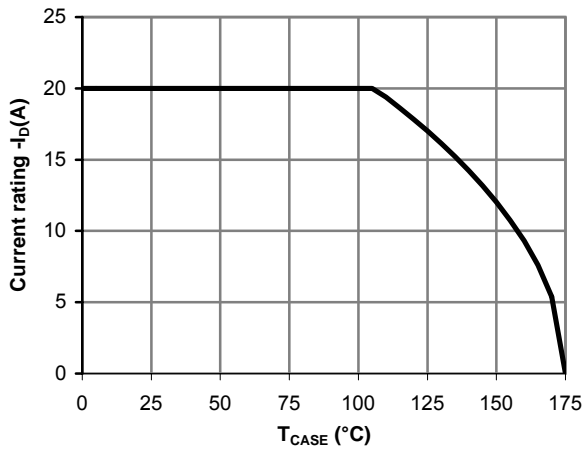


Figure 14: Current De-rating (Note B)

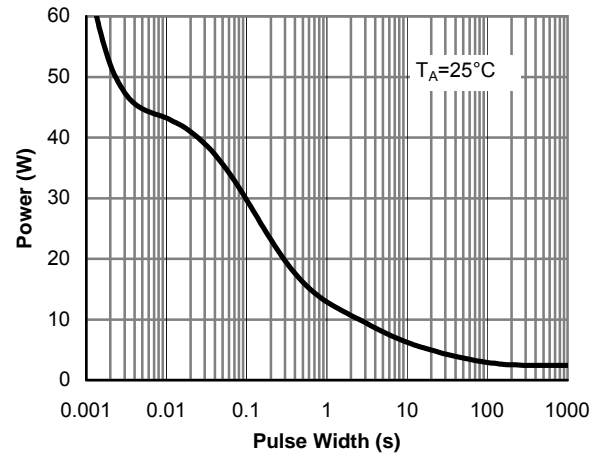


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

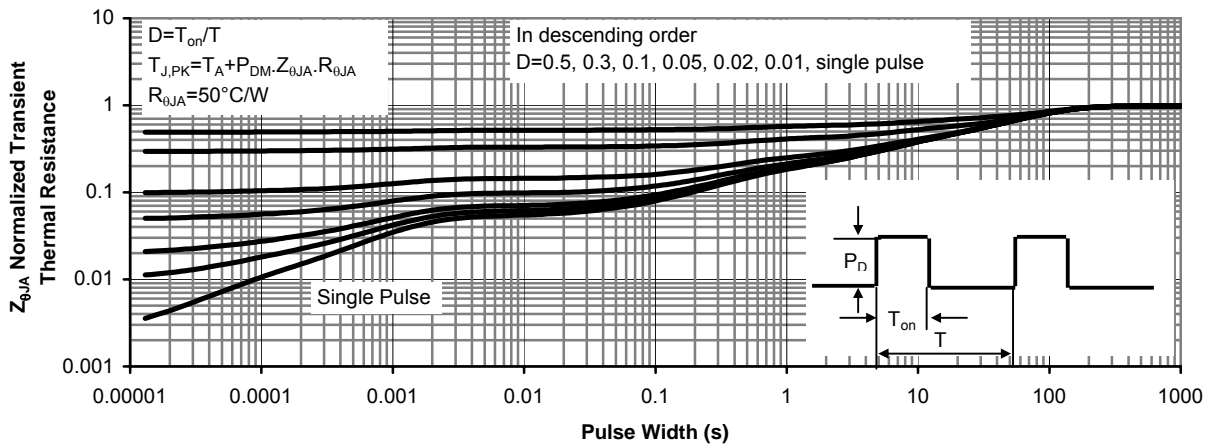


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)