FLASH-ROM MODULE 8MByte (8M x 8-Bit)
Part No. HMF8M8M4G

GENERAL DESCRIPTION

The HMF8M8M4G is a high-speed flash read only memory (FROM) module containing 8,388,608 words organized in a x8bit configuration. The module consists of four 2M x 8 FROM mounted on a 72-pin, single-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.
Four chip enable inputs, (/CE1, /CE2, /CE3, /CE4) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output.
When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Part identification
  - HMF8M8M4 (Solder Plating Lead)
  - HMF8M8M4G (Gold Plating Lead)
- Access time : 70, 90, 120ns
- High-density 8MByte design
- High-reliability, low-power design
- Single + 5V ± 0.5V power supply
- Easy memory expansion
- All inputs and outputs are TTL-compatible
- FR4-PCB design
- Low profile 72-pin SIMM
- Minimum 1,000,000 write/erase cycle
- Flexible sector architecture
- Embedded algorithms
- Erase suspend / Erase resume

OPTIONS MARKING

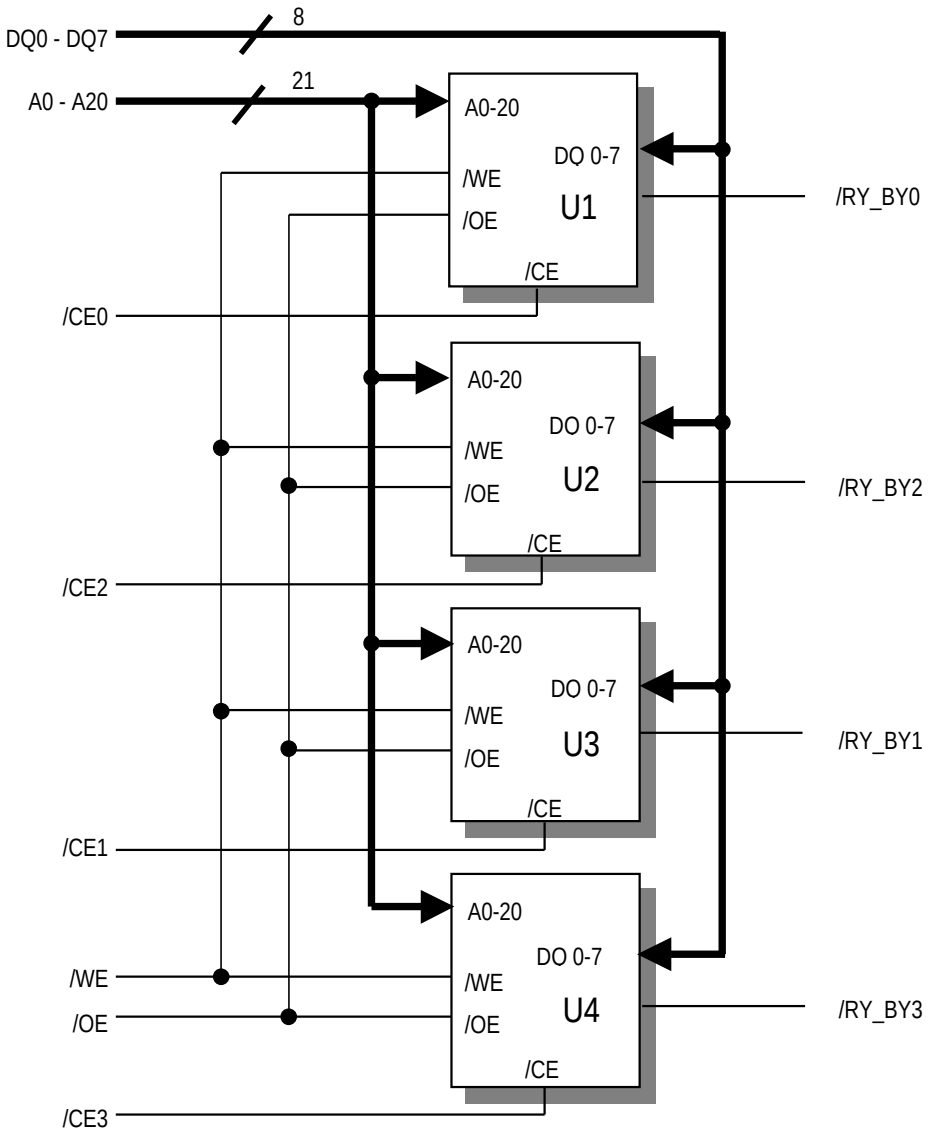
- Timing
  - 70ns access - 70
  - 90ns access - 90
  - 120ns access -120
- Packages
  - 72-pin SIMM M

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	A15	49	NC
2	/CE0	26	A16	50	NC
3	/CE1	27	A17	51	NC
4	/CE2	28	A18	52	NC
5	/CE3	29	A19	53	NC
6	Vcc	30	Vcc	54	NC
7	/WE	31	A20	55	NC
8	/OE	32	DQ0	56	NC
9	/RESET	33	DQ1	57	NC
10	A0	34	DQ2	58	NC
11	A1	35	DQ3	59	Vcc
12	A2	36	DQ4	60	NC
13	A3	37	DQ5	61	NC
14	A4	38	DQ6	62	NC
15	A5	39	Vss	63	Vss
16	A6	40	DQ7	64	NC
17	A7	41	/RY_BY0	65	NC
18	A8	42	/RY_BY1	66	NC
19	A9	43	/RY_BY2	67	NC
20	A10	44	Vcc	68	NC
21	A11	45	/RY_BY3	69	NC
22	A12	46	NC	70	NC
23	A13	47	NC	71	NC
24	A14	48	NC	72	Vss

72-PIN SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE	X	L	L	Din	ACTIVE

Note : X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-2.0V to +7.0V
Voltage with respect to ground Vcc	V_{CC}	-2.0V to +7.0V
Storage Temperature	T_{STG}	-65°C to +125°C
Operating Temperature	T_A	-55°C to +125°C
Power Dissipation	P_D	4W

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for ± 10% device Supply Voltages	Vcc	4.5V		5.5V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0^oC \le T_A \le 70\ ^oC$; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	Vcc=Vcc max, V_{IN}= GND to Vcc	I_{L1}		±1.0	µA
Output Leakage Current	Vcc=Vcc max, VOUT= GND to Vcc	I_{L0}		±1.0	µA
Output High Voltage	I_{OH} = -2.5mA, Vcc = Vcc min	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 12mA, Vcc =Vcc min	V_{OL}		0.45	V
Vcc Active Current for Read(1)	/CE = V_{IL}, /OE=V_{IH},	I_{CC1}		40	mA
Vcc Active Current for Program or Erase(2)	/CE = V_{IL}, /OE=V_{IH}	I_{CC2}		60	mA
Vcc Standby Current	/CE= V_{IH}	I_{CC3}		1.0	mA
Low Vcc Lock-Out Voltage		V_{LKO}	3.2	4.2	V

Notes:

1. The Icc current listed is typically less than 2mA/MHz, with /OE at V_{IH}.
2. Icc active while embedded algorithm (program or erase) is in progress
3. Maximum Icc current specifications are tested with Vcc=Vcc max

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	1	8	sec	Excludes 00H programming prior to erasure

Byte Programming Time	-	7	300	μs	Excludes system-level overhead
Chip Programming Time	-	14.4	43.2	sec	Excludes system-level overhead

TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : Test conditions T_A = 25° C, f=1.0 MHz.

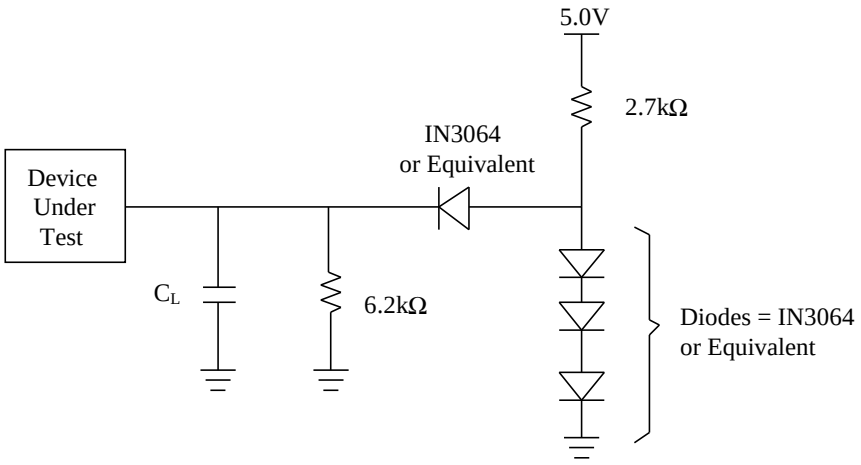
AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		-75	-90	UNIT
JEDEC	STANDARD						
t_{AVAV}	t_{RC}	Read Cycle Time		Min	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	/CE = V_{IL} /OE = V_{IL}	Max	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	/OE = V_{IL}	Max	70	90	ns
t_{GLQV}	t_{OE}	Chip Enable to Output Delay		Max	40	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max	20	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max	20	20	ns
t_{AXQX}	t_{QH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0	0	ns

TEST SPECIFICATIONS

TEST CONDITION	ALL SPEED OPTIONS	UNIT
Output load	1TTL gate	
Output load capacitance, C_L (Including jig capacitance)	100	pF
Input rise and full times	20	ns
Input pulse levels	0.45-2.4	V
Input timing measurement reference levels	0.8	V
Output timing measurement reference levels	2.0	V



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-75	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0	0	ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	1	1	sec
	t_{VCS}	Vcc set up time	Min	50	50	µs

Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

u Erase/Program Operations

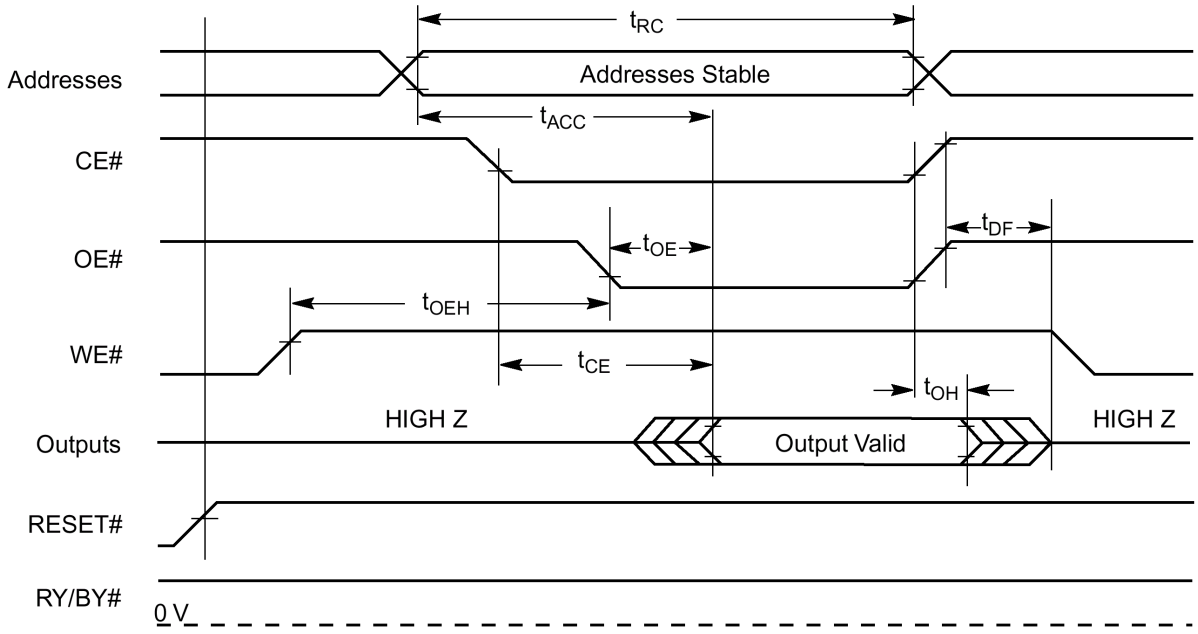
Alternate /CE Controlled Writes

PARAMETER SYMBOLS		DESCRIPTION		-75	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0	0	ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	1	1	sec

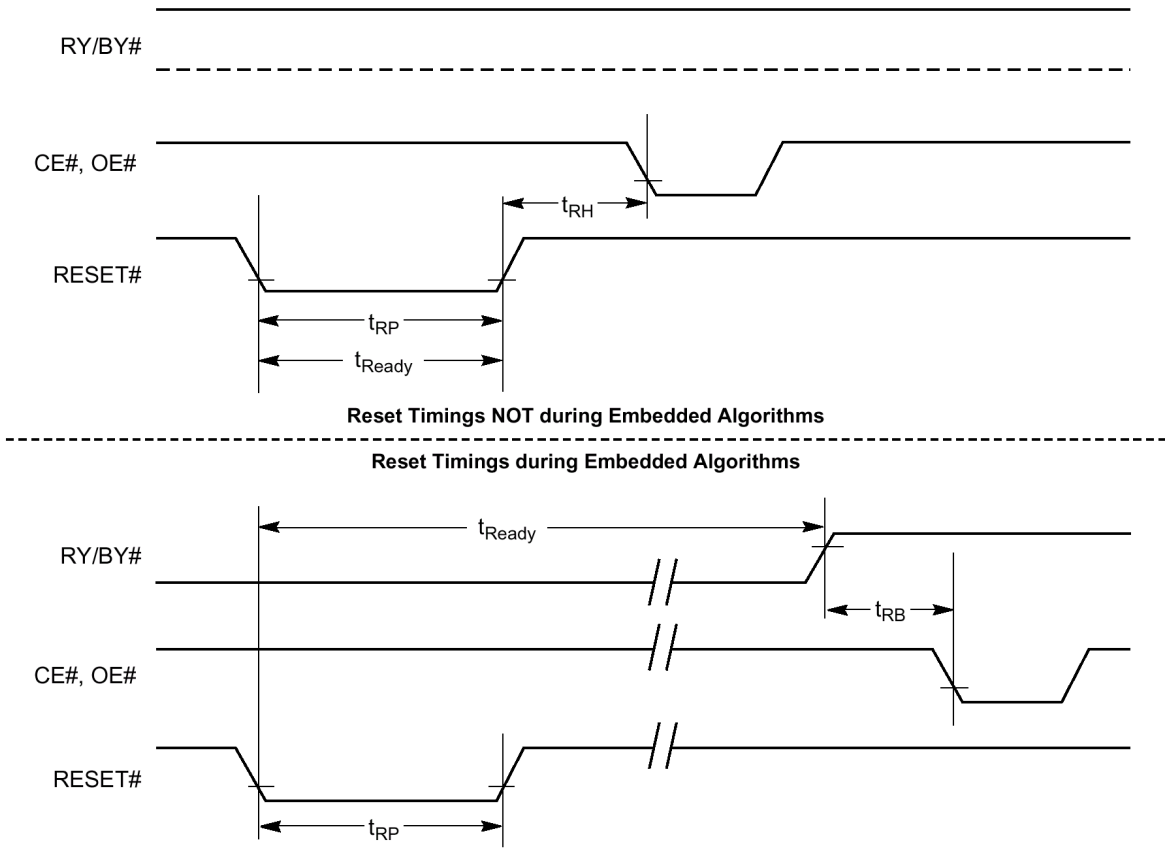
Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

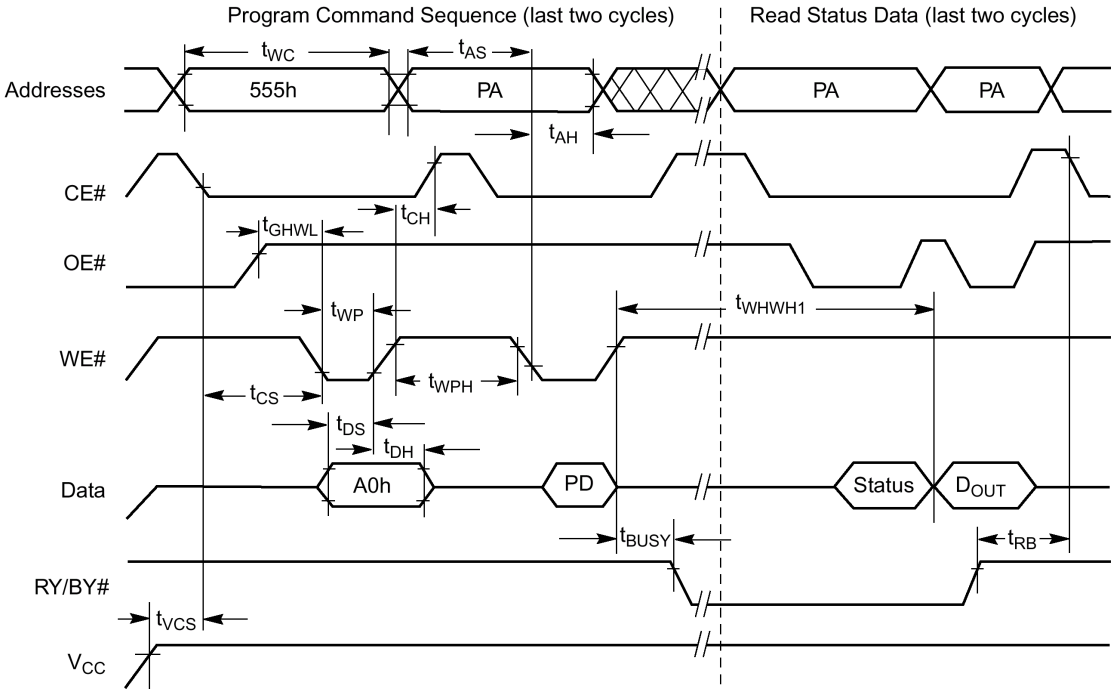
u READ OPERATIONS TIMING



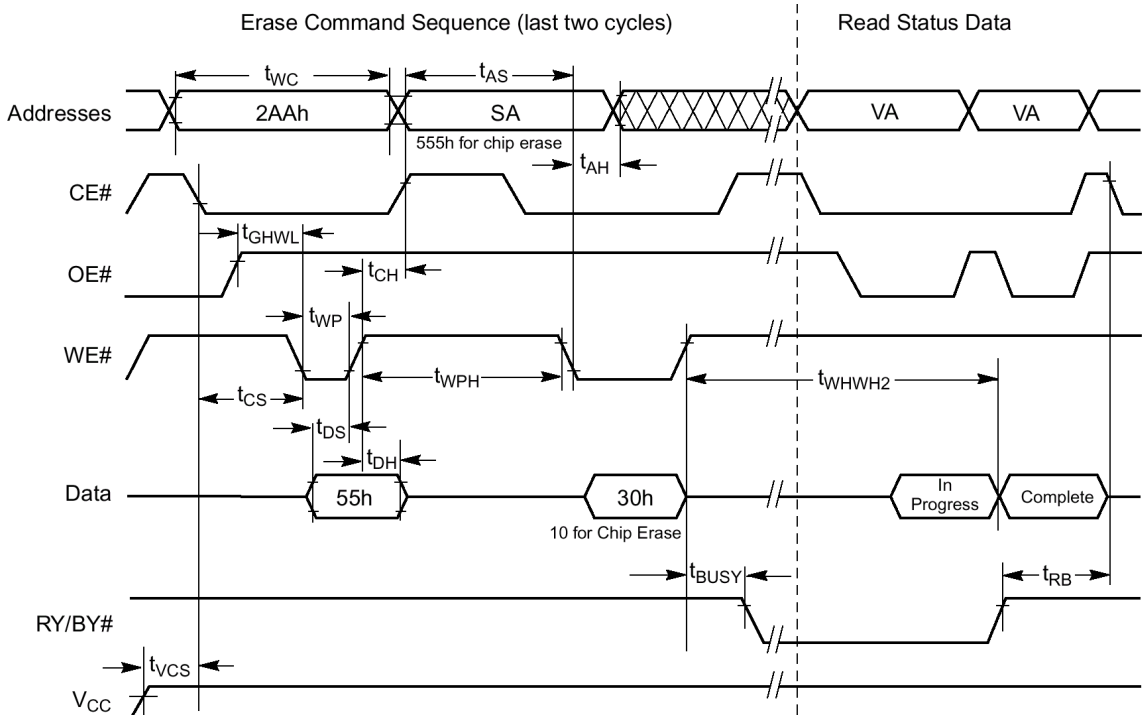
u RESET TIMING



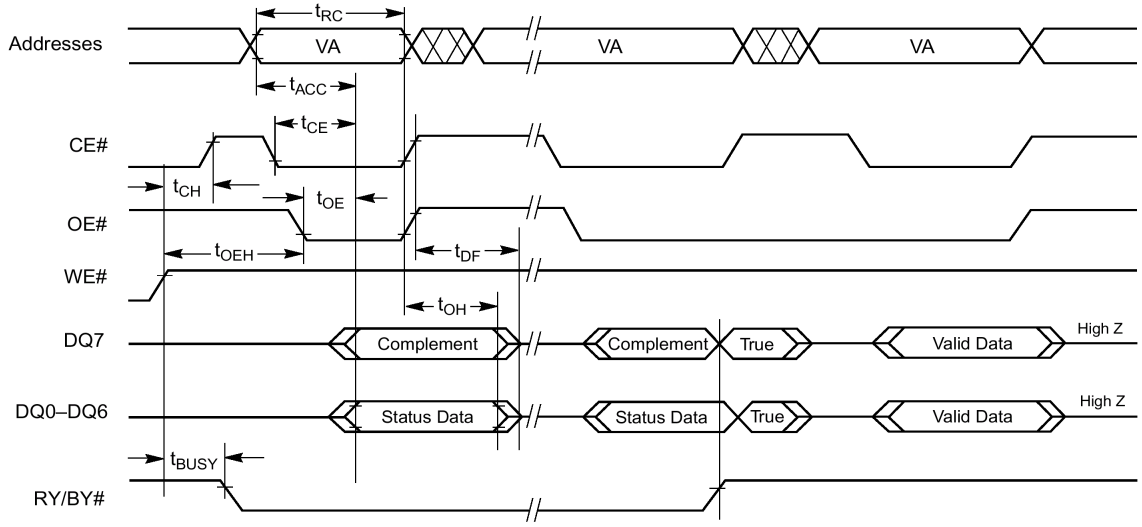
u PROGRAM OPERATIONS TIMING



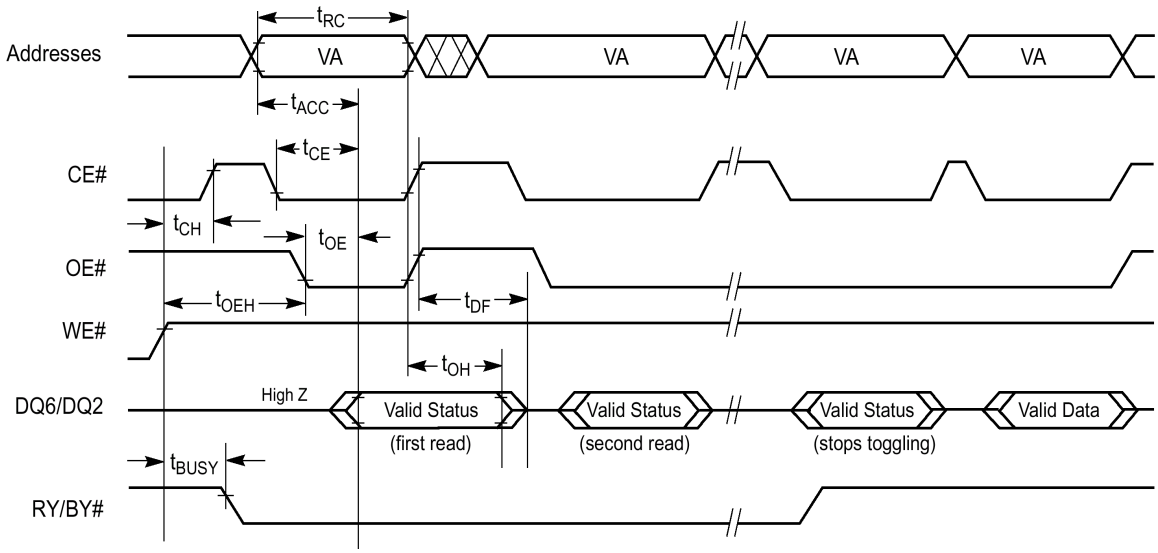
u CHIP/SECTOR ERASE OPERATION TIMINGS



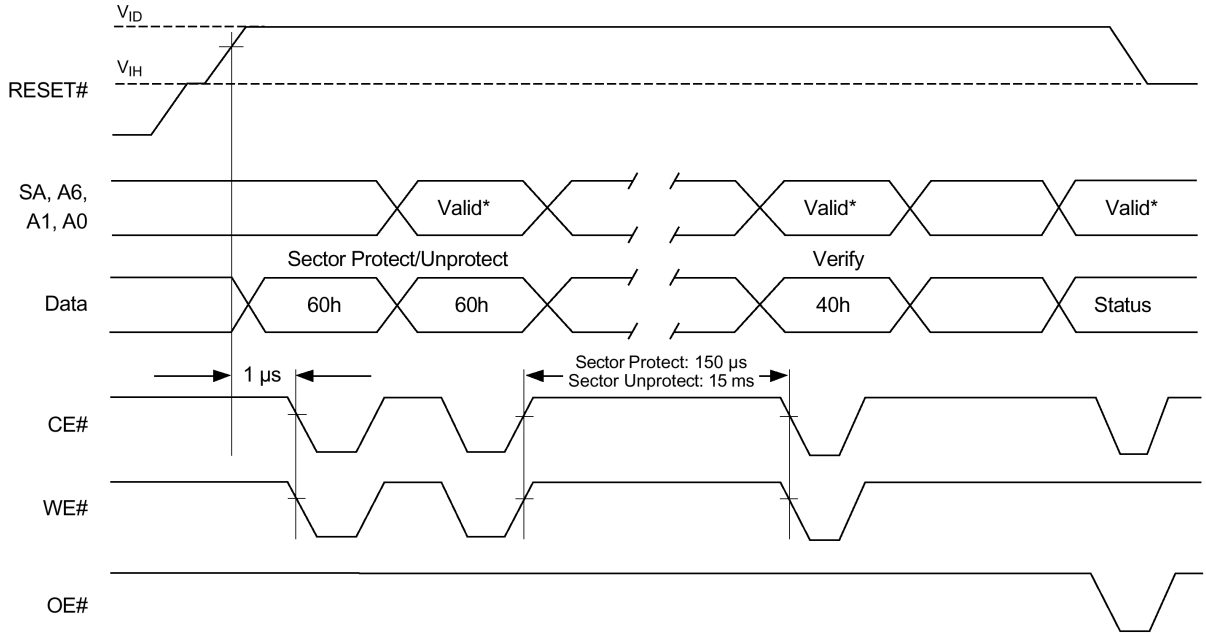
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



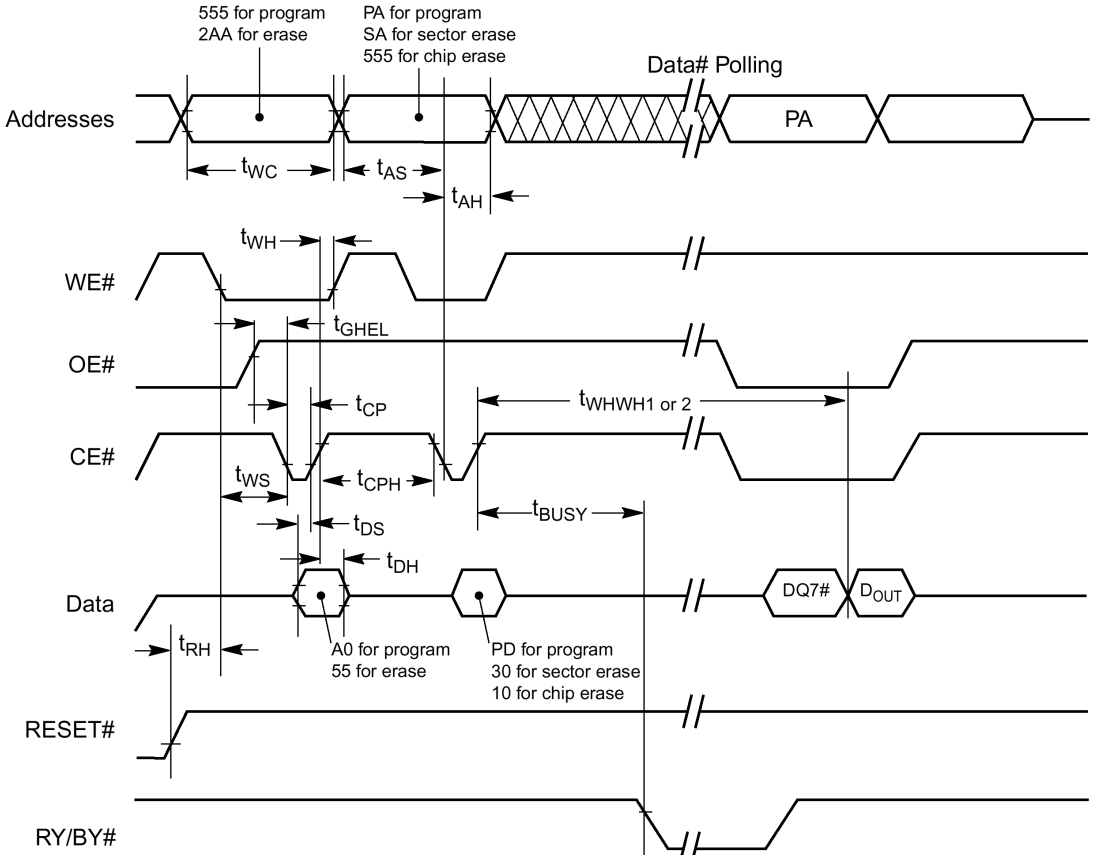
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



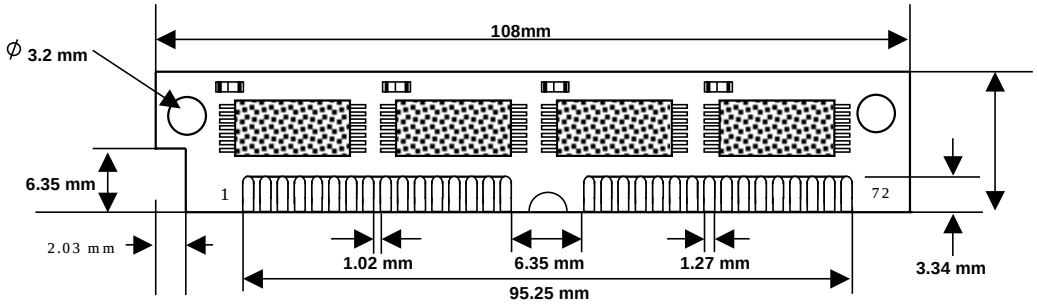
u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

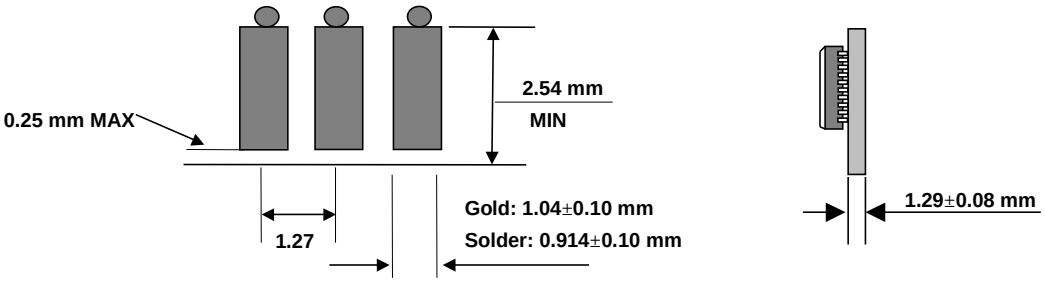


u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS





(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF8M8M4G-70	8MByte	8M X 8bit	72 Pin-SIMM	4EA	5V	70ns
HMF8M8M4G-90	8MByte	8M X 8bit	72 Pin-SIMM	4EA	5V	90ns
HMF8M8M4G-120	8MByte	8M X 8bit	72 Pin-SIMM	4EA	5V	120ns