FLASH-ROM MODULE 2MByte (512K x 32-Bit)
Part No. HMF51232M4V

GENERAL DESCRIPTION

The HMF51232M4V is a high-speed flash read only memory (FROM) module containing 524,288 words organized in a x32bit configuration. The module consists of four 512Kx 8 FROM mounted on a 72-pin, single-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.
Four chip enable inputs, (/CE_UU1, /CE_UM1, /CE_LM1, /CE_LL1) are used to enable the module's 4 bytes independently.
Output enable (/OE) and write enable (/WE) can set the memory input and output.
When FROM module is disable condition, the module is becoming power standby mode, system designer can get low-power design.
All module components may be powered from a single +3V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Access time : 55,70, 90 and 120ns
- High-density 2MByte design
- High-reliability, low-power design
- Single + 3V ± 0.3V power supply
- Easy memory expansion
- All inputs and outputs are TTL- compatible
- FR4-PCB design
- Low profile 72-pin SIMM
- Minimum 1,000,000 write/erase cycle
- Sector erases architecture
- Sector group protection
- Temporary sector group unprotection
- Part Identification

  HMF51232M4V : Gold Plate Lead

OPTIONS MARKING

- Timing

55ns access	- 55
70ns access	- 70
90ns access	- 90
120ns access	- 120

- Package

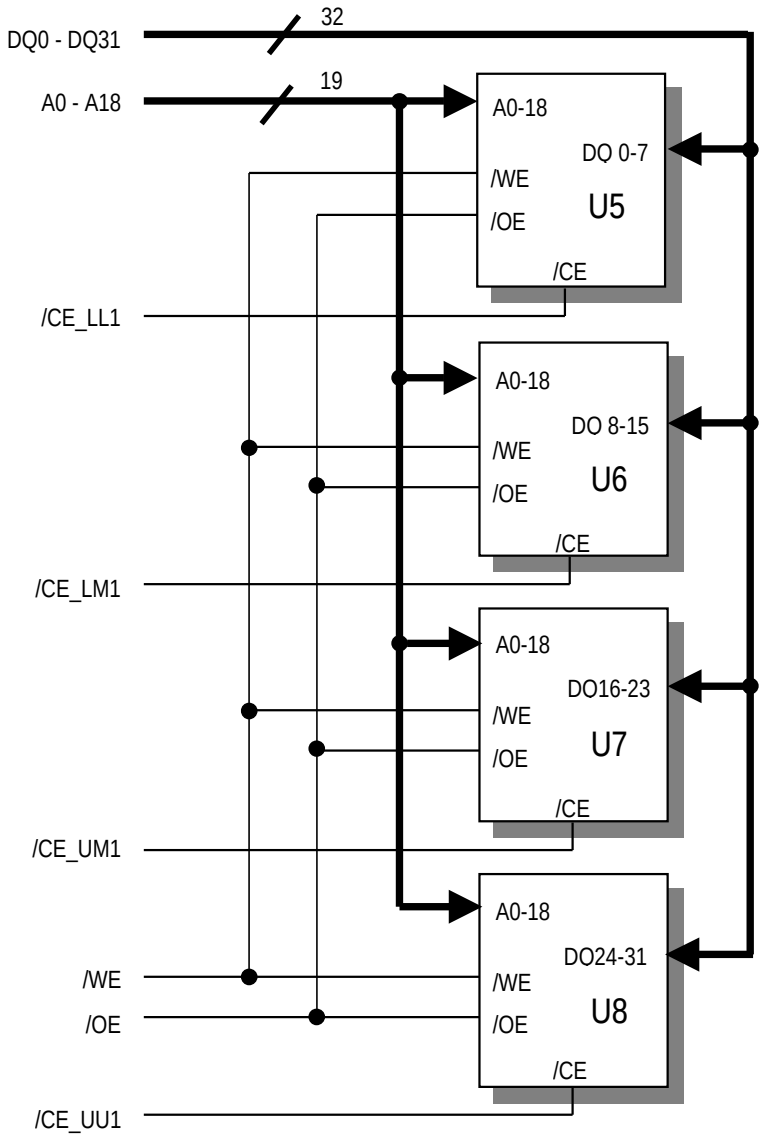
72-pin SIMM	M

FUNCTIONAL BLOCK DIAGRAM

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	Vcc	49	DQ17
2	A3	26	DQ8	50	DQ18
3	A2	27	DQ9	51	DQ22
4	A1	28	DQ10	52	DQ21
5	A0	29	NC	53	DQ20
6	Vcc	30	Vcc	54	DQ19
7	A11	31	/CE_LM1	55	Vcc
8	/OE	32	DQ15	56	A15
9	A10	33	DQ14	57	A12
10	Vcc	34	DQ13	58	A7
11	NC	35	DQ12	59	Vcc
12	/CE_LL1	36	DQ11	60	A8
13	DQ7	37	A18	61	A9
14	DQ0	38	A16	62	DQ24
15	DQ1	39	Vss	63	DQ25
16	DQ2	40	A6	64	DQ26
17	DQ6	41	Vcc	65	NC
18	DQ5	42	A5	66	/CE_UU1
19	DQ4	43	A4	67	DQ31
20	DQ3	44	Vcc	68	DQ30
21	/WE	45	NC	69	DQ29
22	A17	46	/CE_UM1	70	DQ28
23	A14	47	DQ23	71	DQ27
24	A13	48	DQ16	72	Vss

72-PIN SIMM
TOP VIEW



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE	X	L	L	Din	ACTIVE

Note : X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-0.5V to V_{CC} + 7.0V
Voltage with respect to ground Vcc	V_{CC}	-0.5V to + 4.0V
Power Dissipation	Po	4W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	-55°C to +125°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for ±5% device Supply Voltages	V_{CC}	4.75V		5.25V
Vcc for ± 10% device Supply Voltages	Vcc	4.5V		5.5V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0°C \le T_A \le 70°C$; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS
Input Load Current	Vcc=Vcc max, V_{IN}= Vss to Vcc		I_{LI}			±1.0	µA
A9 Input Load Current	Vcc=Vcc max; A9 = 12.5V		I_{LIT}			35	µA
Output Leakage Current	Vcc=Vcc max, VOUT= Vss to Vcc		I_{L0}			±1.0	µA
Vcc Active Read Current	/CE=V_{IL}, /OE=V_{IH},	5 MHz	I_{CC1}		28	48	mA
		1 MHz			8	16	
Vcc Active Write Current	/CE = V_{IL}, /OE=V_{IH}		I_{CC2}		60	120	mA
Vcc Standby Current	/CE= V_{CC}±0.3V		I_{CC3}		0.8	20	µA
Vcc Reset Current			I_{CC4}		0.8	20	µA
Automatic Sleep Mode	V_{IH} = Vcc±0.3V; V_{IL} = Vss±0.3V		I_{CC5}		0.2	5	µA
Input Low Voltage			V_{IL}	-0.5		0.8	V
Input High Voltage			V_{IH}	0.7×Vcc		Vcc+0.3	V
Voltage for Autoselect and Temporary Sector Unprotect	Vcc= 3.3V		V_{ID}	11.5		12.5	V
Output Low Voltage	I_{OL} = 4.0 mA, Vcc =Vcc min		V_{OL}			0.45	V
Output High Voltage	$I_{OH=}$ -0.2 mA, Vcc=Vcc min		V_{OH1}	0.85Vcc			V
	$I_{OH=}$ -100µA, Vcc=Vcc min		V_{OH2}	Vcc-0.4			
Low Vcc Lock-Out Voltage			V_{LKO}	2.3		2.5	V

Notes:

1. The Icc current listed is typically less than 2mA/MHz, with /OE at V_{IH}.

2. Maximum Icc currnet specifications are tested with $V_{cc=}$ V_{cc} max.
3. Icc active while Embedded Erase of Embedded Program is in progress.
4. Not 100%tested.
5. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} +30 ns.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	MIN	TPYP	MAX	UNIT	COMMENTS
Sector Erase Time	-	0.7	15	sec	Excludes 00h programming prior to erasure
Chip Erase Time		11		sec	
Byte Programming Time	-	9	300	us	Excludes system-level overhead
Chip Programming Time	-	4.5	13.5	sec	

Notes:

1. Typical program and erase times assume the following conditions:25° C, 3.0V Vcc, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.
2. Under worst case conditions of 90°C, Vcc=2.7V(3.0V for-55R), 1,000,000cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. In the pre-programming step of th Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 4 for further information on command definitions.
6. The device has a minimum guaranteed erase and program cycle endurance of 1,000,000 cycles.

CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : Test conditions T_A = 25^o C, f=1.0 MHz.

TEST CONDITIONS

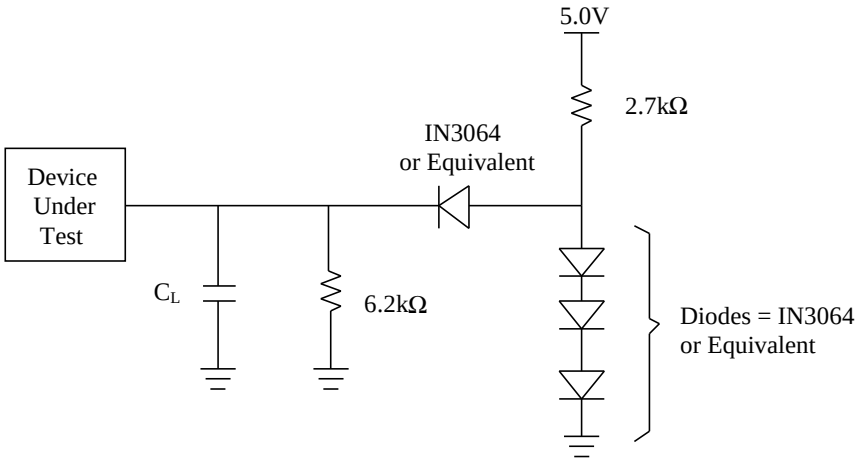
TEST CONDITION	-55R, -70	-90, -120	UNIT
Output load	1 TTL gate		
Output load Capacitance, C_L	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0~3		V
Input timing measurement reference levels	1.5		V

Output timing measurement reference levels	1.5	V

AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS	DESCRIPTION	TEST SETUP	-55		-70		-90		-120		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time		55		70		90		120		ns
t_{ACC}	Address to Output Delay	/CE = V_{IL} /OE = V_{IL}		55		70		90		120	ns
t_{CE}	Chip Enable to Output Delay	/OE = V_{IL}		55		70		90		120	ns
t_{OE}	Chip Enable to Output Delay			30		30		35		50	ns
t_{DF}	Chip Enable to Output High-Z			25		25		30		30	ns
t_{DF}	Output Enable to Output High-Z			25		25		30		30	ns
t_Q	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		0		0		0			0	ns



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETE	DESCRIPTION	-55	-70	-90	-120	UNIT

		MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55		70		90		120		ns
t_{AS}	Address Setup Time	0								ns
t_{AH}	Address Hold Time	45		45		45		50		ns
t_{DS}	Data Setup Time	35		35		45		50		ns
t_{DH}	Data Hold Time	0								ns
t_{OES}	Output Enable Setup Time	0								ns
t_{GHWL}	Read Recover Time Before Write	0								ns
t_{CS}	/CE Setup Time	0								ns
t_{CH}	/CE Hold Time	0								ns
t_{WP}	Write Pulse Width	35		35		35		50		ns
t_{WPH}	Write Pulse Width High	30								ns
t_{WHWH1}	Programming Operation	9								µs
t_{WHWH2}	Sector Erase Operation (Note1)	0.7								sec
t_{VCS}	Vcc set up time	50								µs

Notes :

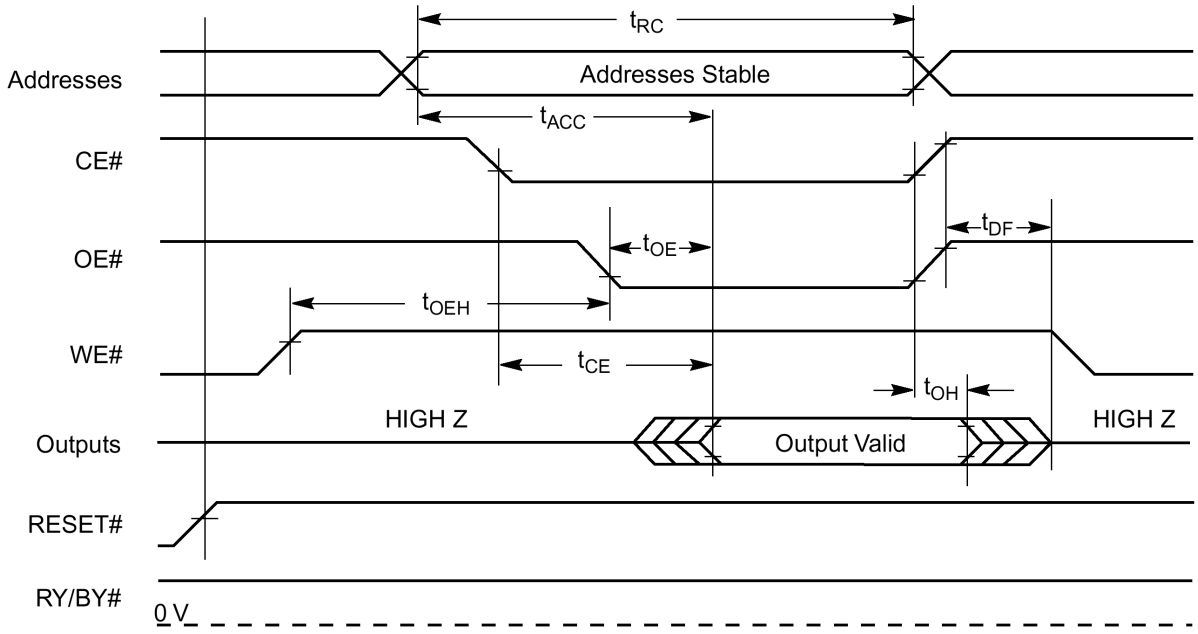
1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

u Erase/Program Operations
Alternate /CE Controlled Writes

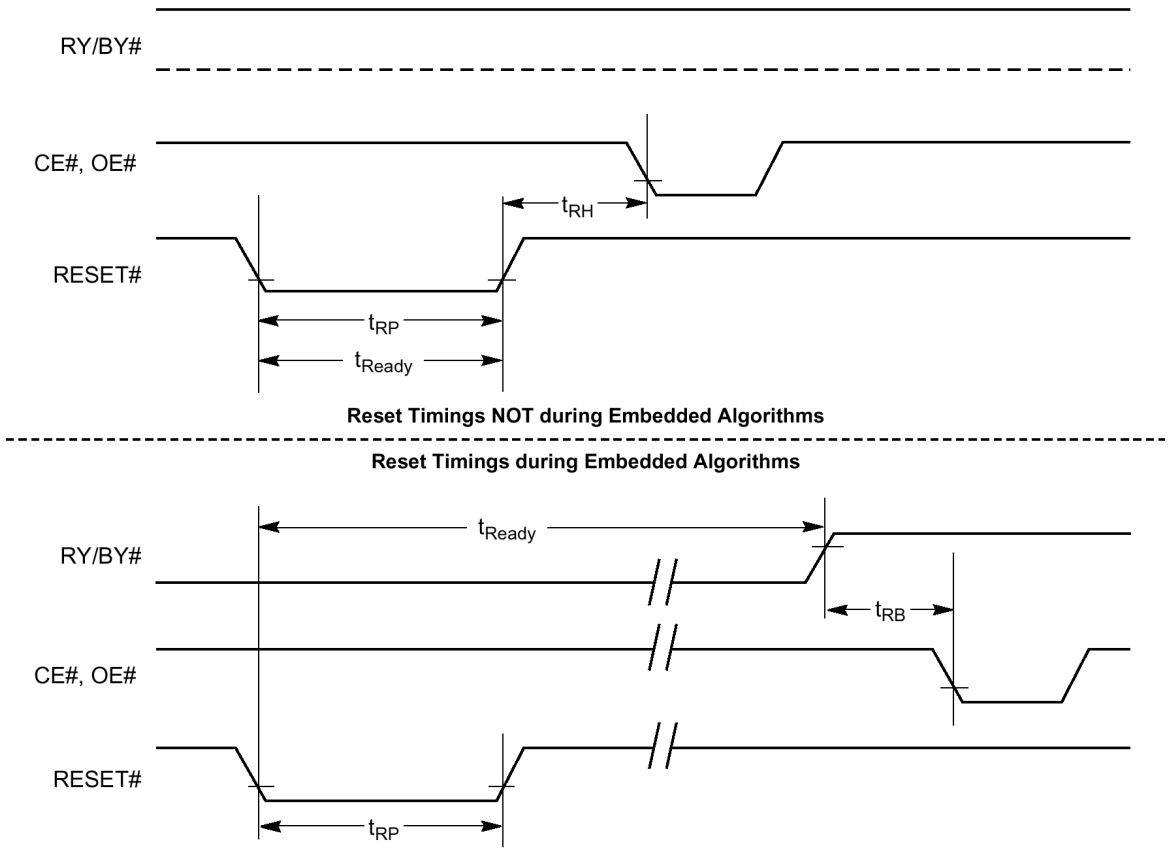
PARAMETER SYMBOLS	DESCRIPTION	-55		-70		-90		-120		UNIT
		MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55		70		90		120		ns
t_{AS}	Address Setup Time	0								ns
t_{AH}	Address Hold Time	40		45		45		50		ns
t_{DS}	Data Setup Time	35		35		35		50		ns
t_{DH}	Data Hold Time	0								ns
t_{GHEL}	Read Recover Time Before Write	0								ns
t_{WS}	/WE Setup Time	0								ns
t_{WH}	/WE Hold Time	0								ns
t_{CP}	/CE Pulse Width	35		35		45		50		ns
t_{CPH}	/CE Pulse Width High	30								ns
t_{WHWH1}	Programming Operation	9								µs
t_{WHWH2}	Sector Erase Operation (Note)	0.7								sec

Notes : This does not include the preprogramming time.

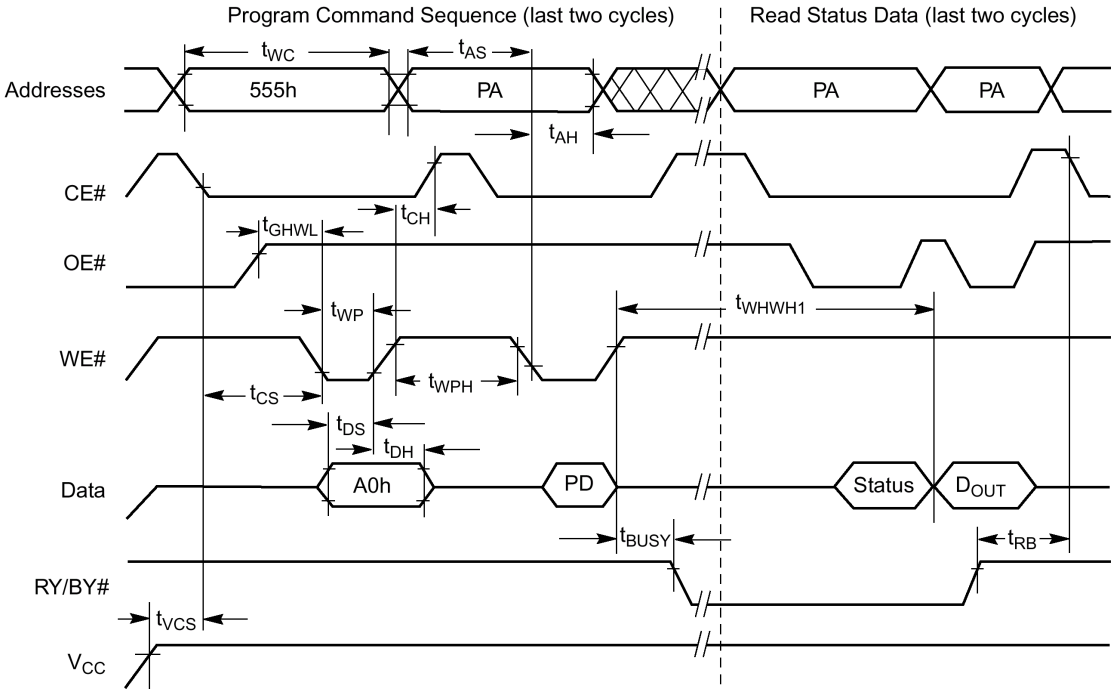
u READ OPERATIONS TIMING



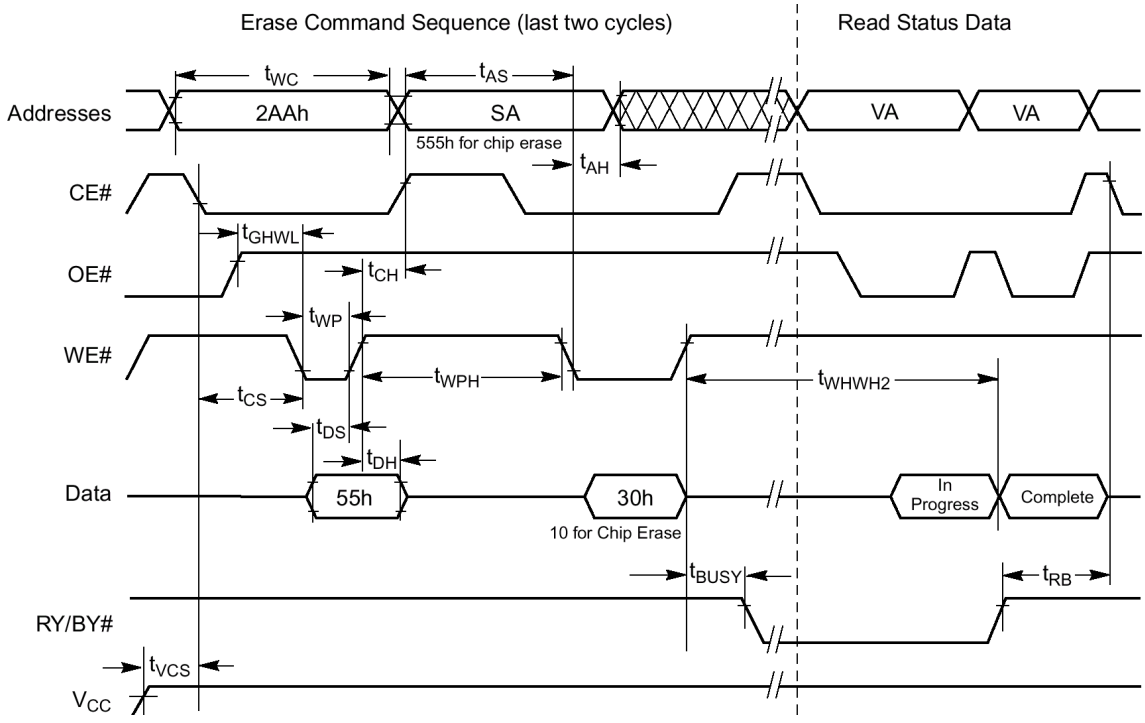
u RESET TIMING



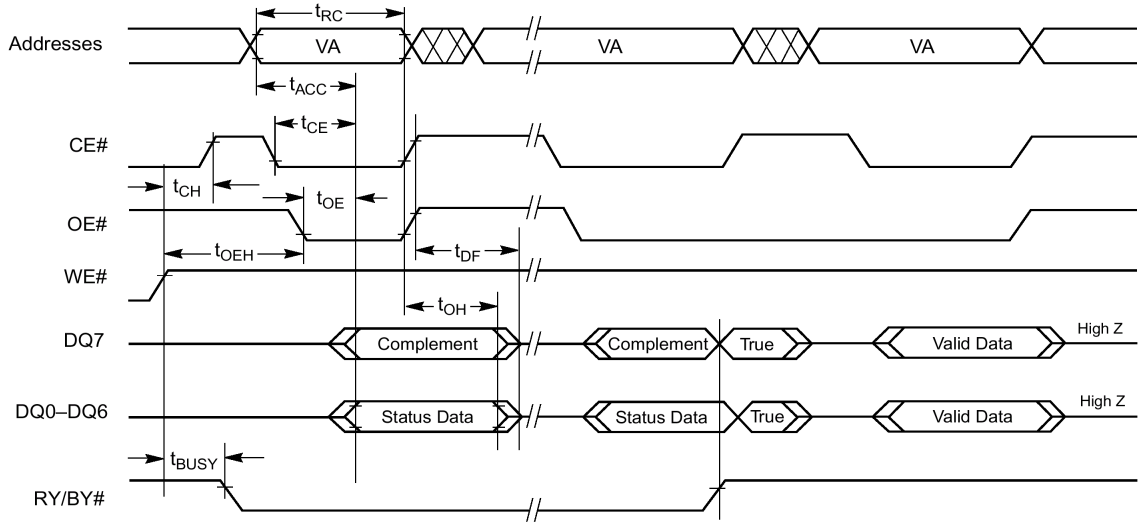
u PROGRAM OPERATIONS TIMING



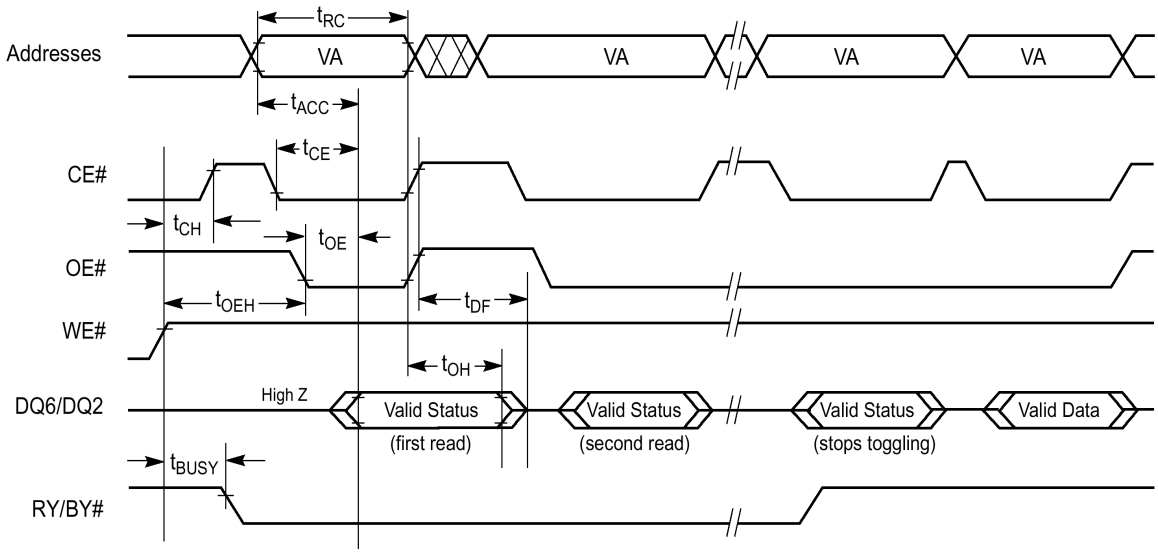
u CHIP/SECTOR ERASE OPERATION TIMINGS



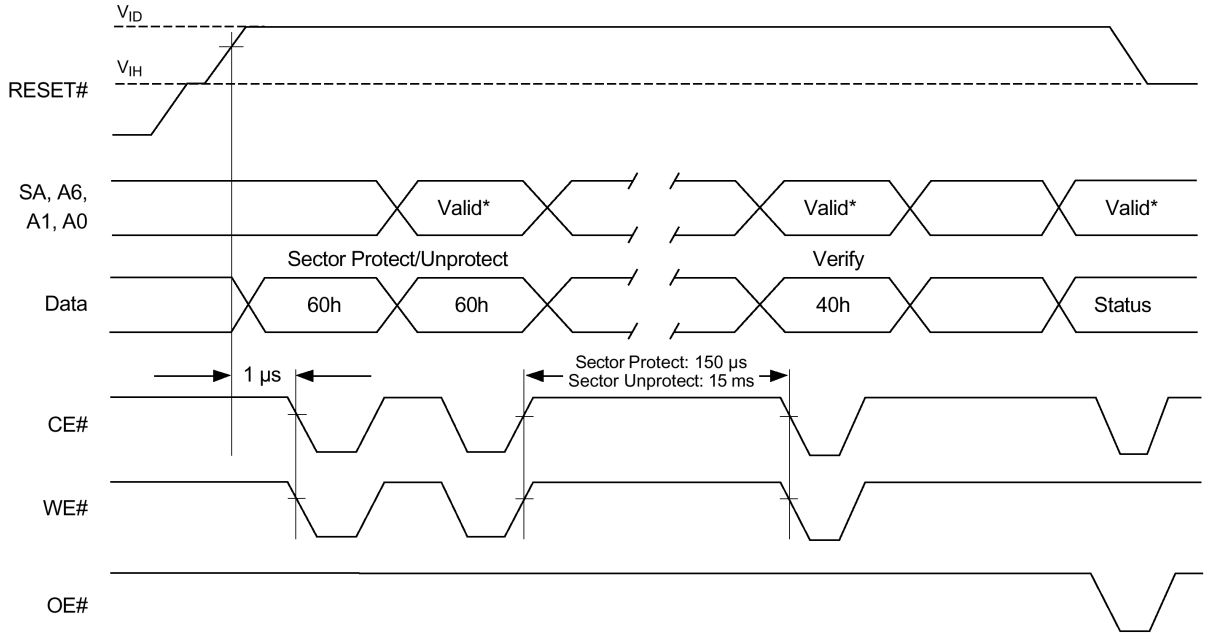
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



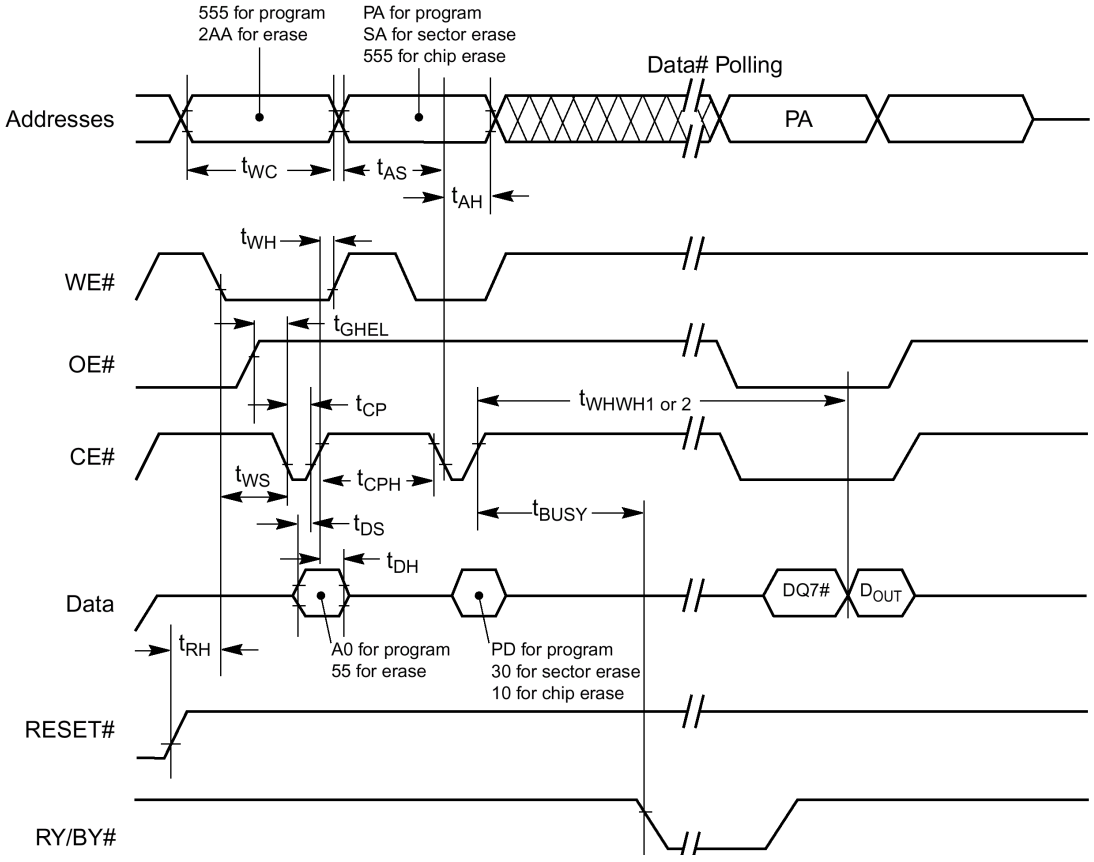
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



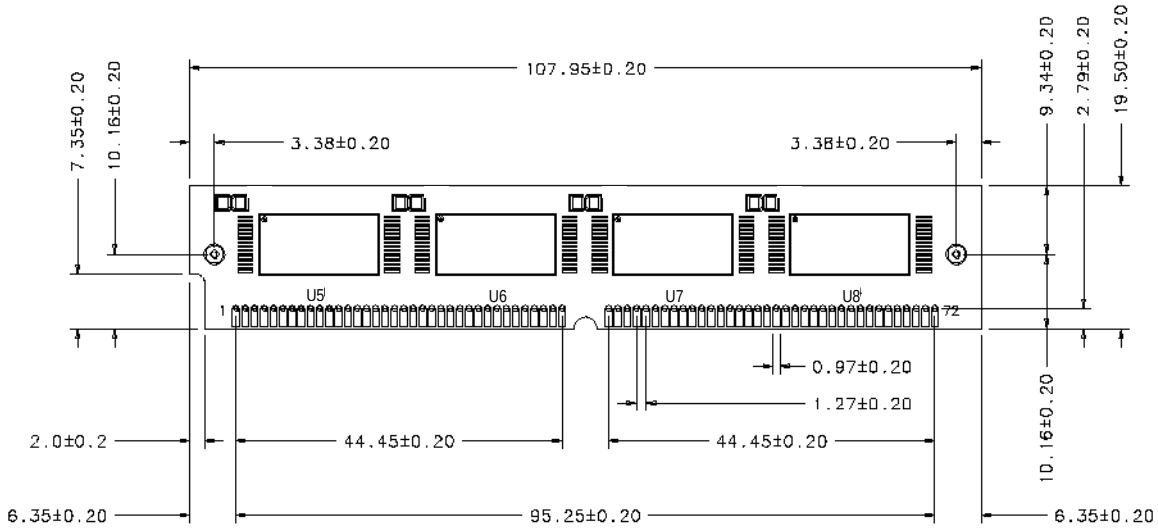
u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

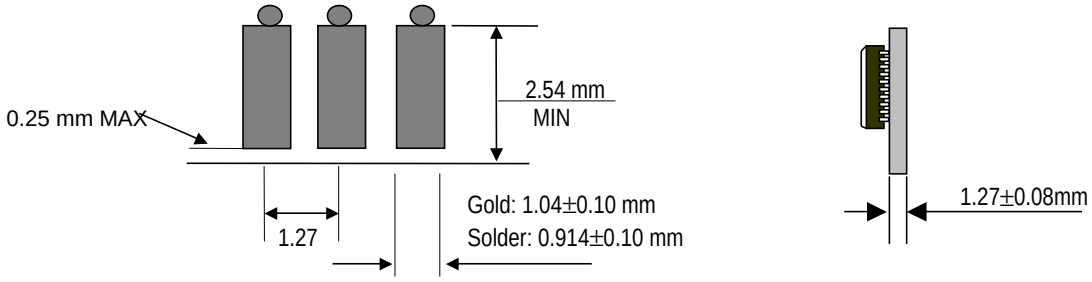


u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS





(Solder & Gold Plating)

ODERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF51232M4V-55	2MByte	512K×32bit	72 Pin-SIMM	4EA	3.3V	55ns
HMF51232M4V-70	2MByte	512K×32bit	72 Pin-SIMM	4EA	3.3V	70ns
HMF51232M4V-90	2MByte	512K×32bit	72 Pin-SIMM	4EA	3.3V	90ns
HMF51232M4V-120	2MByte	512K×32bit	72 Pin-SIMM	4EA	3.3V	120ns