32Mbyte(4Mx72) EDO Mode 4K Ref. 5V, DIMM 168 pin
Part No. HMD4M72D18EG-6

GENERAL DESCRIPTION

The HMD4M72D18EG is a 4Mx72bits Dynamic RAM high density memory module. The HMD4M72D18EG consists of eighteen CMOS 4Mx4bits DRAMs in SOJ/TSOPII 400mil packages mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The HMD4M72D18EG is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets

FEATURES

w Part Identification
HMD4M72D18EG --- 4KCycles/64ms Ref, Gold Plate Lead

w High-density 32MByte design
w New JEDEC standard proposal without buffer
w CAS-before-RAS Refresh capability
w RAS-only and Hidden refresh capability
w Single +5±0.5V power supply
w EDO mode operation.
w LVTTL compatible inputs and outputs
w FR4-PCB design
w Access times : 50, 60ns

PERFORMANCE RANGE

SPEED	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	15ns	84ns	20ns
-6	60ns	17ns	104ns	25ns

w Timing
50ns access -5
60ns access -6
w Packages
168-pin DIMM D

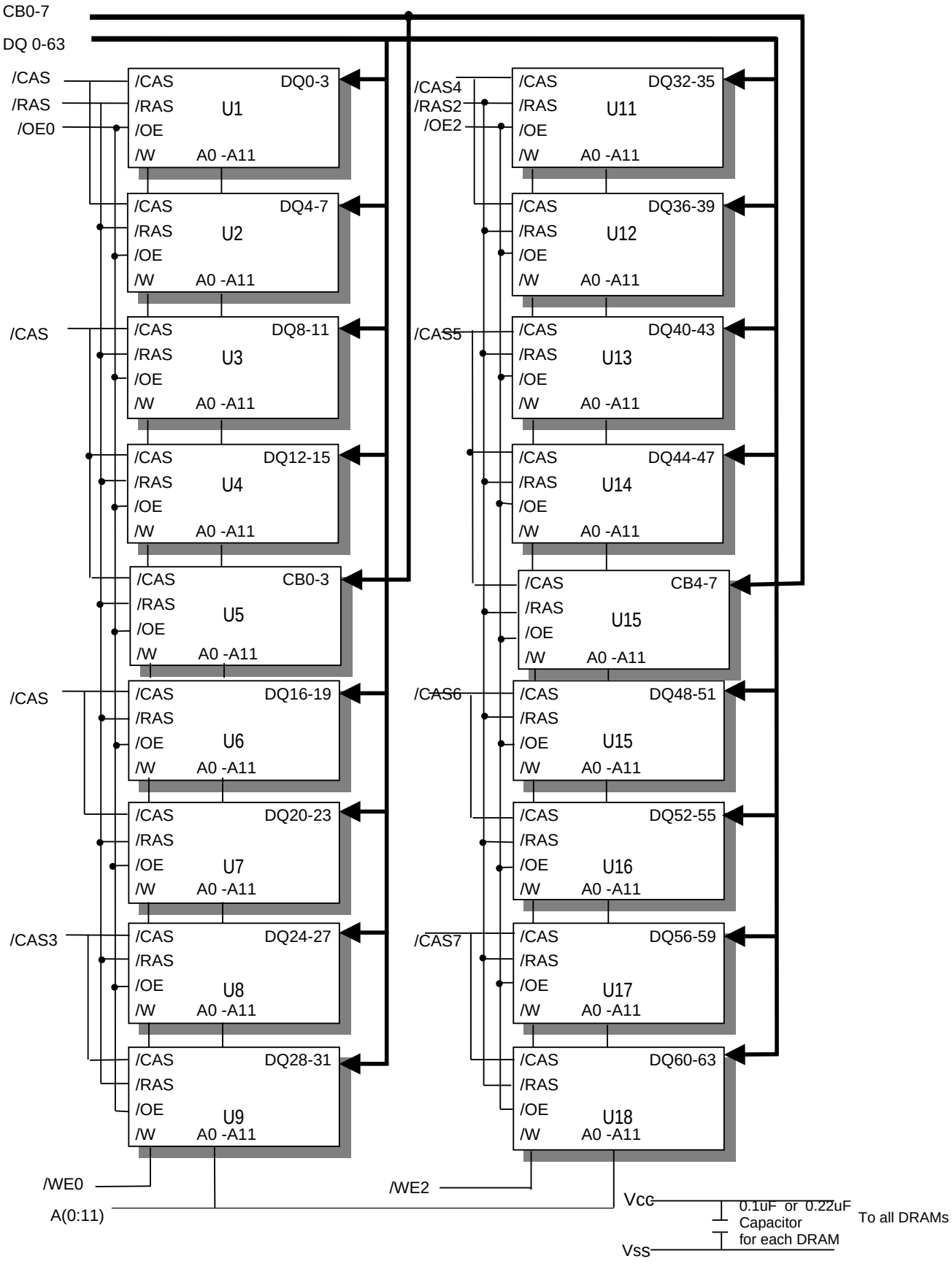
PIN NAMES

Pin Name	Function	Pin Name	Function	Pin Name	Function
A0-A11	Address Input (4k ref)	/RAS0, /RAS2	Row Address Strobe	Vss	Ground
A0-A12	Address Input (8k ref)	/CAS0 - /CAS7	Column Address Strobe	NC	No Connection
/W0,/W2	Read/Write Enable	SCL	Serial Clock	Vcc	Power (+5V)
/OE0,/OE2	Output Enable	DU	Don't use	SDA	Serial Address /Data I/O
SA0 – SA2	Address in EEPROM	CB0 - CB7	Check Bit	DQ0-DQ63	Data In/Out

PIN ASSIGNMENT

PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vss	29	/CAS1	57	DQ18	85	Vss	113	/CAS5	141	DQ50
2	DQ0	30	/RAS0	58	DQ19	86	DQ32	114	/RAS1	142	DQ51
3	DQ1	31	/OE0	59	Vcc	87	DQ33	115	NC	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	NC	90	Vcc	118	A3	146	NC
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	NC	67	DQ23	95	DQ40	123	NC	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	NC	153	DQ56
14	DQ10	42	NC	70	DQ25	98	DQ42	126	NC	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	/OE2	72	DQ27	100	DQ44	128	NC	156	DQ59
17	DQ13	45	/RAS2	73	Vcc	101	DQ45	129	/RAS3	157	Vcc
18	Vcc	46	/CAS2	74	DQ28	102	Vcc	130	/CAS6	158	DQ60
19	DQ14	47	/CAS3	75	DQ29	103	DQ46	131	/CAS7	159	DQ61
20	DQ15	48	/W2	76	DQ30	104	DQ47	132	NC	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	/W0	55	DQ16	83	SCL	111	NC	139	DQ48	167	SA2
28	/CAS0	56	DQ17	84	Vcc	112	/CAS4	140	DQ49	168	Vcc

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to 4.6V
Voltage on Vcc Supply Relative to Vss	Vcc	-0.5V to 4.6V
Power Dissipation	P_D	18W
Storage Temperature	T_{STG}	-55°C to 150°C
Short Circuit Output Current	I_{OS}	50mA

w Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5..	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

SYMBOL	SPEED	HMD4M72D18EG (4K REF)		UNITS
		MIN	MAX	
I_{CC1}	-5	-	1980	mA
	-6		1800	mA
I_{CC2}	Don't care	-	18	MA
I_{CC3}	-5	-	1980	mA
	-6		1800	mA
I_{CC4}	-5	-	1620	mA
	-6		1440	mA
I_{CC5}	Don't care	-	9	MA
I_{CC6}	-5	-	1980	mA
	-6		1800	mA
Icc7	L		4500	µA
Iccs	L		3600	µA

I_{CC1} : Operating Current * (/RAS , /CAS , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current (/RAS=/CAS=V_{IH})

I_{CC3} : /RAS Only Refresh Current * (/CAS=V_{IH}, /RAS, Address cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * (/RAS=V_{IL}, /CAS, Address cycling @t_{PC}=min)

I_{CC5} : Standby Current (/RAS=/CAS=Vcc-0.2V)

I_{CC6} : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @t_{RC}=min)

I_{IL} : Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 4.5V, all other pins not under test = 0V)

I_{OL} : Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 3.3V

V_{OH} : Output High Voltage Level (I_{OH}= -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address cad be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.

CAPACITANCE (T_A=25°C, Vcc = 5V, f = 1Mz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance (A0-A11)	C_{IN1}	-	20	pF
Input Capacitance (/W0,/W1,/OE0,/OE2)	C_{IN2}	-	20	pF
Input Capacitance (/RAS0,/RAS2)	C_{IN3}	-	73	pF
Input Capacitance (/CAS0-/CAS7)	C_{IN4}	-	20	pF
Input/Output Capacitance (DQ0-63)	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, See notes 1,2.)

STANDARD OPERATION	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	t_{RC}	84		104		ns
Read-modify-write cycle time	t_{RWC}	116		140		ns
Access time from /RAS	t_{RAC}		50		60	ns
Access time from /CAS	t_{CAC}		13		15	ns
Access time from column address	t_{AA}		25		30	ns
/CAS to output in Low-Z	t_{CLZ}	3		3		ns
/OE to output in Low-Z	t_{OLZ}	3		3		ns
Output buffer turn-off delay from /CAS	t_{OFF}	3	13	3	13	ns
Transition time (rise and fall)	t_T	2	50	2	50	ns
/RAS precharge time	t_{RP}	30		40		ns
/RAS pulse width	t_{RAS}	50	10K	60	10K	ns
/RAS hold time	t_{RSH}	13		15		ns
/CAS hold time	t_{CSH}	38		45		ns
/CAS pulse width	t_{CAS}	8	10K	10	10K	ns
/RAS to /CAS delay time	t_{RCD}	20	37	20	45	ns
/RAS to column address delay time	t_{RAD}	15	25	15	30	ns

/CAS to /RAS precharge time	t_{CRP}	5		5		ns
Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	10		10		ns
Column address set-up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	8		10		ns
Column address hold referenced to /RAS	t_{RRH}	0		0		ns
Column Address to /RAS lead time	t_{RAL}	25		30		ns
Read command set-up time	t_{RCS}	0		0		ns
Read command hold referenced to /CAS	t_{RCH}	0		0		ns
Read command hold referenced to /RAS	t_{RRH}	0		0		ns
Write command hold time	t_{WCH}	10		10		ns
Write command pulse width	t_{WP}	10		10		ns
Write command to /RAS lead time	t_{RWL}	13		15		ns
Write command to /CAS lead time	t_{CWL}	8		10		ns
Data-in set-up time	t_{DS}	0		0		ns
Data-in hold time	t_{DH}	8		10		ns
Refresh period	t_{REF}		32		32	ms
Write command set-up time	t_{WCS}	0		0		ns
/CAS to /W delay time	t_{CWD}	30		34		ns
/RAS to /W delay time	t_{RWD}	67		79		ns
Column address to /W delay time	t_{AWD}	42		49		ns
/CAS precharge to /W delay time	t_{CPWD}	47		54		ns
/CAS setup time (/CAS-before /RAS refresh)	t_{CSR}	5		5		ns
/CAS hold time(/CAS-before-/RAS refresh)	t_{CHR}	10		10		ns
/RAS to /CAS precharge time	t_{RPC}	5		5		ns
Access time from /CAS precharge	t_{CPA}		28		35	ns
Hyper page mode cycle time	t_{HPC}	20		25		ns
Hyper page mode read-modify write cycle time	t_{HPRWC}	47		56		ns
/CAS precharge time(Hyper page cycle)	t_{CP}	8		10		ns
/RAS pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns
/RAS hold time from /CAS precharge	t_{RHCP}	30		35		ns
/OE access time	t_{OEA}		13		15	ns
/OE to date delay	t_{OED}	13		15		ns
Output buffer tune off delay time from /OE	t_{OEZ}	3	13	3	15	ns
/OE command hold time	t_{OEH}	13		13		ns

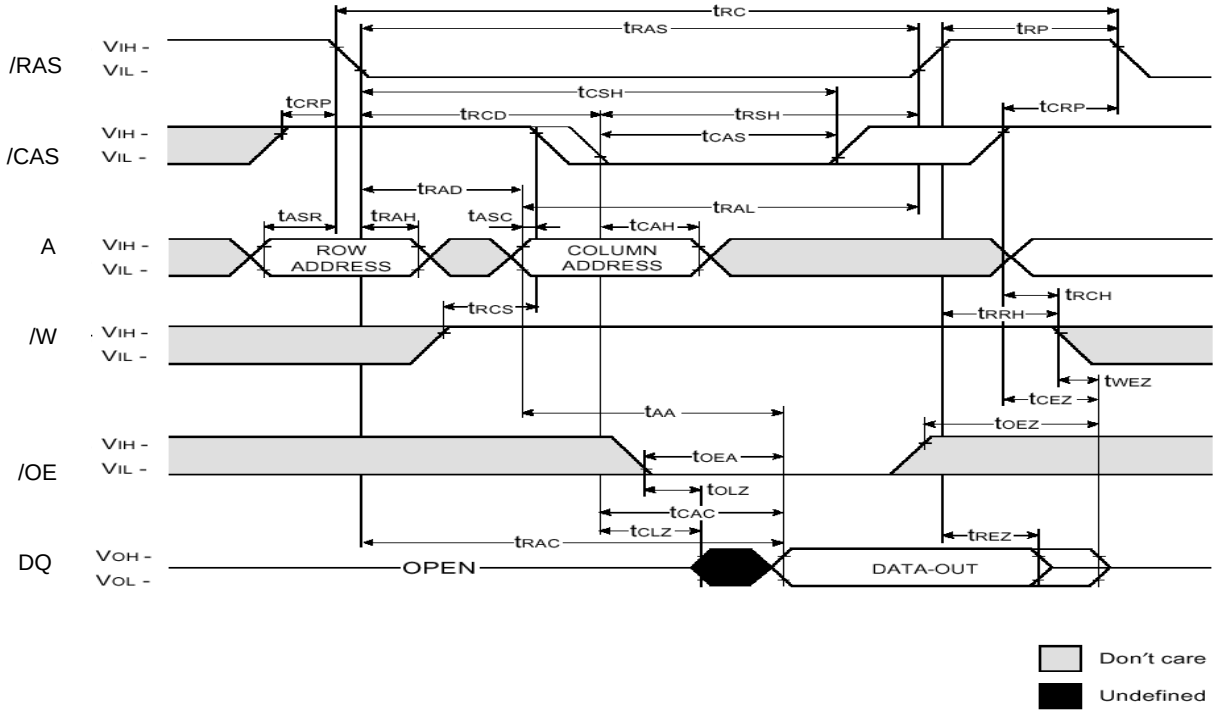
Output data hold time	t_{DOH}	10		10		ns
Output buffer turn off delay from /RAS	t_{REZ}	3	13	3	15	ns
Output buffer turn off delay from /W	t_{WEZ}	3	13	3	15	ns
/W to data delay	t_{WED}	15		15		ns
/OE to /CAS hold time	t_{OCH}	5		5		ns
/CAS hold time to /OE	t_{CHO}	5		5		ns
/OE precharge time	t_{OEP}	5		5		ns
/W pulse width (Hyper page cycle)	t_{WPE}	5		5		ns

NOTES

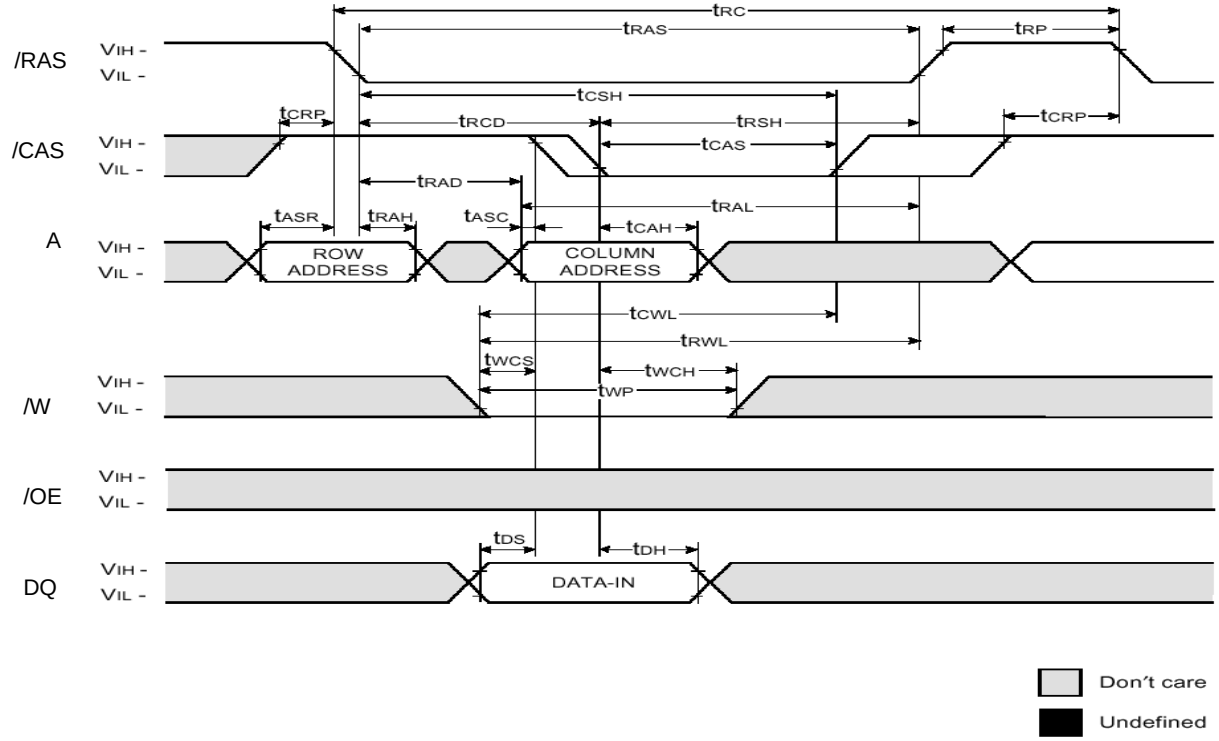
1. An initial pause of 200μs is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are $V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter.
   They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, The condition of the data out is indeternimated.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit. then access time is controlled by t_{AA}.
10. If /RAS goes to high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going. If /Cas goes to high before /RAS high going, the open circuit condition of the output is achieved by /RAS high going.
11. $t_{ASC} \geq 6ns$

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE

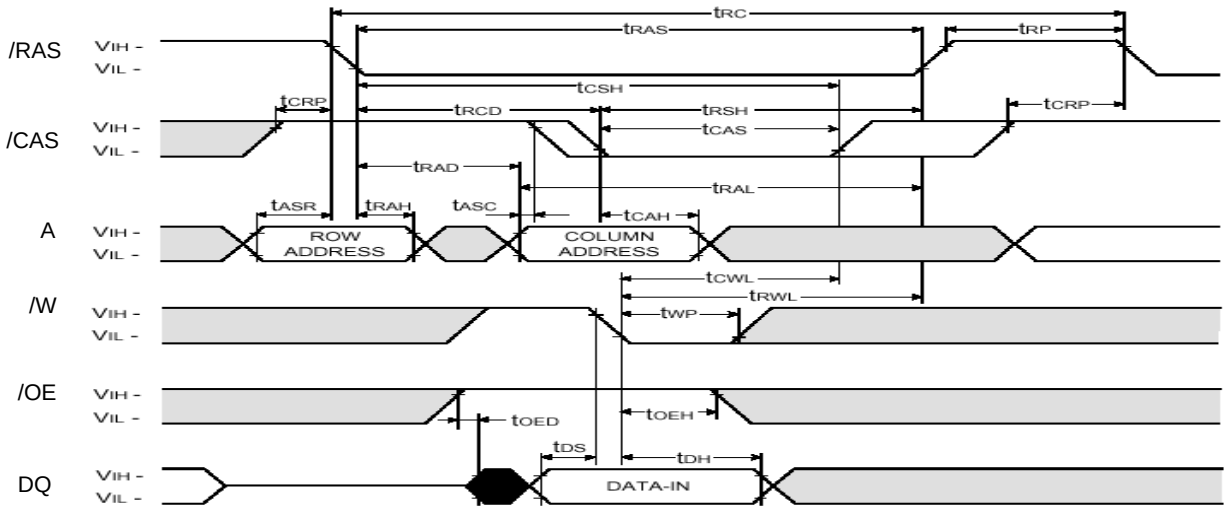


TIMING WAVEFORM OF WRITE CYCLE (EARLY WRITE)

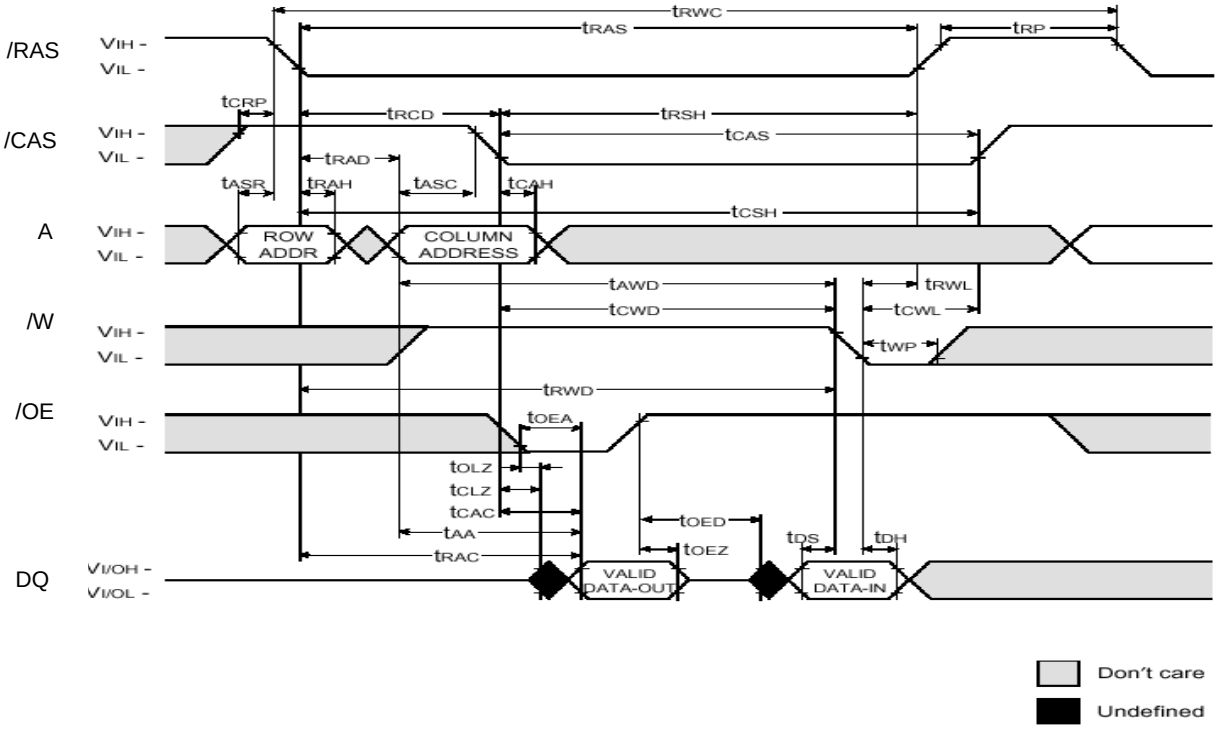


TIMING WAVEFORM OF WRITE CYCLE (/OE CONTROLLED WRITE)

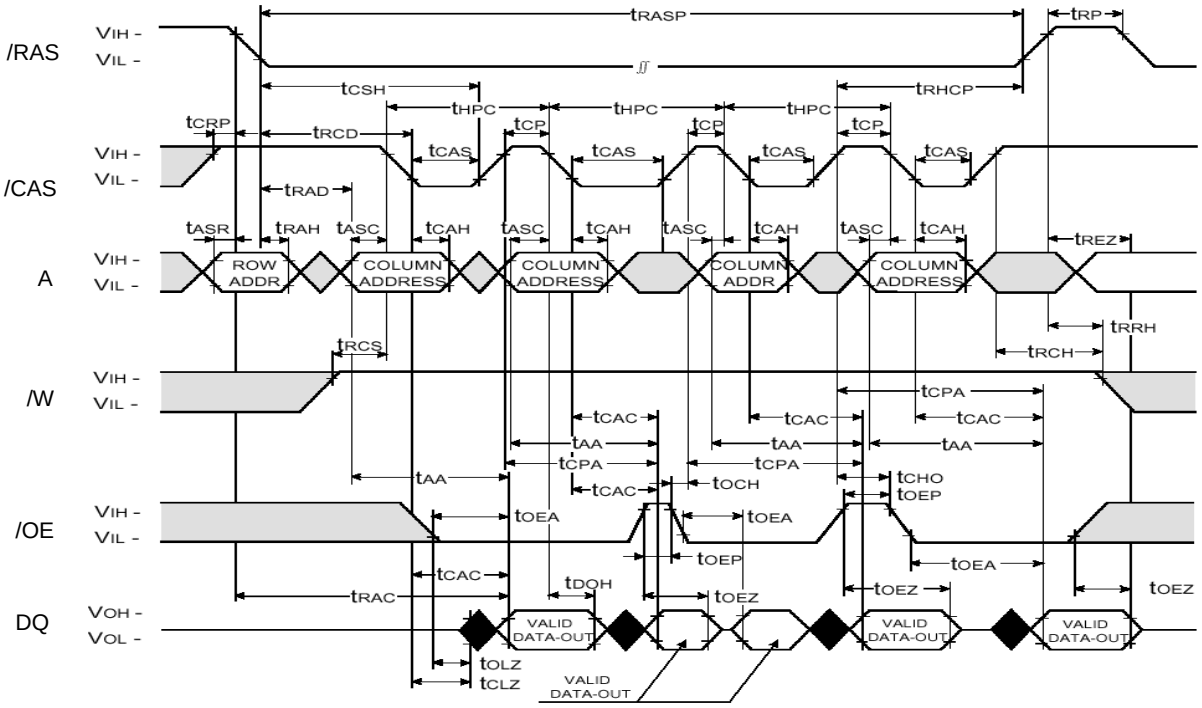
NOTE : Dout = OPEN



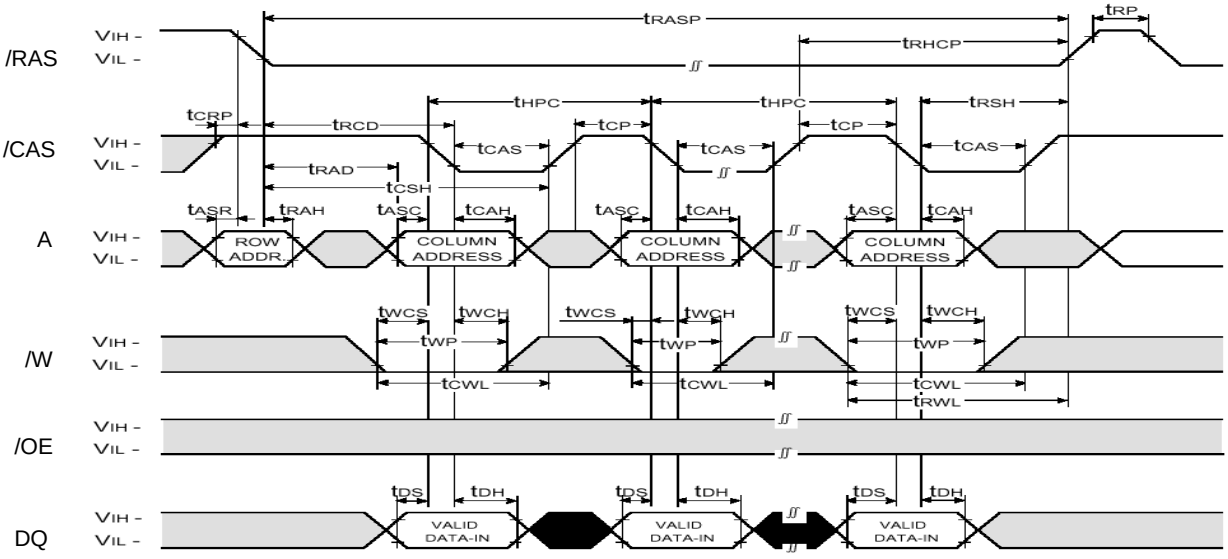
READ MODIFY WRITE CYCLE



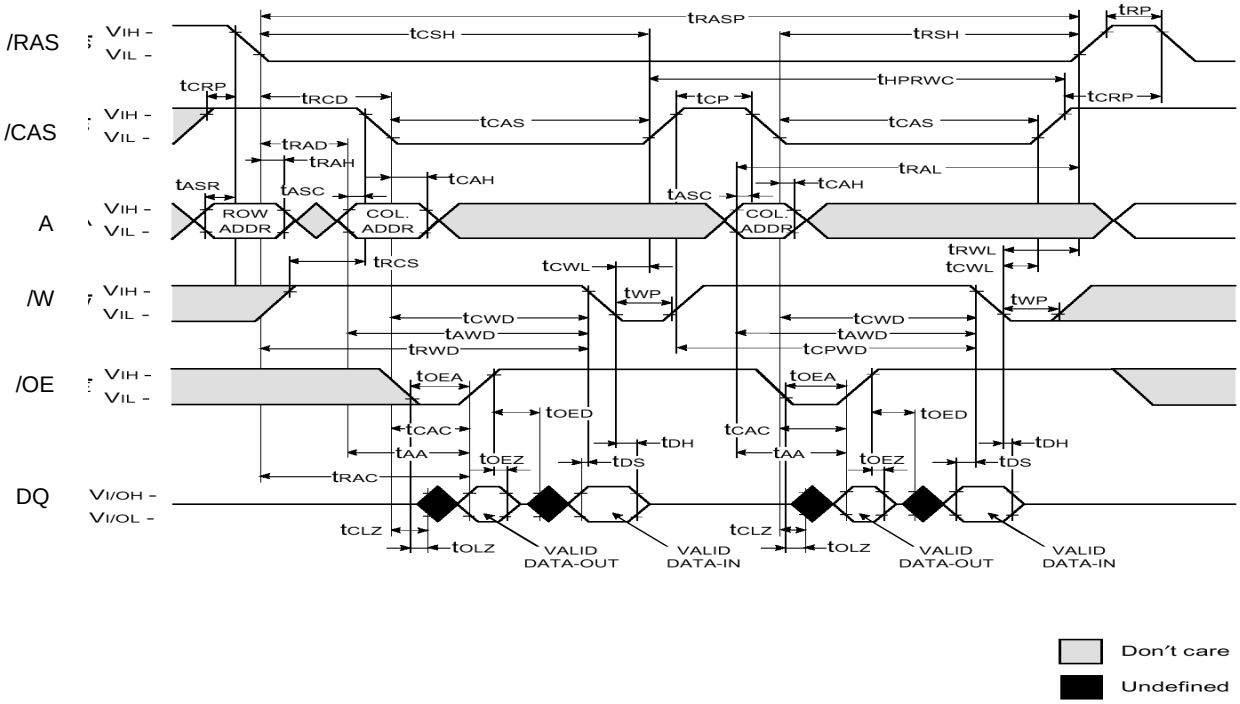
HYPER PAGE READ CYCLE



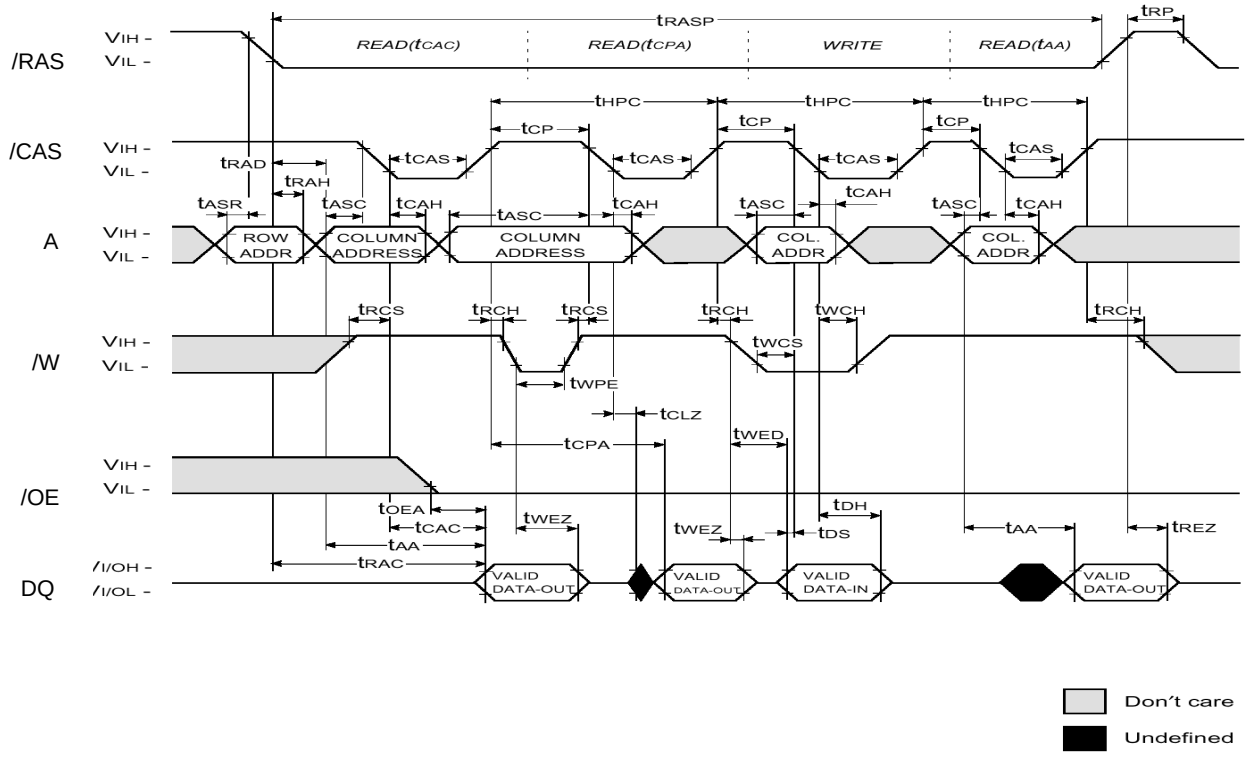
HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ MODIFY WRITE CYCLE



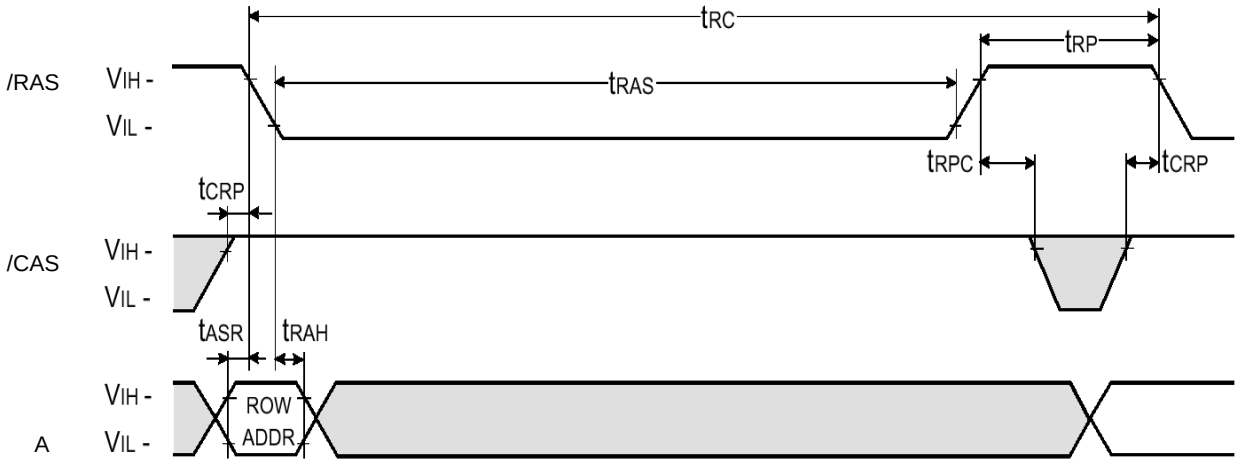
HYPER PAGE READ AND WRITE MIXED CYCLE



/RAS ONLY REFRESH CYCLE

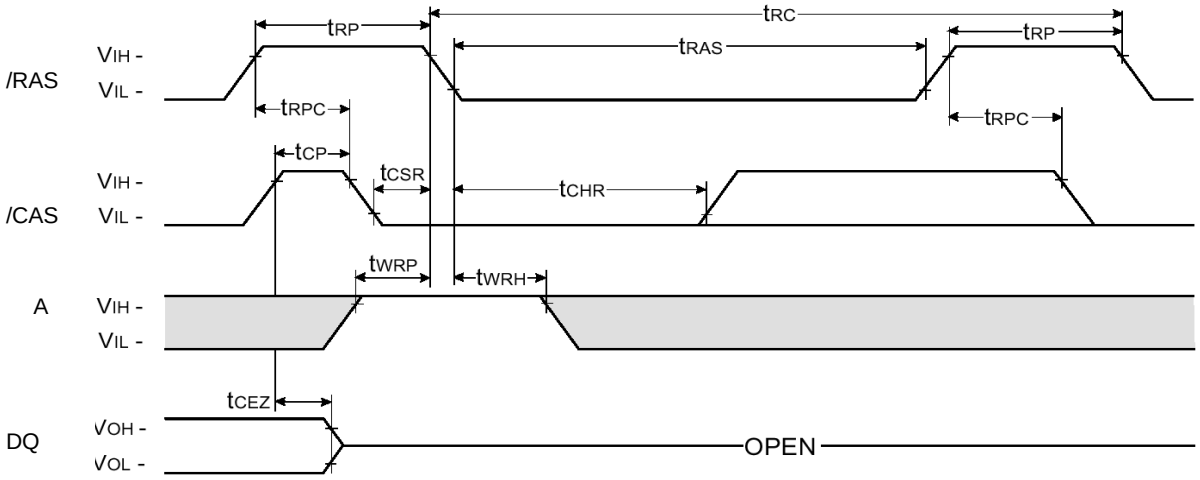
NOTE: /W,/OE,Din = Don't care

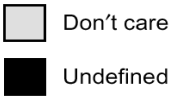
Dout = OPEN



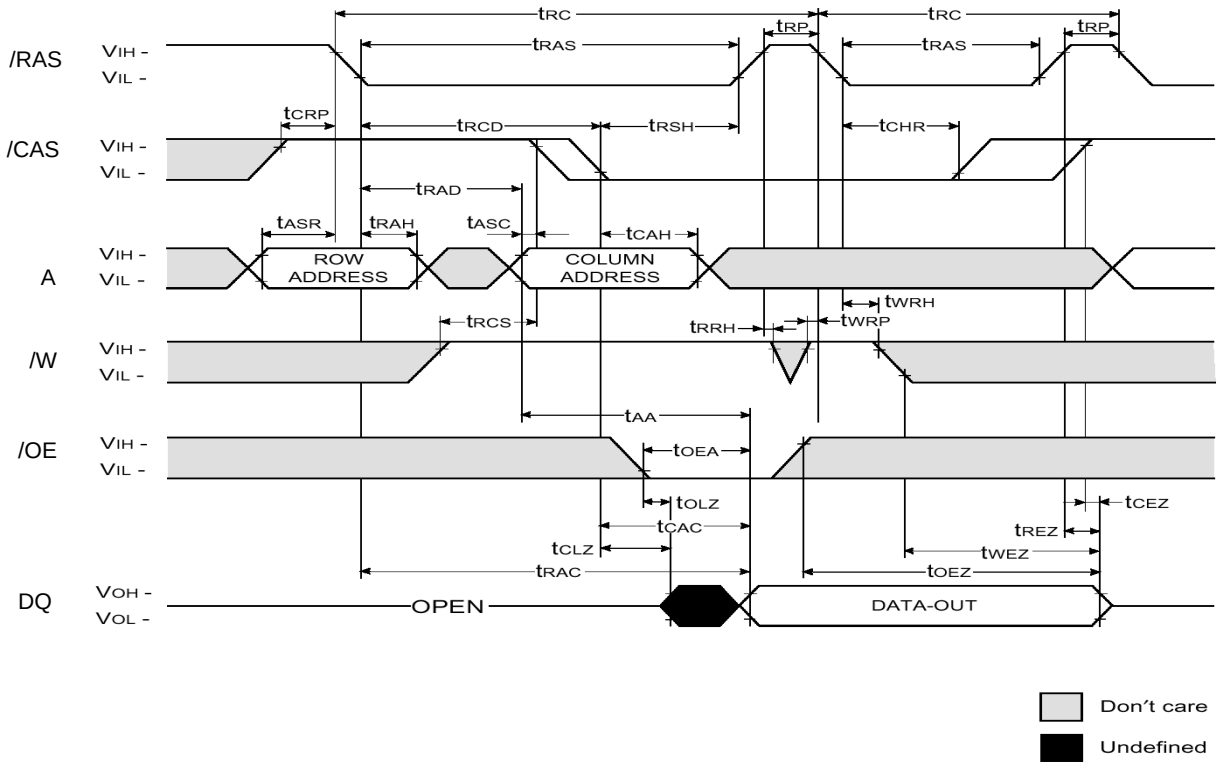
/CAS BEFORE /RAS REFRESH CYCLE

NOTE: /OE, A = Don't care



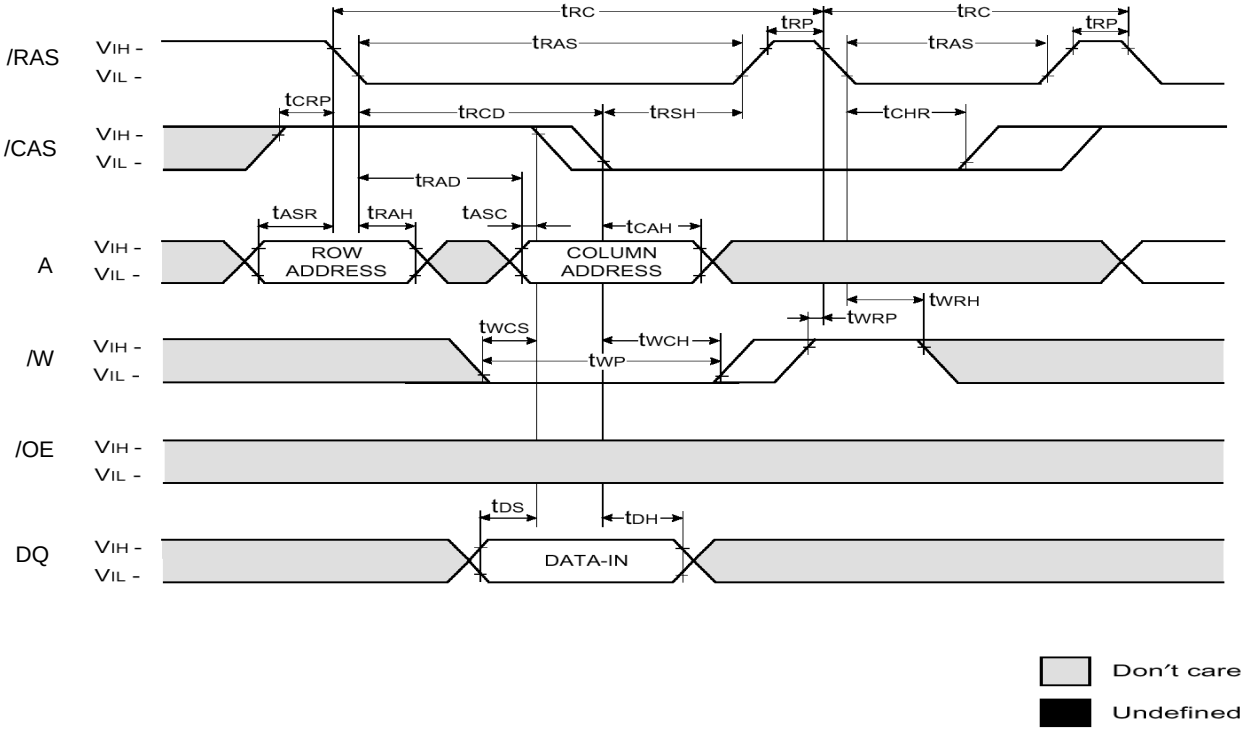


HIDDEN REFRESH CYCLE (READ)

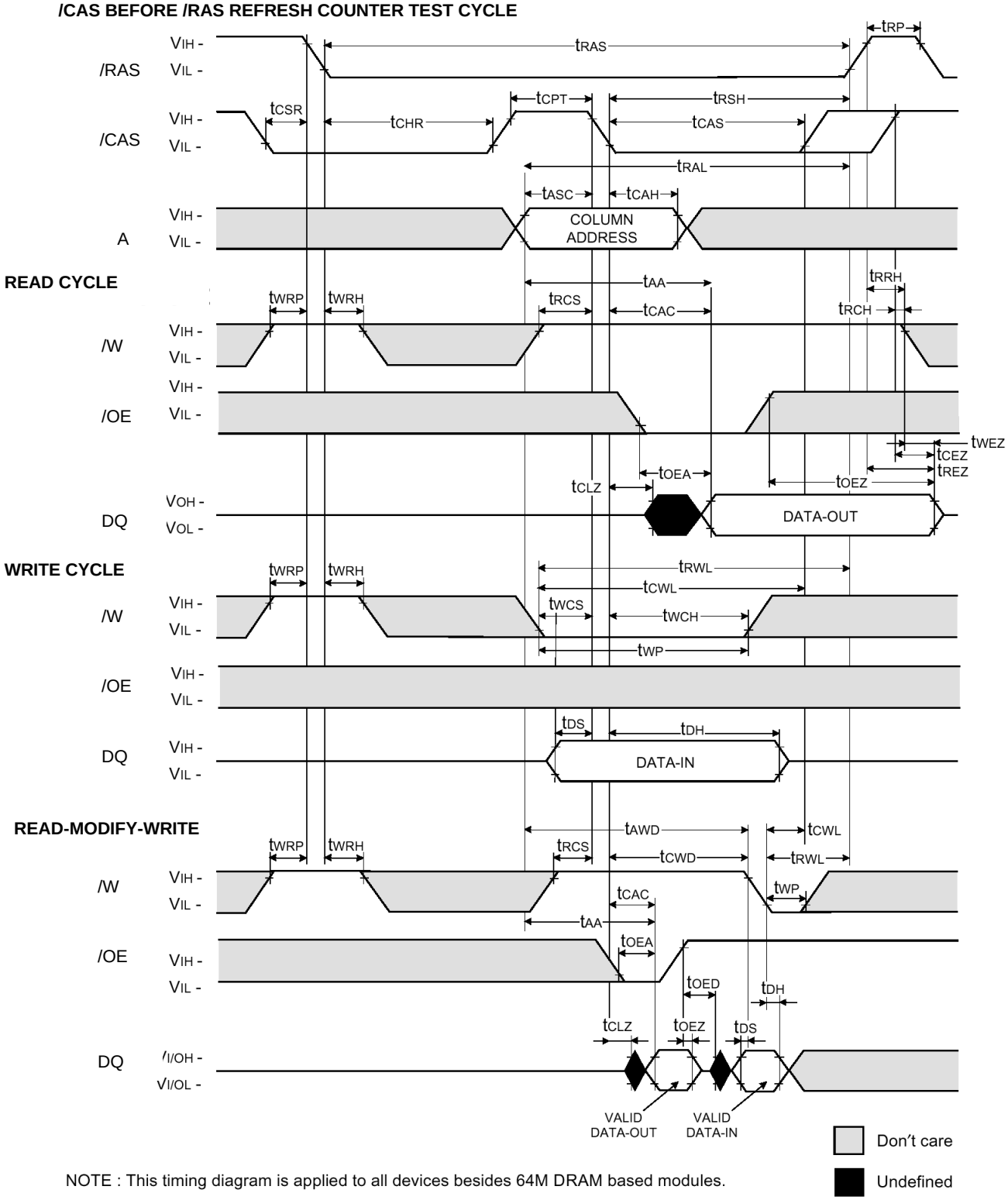


HIDDEN REFRESH CYCLE (WRITE)

NOTE: Dout = OPEN



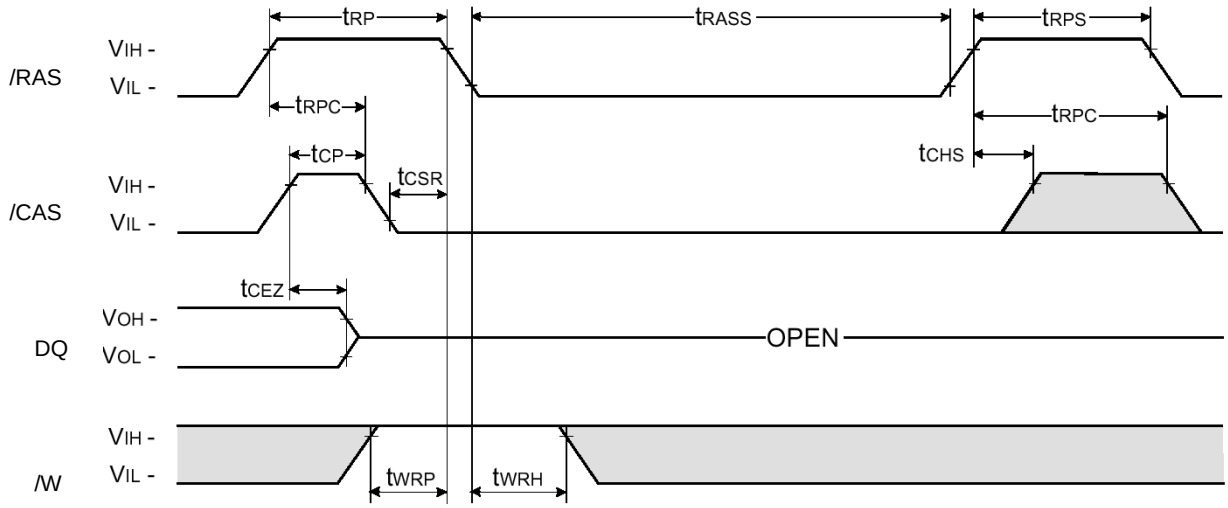
/CAS BEFORE /RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

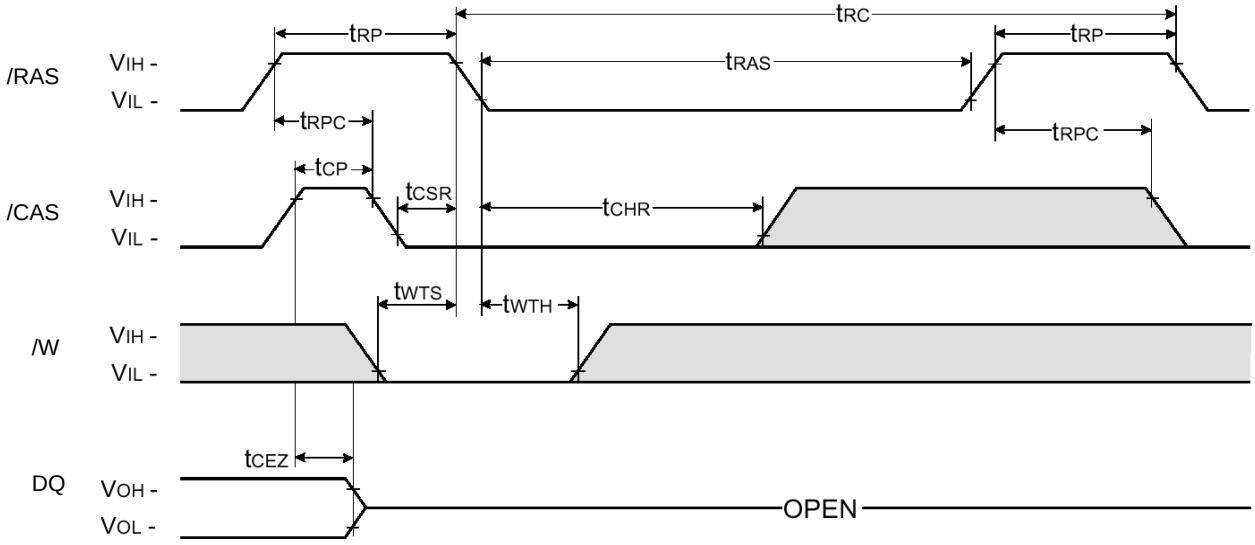
/CAS BEFORE /RAS SELF REFRESH CYCLE

NOTE : /OE, A = Don't care



TEST MODE IN CYCLE

NOTE: /OE, A = Don't care



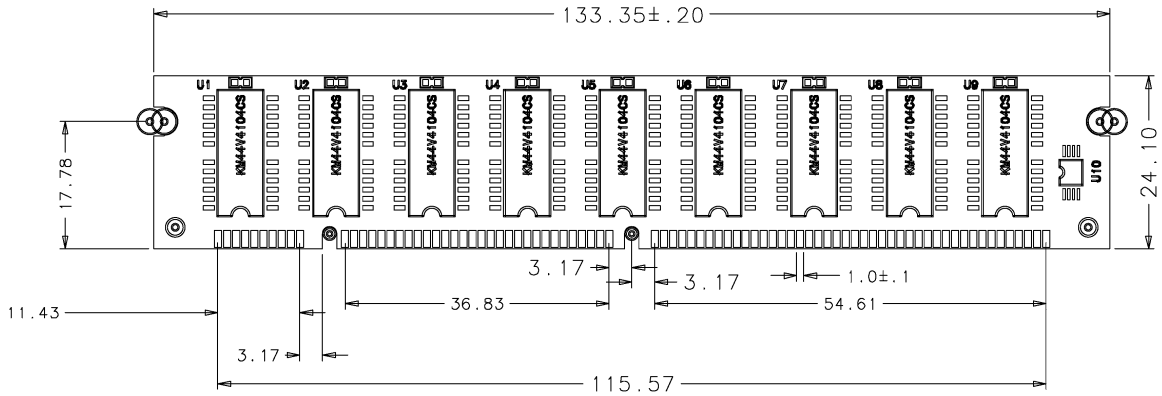
Don't care

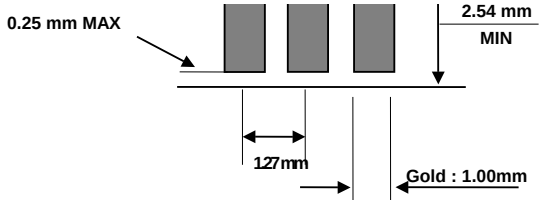
Undefined

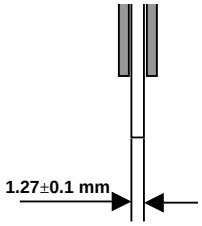
PACKAGING INFORMATION

UNIT:mm

(FRONT VIEW)







ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	MODE	SPEED
HMD4M72D18EG-5	32MByte	x 72	168 Pin-DIMM	18EA	5V	EDO	50ns
HMD4M72D18EG-6	32MByte	x 72	168 Pin-DIMM	18EA	5V	EDO	60ns