

## 0.8V Reference Ultra Low Dropout (0.25V@3A) Linear Regulator

### Features

- Ultra Low Dropout
  - 0.25V(typical) at 3A Output Current
- Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable
- 0.8V Reference Voltage
- High Output Accuracy
  - $\pm 1.5\%$  over Line, Load and Temperature
- Fast Transient Response
- Adjustable Output Voltage by External Resistors
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit Protection
- Under-Voltage Protection
- Thermal Shutdown with Hysteresis
- Power-OK Output with a Delay Time
- Shutdown for Standby or Suspend Mode
- Simple SOP-8-P Package with Exposed Pad
- Lead Free Available (RoHS Compliant)

### Applications

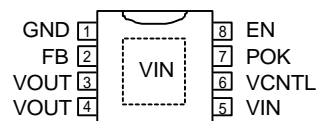
- Front Side Bus VTT (1.2V/3A)
- Note Book PC Applications
- Motherboard Applications

### General Description


The APL5913 is a 3A ultra low dropout linear regulator. This product is specifically designed to provide well supply volatage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The APL5913 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The APL5913 can be enabled by other power system. Pulling and holding the EN pin below 0.3V shuts off the output.

The APL5913 is available in SOP-8-P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance, being applicable in 2~3W applications.

### Pin Configuration



SOP-8-P (Top View)

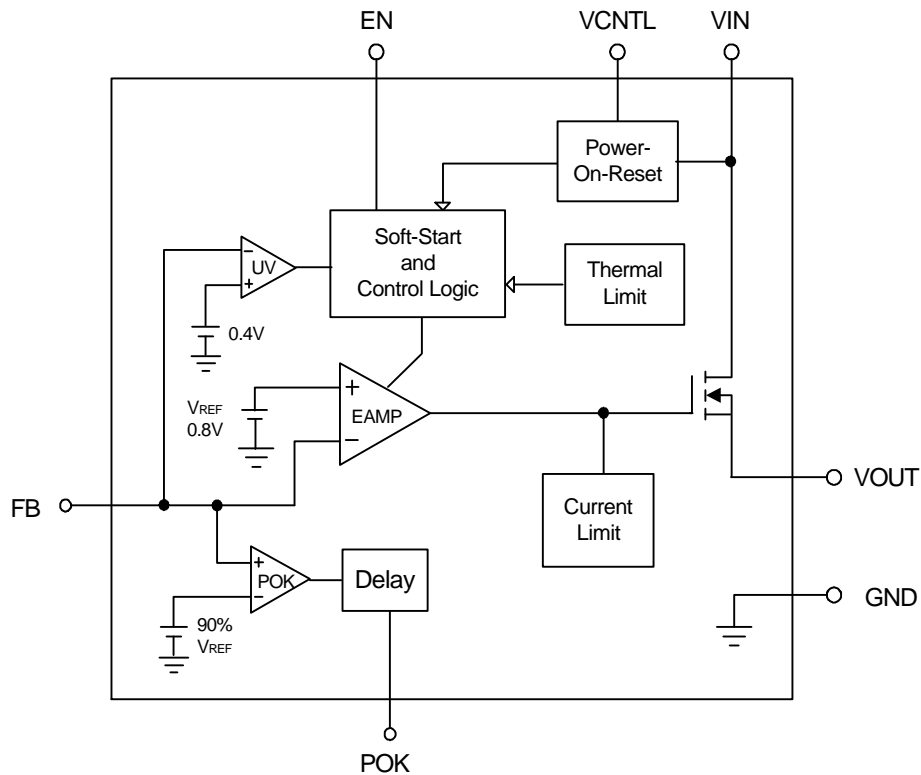
 = Exposed Pad  
(connected to  $V_{IN}$  plane for better heat dissipation)

## Ordering and Marking Information

<p>APL5913 - □□□-□□□</p> <ul style="list-style-type: none"> <li>□□□ - Lead Free Code</li> <li>□□ - Handling Code</li> <li>□ - Temp. Range</li> <li>□ - Package Code</li> </ul>	<p>Package Code                  KA : SOP-8-P                  Operating Ambient Temp. Range                  C : 0 to 70°C                  Handling Code                  TU : Tube      TR : Tape &amp; Reel                  Lead Free Code                  L : Lead Free Device      Blank : Original Device</p>
<p>APL5913 KA :      <span style="border: 1px solid black; padding: 2px;">APL5913 XXXXX</span></p>	<p>XXXXX - Date Code</p>

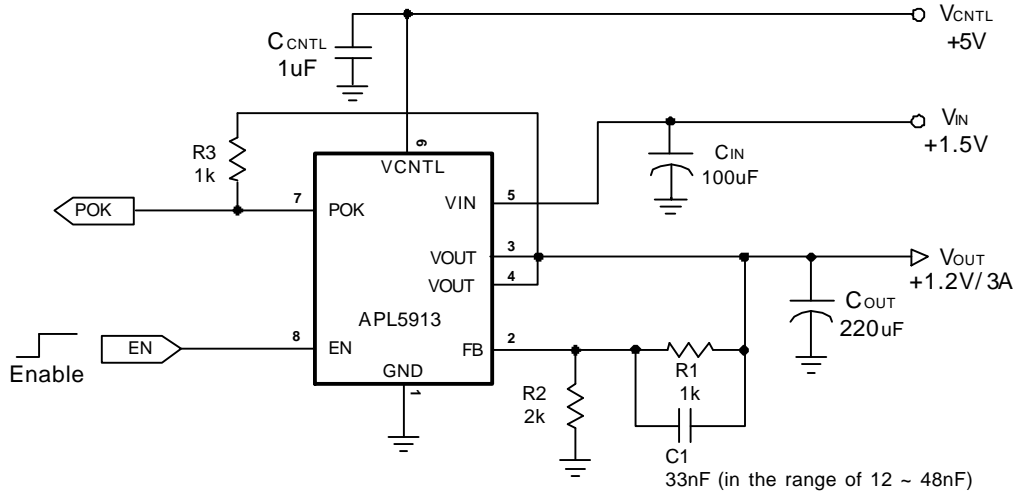
Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

## Block Diagram

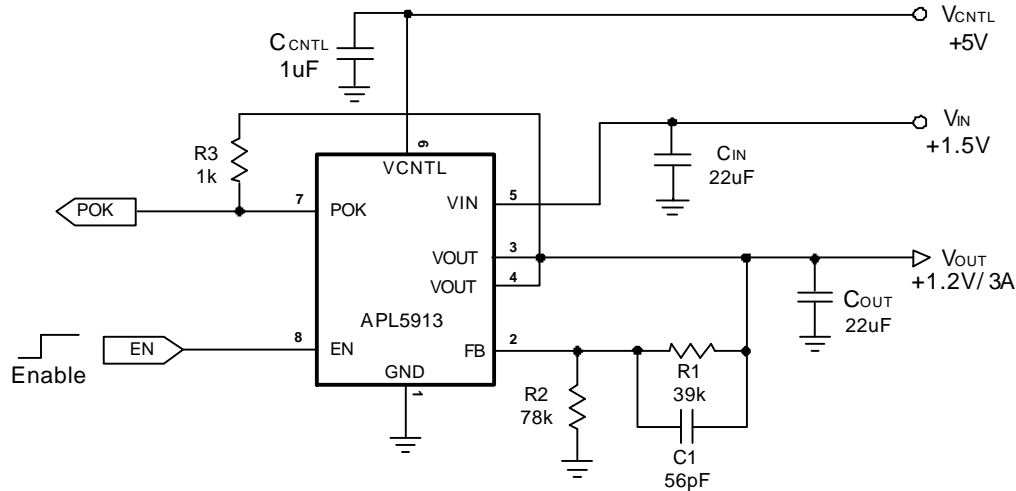


## Typical Application Circuit

### 1. Using an Output Capacitor with $ESR \geq 18m\Omega$



### 2. Using an MLCC as the Output Capacitor



V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
1.05	43	137.6	47
1.5	27	30.86	82
1.8	15	12	150

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>CNTL</sub>	VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 7	V
V <sub>IN</sub>	VIN Supply Voltage (VIN to GND)	-0.3 ~ 3.3	V
V <sub>I/O</sub>	EN and FB to GND	-0.3 ~ V <sub>CNTL</sub> +0.3	V
V <sub>POK</sub>	POK to GND	-0.3 ~ 7	V
P <sub>D</sub>	Average Power Dissipation	3	W
P <sub>PEAK</sub>	Peak Power Dissipation (<20mS)	20	W
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>STG</sub>	Storage Temperature	-65 ~ 150	°C
T <sub>SDR</sub>	Soldering Temperature, 10 Seconds	300	°C
V <sub>ESD</sub>	Minimum ESD Rating (Human Body Mode)	±2	kV

## Thermal Characteristics

Symbol	Parameter	Value	Unit
θ <sub>JA</sub>	Junction-to-Ambient Thermal Resistance in Free Air (Note)	40	°C/W

Note : θ<sub>JA</sub> is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8-P is soldered directly on the PCB.

## Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V <sub>CNTL</sub>	VCNTL Supply Voltage	3.1 ~ 6	V
V <sub>IN</sub>	VIN Supply Voltage	1.1 ~ 3.3	V
V <sub>OUT</sub>	Output Voltage	$V_{CNTL}=3.3\pm5\%$ $V_{CNTL}=5.0\pm5\%$ 0.8 ~ 1.2 0.8 ~ V <sub>IN</sub> -0.2	V
I <sub>OUT</sub>	VOUT Output Current	0 ~ 4	A
T <sub>J</sub>	Junction Temperature	-25 ~ 125	°C

## Electrical Characteristics

Refer to the typical application circuit. These specifications apply over, V<sub>CNTL</sub> = 5V, V<sub>IN</sub> = 1.5V, V<sub>OUT</sub> = 1.2V and T<sub>A</sub> = 0 to 70°C, unless otherwise specified. Typical values refer to T<sub>A</sub> = 25°C.

Symbol	Parameter	Test Conditions	APL5913			Unit
			Min	Typ	Max	
<b>SUPPLY CURRENT</b>						
I <sub>CNTL</sub>	VCNTL Nominal Supply Current	EN = VCNTL	0.4	1	8	mA
I <sub>SD</sub>	VCNTL Shutdown Current	EN = GND		180	300	µA

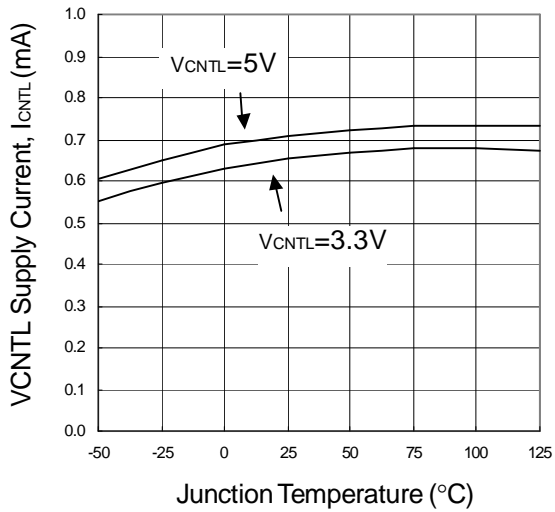
## Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over,  $V_{CNTL} = 5V$ ,  $V_{IN} = 1.5V$ ,  $V_{OUT} = 1.2V$  and  $T_A = 0$  to  $70^{\circ}C$ , unless otherwise specified. Typical values refer to  $T_A = 25^{\circ}C$ .

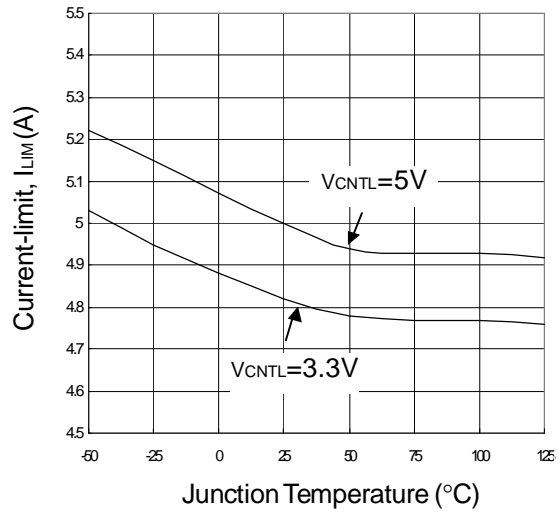
Symbol	Parameter	Test Conditions	APL5913			Unit
			Min	Typ	Max	
<b>POWER-ON-RESET</b>						
	VCNTL POR Threshold	VCNTL Rising	2.7	2.9	3.1	V
	VCNTL POR Hysteresis			0.4		V
	VIN POR Threshold	VIN Rising	0.8	0.9	1.0	
	VIN POR Hysteresis			0.5		V
<b>OUTPUT VOLTAGE</b>						
VREF	Reference Voltage	FB =VOUT		0.8		V
	Output Voltage Accuracy	IOUT=0A ~ 5A, TJ= -25 ~125°C	-1.5		+1.5	%
	Line Regulation	VCNTL=3.3 ~ 5V		0.06	0.15	%
	Load Regulation	IOUT=0A ~ 3A		0.06	0.15	%
<b>DROPOUT VOLTAGE</b>						
	Dropout Voltage	IOUT = 3A, VCNTL=5V, TJ= 25°C		0.17	0.25	V
		IOUT = 3A, VCNTL=5V, TJ= -50~125°C			0.3	V
<b>PROTECTION</b>						
ILIM	Current Limit	VCNTL=5V, TJ= 25°C	3.8	5	6.2	A
		VCNTL=5V, TJ= -25 ~ 125°C	4			A
		VCNTL=3.3V, TJ= 25°C	3.8	4.8	5.3	A
		VCNTL=3.3V, TJ= -25 ~ 125°C	3.8			A
TSD	Thermal Shutdown Temperature	TJ Rising		150		°C
	Thermal Shutdown Hysteresis			50		°C
	Under-Voltage Threshold	VFB Falling		0.4		V
<b>ENABLE and SOFT-START</b>						
	EN Logic High Threshold Voltage	VEN Rising	0.3	0.4	0.5	V
	EN Hysteresis			30		mV
	EN Pin Pull-Up Current	EN=GND		10		µA
TSS	Soft-Start Interval			2		mS
<b>POWER OK and DELAY</b>						
VPOK	POK Threshold Voltage for Power OK	VFB Rising	90%	92%	94%	VREF
VPNOK	POK Threshold Voltage for Power Not OK	VFB Falling	79%	81%	83%	VREF
	POK Low Voltage	POK sinks 5mA		0.25	0.4	V
TDELAY	POK Delay Time		1	3	10	mS

## Typical Operating Characteristics

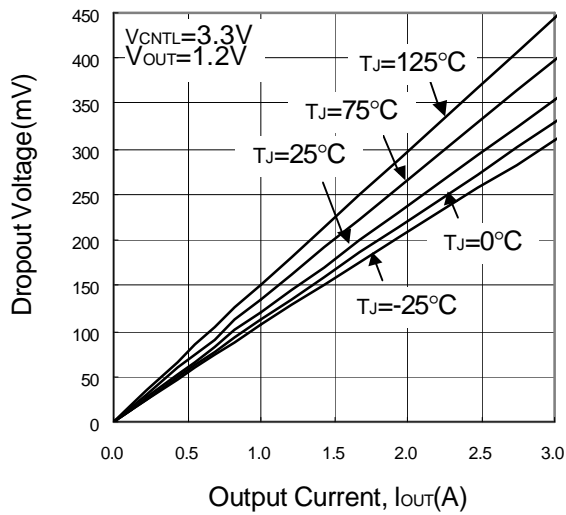
VCNTL Supply Current vs. Junction Temperature



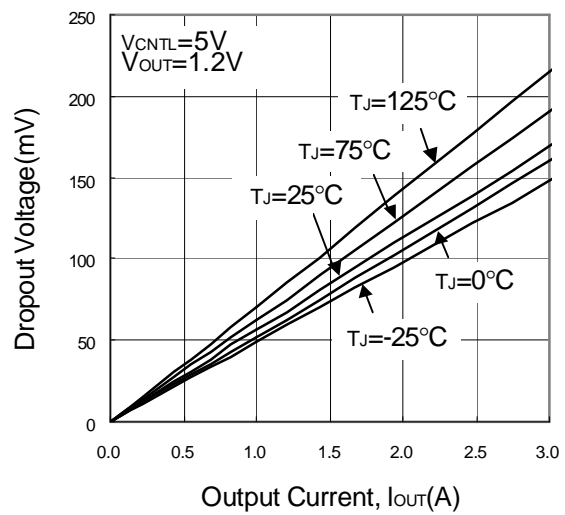
Current-limit vs. Junction Temperature



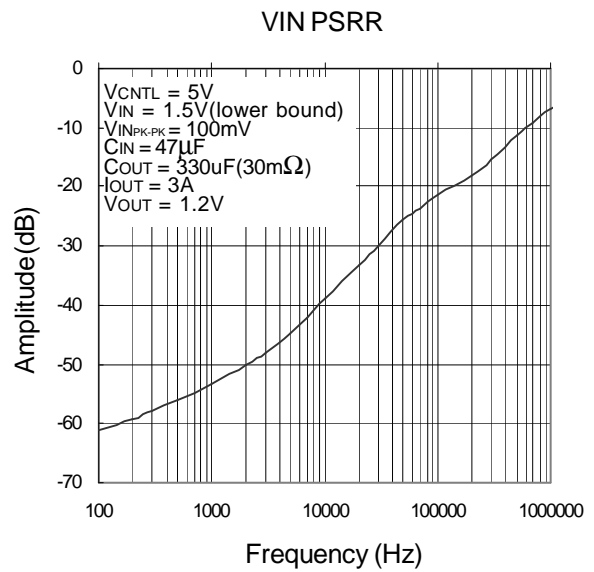
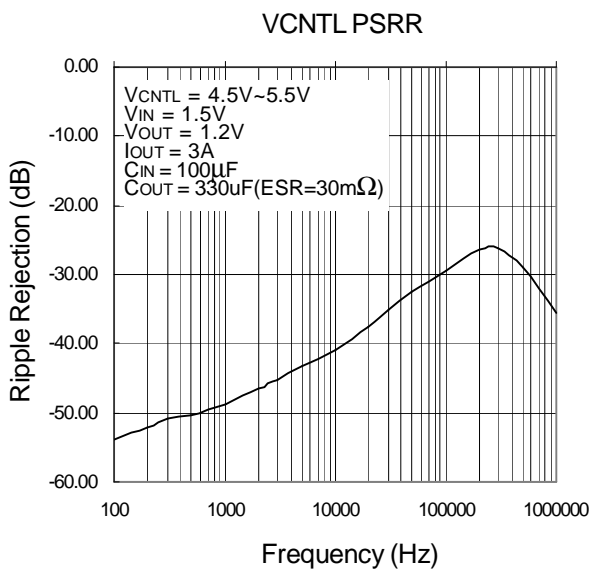
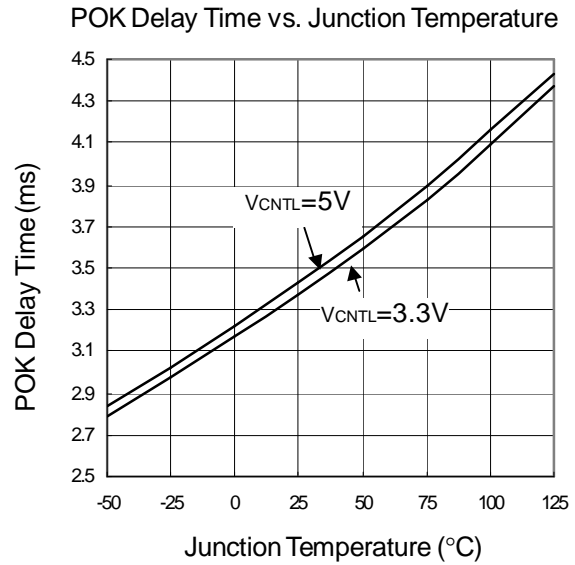
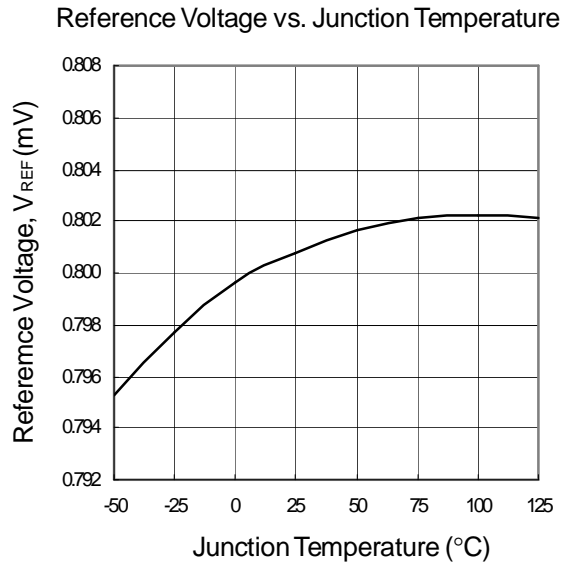
Dropout Voltage vs. Output Current



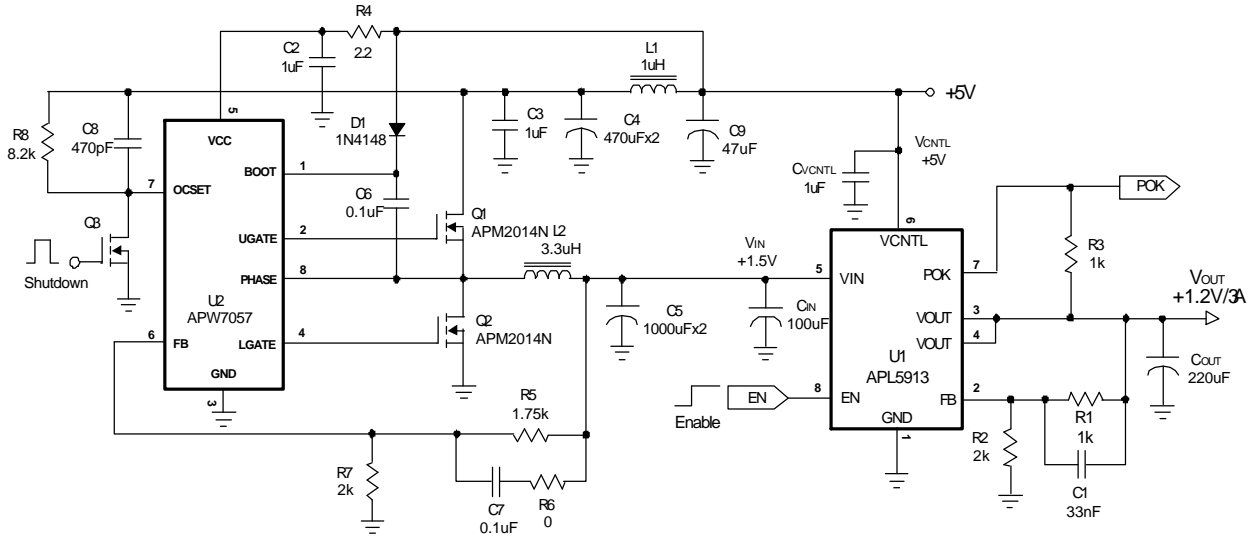
Dropout Voltage vs. Output Current



## Typical Operating Characteristics



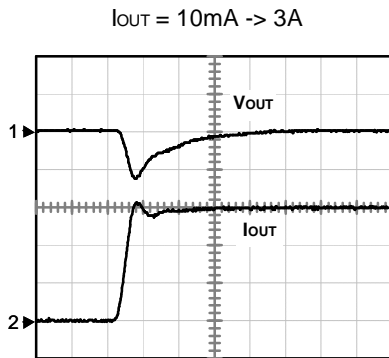
## Operating Waveforms



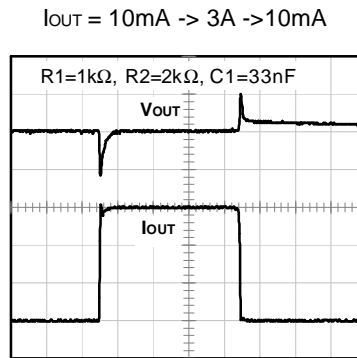
### 1. Load Transient Response :

#### 1.1 Using an Output Capacitor with $ESR \geq 18m\Omega$

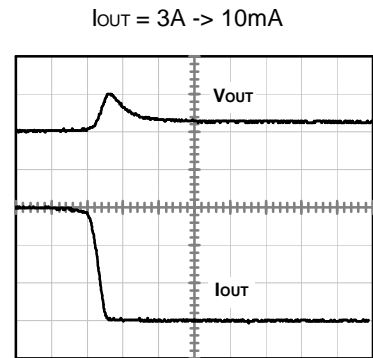
- $C_{OUT} = 220\mu F/6.3V$  ( $ESR = 30m\Omega$ ),  $C_{IN} = 100\mu F/6.3V$
- $I_{OUT} = 10mA$  to  $3A$  to  $10mA$ , Rise time = Fall time =  $1\mu S$



Ch1 : Vout, 50mV/Div  
Ch2 : Iout, 1A/Div  
Time : 2µS/Div



Ch1 : Vout, 50mV/Div  
Ch2 : Iout, 1A/Div  
Time : 20µS/Div



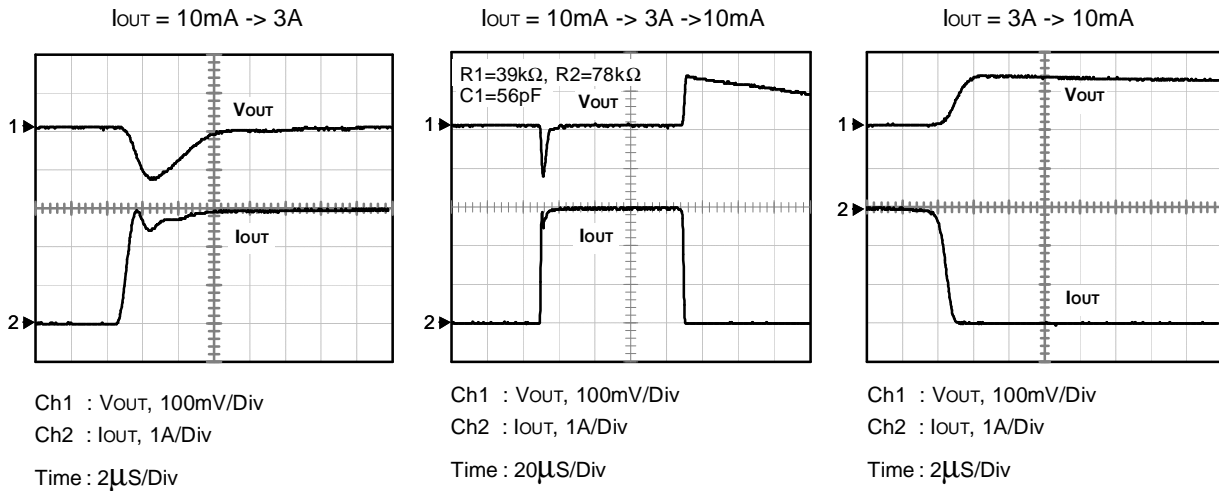
Ch1 : Vout, 50mV/Div  
Ch2 : Iout, 1A/Div  
Time : 2µS/Div



## Operating Waveforms (Cont.)

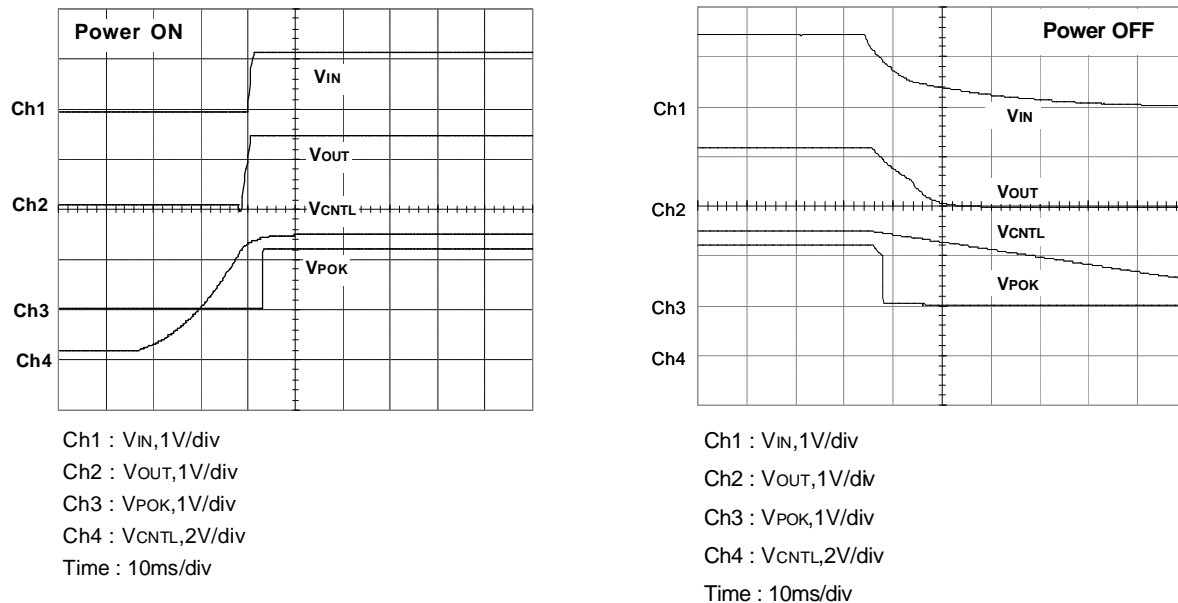
### 1.2 Using an MLCC as the Output Capacitor

- $C_{OUT} = 22\mu\text{F}/6.3\text{V}$  (ESR =  $3\text{m}\Omega$ ),  $C_{IN} = 22\mu\text{F}/6.3\text{V}$
- $I_{OUT} = 10\text{mA}$  to  $3\text{A}$  to  $10\text{mA}$ , Rise time = Fall time =  $1\mu\text{s}$



### 2. Power ON / Power OFF :

- $V_{IN} = 1.5\text{V}$ ,  $V_{CNTL} = 5\text{V}$ ,  $V_{OUT} = 1.2\text{V}$
- $C_{OUT} = 220\mu\text{F}/6.3\text{V}$  (ESR =  $30\text{m}\Omega$ ),  $C_{IN} = 100\mu\text{F}/6.3\text{V}$ ,  $R_L = 1\Omega$

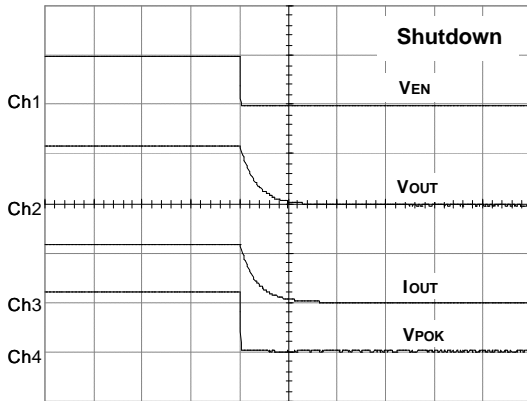


## Operating Waveforms (Cont.)

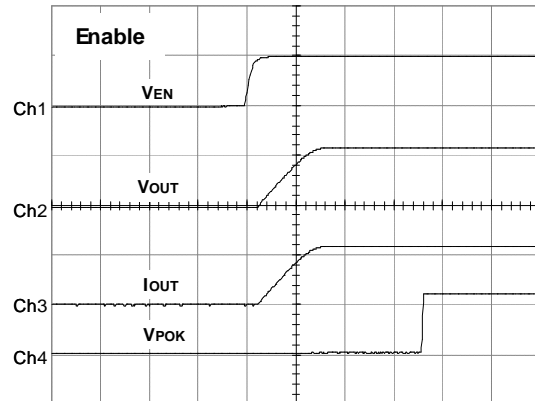
### 3. Shutdown and Enable :

-  $V_{IN} = 1.5V$ ,  $V_{CNTL} = 5V$ ,  $V_{OUT} = 1.2V$

-  $C_{OUT} = 220\mu F/6.3V$  (ESR =  $30m\Omega$ ),  $C_{IN} = 100\mu F/6.3V$ ,  $R_L = 1\Omega$



Ch1 :  $V_{EN}, 5V/div$   
 Ch2 :  $V_{OUT}, 1V/div$   
 Ch3 :  $I_{OUT}, 1A/div$   
 Ch4 :  $V_{POK}, 1V/div$   
 Time :  $1ms/div$

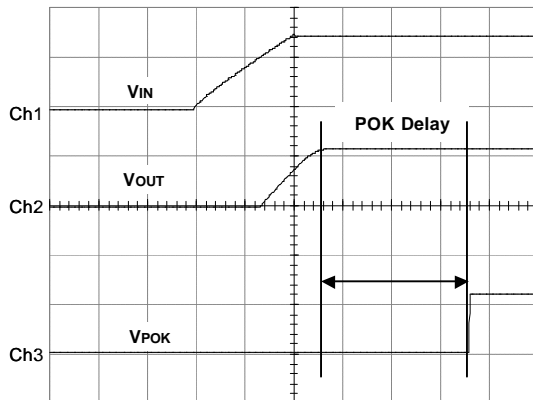


Ch1 :  $V_{EN}, 5V/div$   
 Ch2 :  $V_{OUT}, 1V/div$   
 Ch3 :  $I_{OUT}, 1A/div$   
 Ch4 :  $V_{POK}, 1V/div$   
 Time :  $1ms/div$

### 4. POK Delay :

-  $V_{IN} = 1.5V$ ,  $V_{CNTL} = 5V$ ,  $V_{OUT} = 1.2V$

-  $C_{OUT} = 220\mu F/6.3V$  (ESR =  $30m\Omega$ ),  $C_{IN} = 100\mu F/6.3V$ ,  $R_L = 1\Omega$



Ch1 :  $V_{IN}, 1V/div$   
 Ch2 :  $V_{OUT}, 1V/div$   
 Ch3 :  $V_{POK}, 1V/div$   
 Time :  $1ms/div$

## Functional Pin Description

### GND (Pin 1)

Ground pin of the circuitry. All voltage levels are measured with respect to this pin.

### FB (Pin 2)

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left( 1 + \frac{R1}{R2} \right) \quad (V)$$

where R1 is connected from VOUT to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response. The recommended R2 and R1 are in the range of 100~10kΩ.

### VOUT (Pin 3,4)

Output of the regulator. Please connect Pin 3 and 4 together using wide tracks. It is necessary to connect a output capacitor with this pin for closed-loop compensation and improving transient responses.

### VIN (Pin 5) and Exposed Pad

Main supply input pins for power conversions. The Exposed Pad provide a very low impedance input path

for the main supply voltage. Please tie the Exposed Pad and VIN Pin (Pin 8) together to reduce the dropout voltage. The voltage at this pins is monitored for Power-On Reset purpose.

### VCNTL (Pin 6)

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

### POK (Pin 7)

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the  $V_{POK}$  threshold or the falling FB voltage is below the  $V_{PNOK}$  threshold, indicating the output is not OK.

### EN (Pin 8)

Enable control pin. Pulling and holding this pin below 0.3V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. Left this pin open, an internal current source 10mA pulls this pin up to VCNTL voltage, enabling the regulator.

## Functional Description

### Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the VCNTL voltage falls below its falling POR threshold.

### Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2mS.

### Output Voltage Regulation

An error amplifier working with a temperature-compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain

## Functional Description (Cont.)

### Output Voltage Regulation (Cont.)

provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

### Current-Limit

The APL5913 monitors the current via the output NMOS and limits the maximum current to prevent load and APL5913 from damages during overload or short-circuit conditions.

### Under-Voltage Protection (UVP)

The APL5913 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disable during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the APL5913 starts a new soft-start to regulate output.

### Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5913. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed

with a 50°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device.

For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

### Enable Control

The APL5913 has a dedicated enable pin (EN). A logic low signal ( $V_{EN} < 0.3V$ ) applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new softstart cycle. Left open, this pin is pulled up by an internal current source (10 $\mu$ A typical) to enable operation. It's not necessary to use an external transistor to save cost.

### Power-OK and Delay

The APL5913 indicates the status of the output voltage by monitoring the feedback voltage ( $V_{FB}$ ) on FB pin. As the  $V_{FB}$  rises and reaches the rising Power-OK threshold ( $V_{POK}$ ), an internal delay function starts to perform a delay time. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate the output is OK. As the  $V_{FB}$  falls and reaches the falling Power-OK threshold ( $V_{PNOK}$ ), the IC immediately turns on the NMOS of the POK to indicate the output is not OK without a delay time.

## Application Information

### Power Sequencing

The power sequencing of VIN and VCNTL is not necessary to be concerned. But do not apply a voltage to VOUT for a long time when the main voltage applied at VIN is not present. The reason is the internal parasitic diode from VOUT to VIN conducts and dissipates power without protections due to the forward-voltage.

### Output Capacitor

The APL5913 requires a proper output capacitor to maintain stability and improve transient response over temperature and current. The output capacitor selection is to select proper ESR (equivalent series resistance) and capacitance of the output capacitor for good stability and load transient response.

## Application Information (Cont.)

### Output Capacitor (Cont.)

The APL5913 is designed with a programmable feedback compensation adjusted by an external feedback network for the use of wide ranges of ESR and capacitance in all applications. Ultra-low-ESR capacitors (such as ceramic chip capacitors), low-ESR bulk capacitors (such as solid Tantalum, POSCap, and Aluminum electrolytic capacitors) all can be used as an output capacitor. The value of the output capacitors can be increased without limit.

During load transients, the output capacitors, depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the APL5913 and help the device to minimize the variations of output voltage for good transient response. For the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors must be placed at the load and ground pins as close as possible and the impedance of the layout must be minimized.

### Input Capacitor

The APL5913 requires proper input capacitors to supply current surge during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents. More parasitic inductance needs more input capacitance.

Ultra-low-ESR capacitors, such as ceramic chip capacitors, are very good for the input capacitors. An aluminum electrolytic capacitor (>100mF, ESR <300mΩ) is recommended as the input capacitor. It is not necessary to use low-ESR capacitors. More capacitance reduce the variations of the input voltage of VIN pin.

### Feedback Network

Figure 1 shows the feedback network between VOUT, GND and FB pins. It works with the internal error amplifier to provide proper frequency response for the linear regulator. The ESR is the equivalent series resistance of the output capacitor. The C<sub>OUT</sub> is ideal capacitance in the output capacitor. The V<sub>OUT</sub> is the setting of the output voltage.

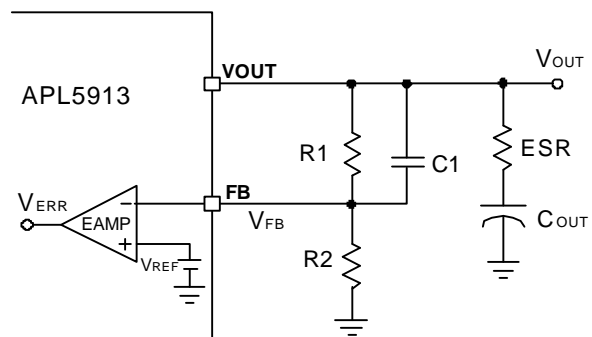


Figure 1

The feedback network selection depends on the values of the ESR and C<sub>OUT</sub>, which has been classified into three conditions:

- **Condition 1 : Large ESR ( ≥18mΩ )**
  - Select the R1 in the range of 400Ω ~ 2.4kΩ
  - Calculate the R2 as the following :

$$R2(k\Omega) = R1(k\Omega) \cdot \frac{0.8(V)}{V_{OUT(V)} - 0.8(V)} \dots\dots\dots (1)$$

- Calculate the C1 as the following :

$$10 \cdot \frac{V_{OUT(V)}}{R1(k\Omega)} \leq C1(nF) \leq 40 \cdot \frac{V_{OUT(V)}}{R1(k\Omega)} \dots\dots\dots (2)$$

- **Condition 2 : Middle ESR**

- Calculate the R1 as the following:

$$R1(k\Omega) = \frac{2157}{ESR(m\Omega)} - 37.5 \cdot V_{OUT(V)} + 15 \dots\dots\dots (3)$$

## Application Information (Cont.)

### Feedback Network (Cont.)

Select a proper R1(selected) to be a little larger than the calculated R1.

- Calculate the C1 as the following :

$$C1_{(pF)} = [0.71 \cdot ESR_{(m\Omega)} + 101] \cdot \frac{C_{OUT(uF)}}{R1_{(k\Omega)}} \dots\dots (4)$$

Where R1=R1(selected)

Select a proper C1(selected) to be a little smaller than the calculated C1.

- The C1 calculated from equation (4) must meet the following equation:

$$C1_{(pF)} \geq 7.2 \cdot \left[ 1 + \frac{143}{ESR_{(m\Omega)}} \right] \cdot \left[ 1 + \frac{37.5 \cdot V_{OUT(V)}}{R1_{(k\Omega)}} \right] \dots (5)$$

Where R1=R1(calculated) from equation (3)

**If the C1(calculated) can not meet the equation (5), please use the Condition 3.**

- Use equation (2) to calculate the R2.

- **Condition 3 : Low ESR (eg. Ceramic Capacitors)**

- Calculate the R1 as the following:

$$R1_{(k\Omega)} = \sqrt{(2.1 \cdot ESR_{(m\Omega)} + 300) \cdot C_{OUT(uF)} - 37.5 \cdot V_{OUT(V)}} \dots (6)$$

Select a proper R1(selected) to be a little larger than the calculated R1. **The minimum selected R1 is equal to 1kΩ when the calculated R1 is smaller than 1k or negative.**

- Calculate the C1 as the following :

$$C1_{(pF)} = \sqrt{(0.24 \cdot ESR_{(m\Omega)} + 34.2) \cdot C_{OUT(uF)}} \cdot \left[ 1 + \frac{37.5 \cdot V_{OUT(V)}}{R1_{(k\Omega)}} \right] \dots (7)$$

Where R1=R1(selected)

Select a proper C1(selected) to be a little smaller than the calculated C1.

- The C1 calculated from equation (7) must meet the following equation :

$$C1_{(pF)} \geq \left[ 0.033 + \frac{1.25 \cdot V_{OUT(V)}}{R1_{(k\Omega)}} \right] \cdot ESR_{(m\Omega)} \cdot C_{OUT(uF)} \dots (8)$$

Where R1=R1(calculated) from equation (6)

**If the C1(calculated) can not meet the equation (8), please use the Condition 2.**

- Use equation (2) to calculate the R2.

The reason to have three conditions described above is to optimize the load transient responses for all kinds of the output capacitor. For stability only, the Condition 2, regardless of equation (5), is enough for all kinds of output capacitor.

### PCB Layout Considerations (See Figure 2)

1. Please solder the Exposed Pad and VIN together on the PCB. The main current flow is through the exposed pad. Refer Figure 3 to make a proximate topology.
2. Please place the input capacitors for VIN and VCNTL pins near pins as close as possible.
3. Ceramic decoupling capacitors for load must be placed near the load as close as possible.
4. To place APL5913 and output capacitors near the load is good for performance.
5. The negative pins of the input and output capacitors and the GND pin of the APL5913 are connected to the ground plane of the load.
6. Please connect PIN 3 and 4 together by a wide track.
7. Large current paths must have wide tracks.
8. See the Typical Application (see next page Figure 2)
  - Connect the one pin of the R2 to the GND of APL5913
  - Connect the one pin of R1 to the Pin 3 of APL5913
  - Connect the one pin of C1 to the Pin 3 of APL5913

## Application Information (Cont.)

### PCB Layout Considerations (Cont.)

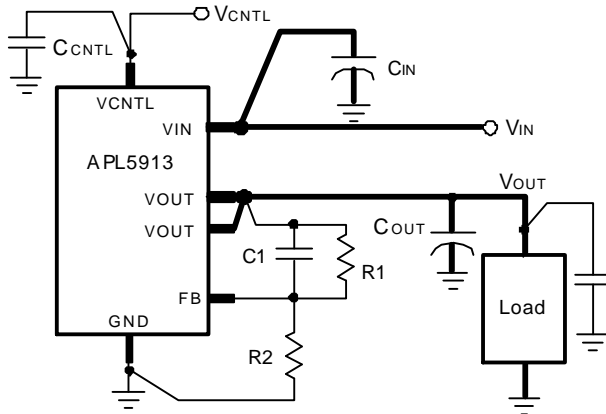


Figure 2

### Thermal Considerations

See Figure 3. The SOP-8-P is a cost-effective package featuring a small size like a standard SOP-8 and a bottom exposed pad to minimize the thermal resistance of the package, being applicable to high current applications. The exposed pad must be soldered to the top  $V_{IN}$  plane. The copper of the  $V_{IN}$  plane on the Top layer conducts heat into the PCB and air. Please enlarge the area to reduce the case-to-ambient resistance ( $\theta_{CA}$ ).

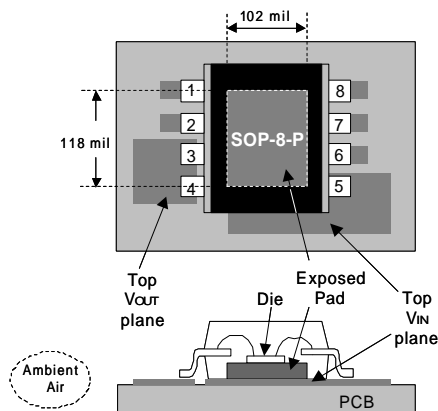
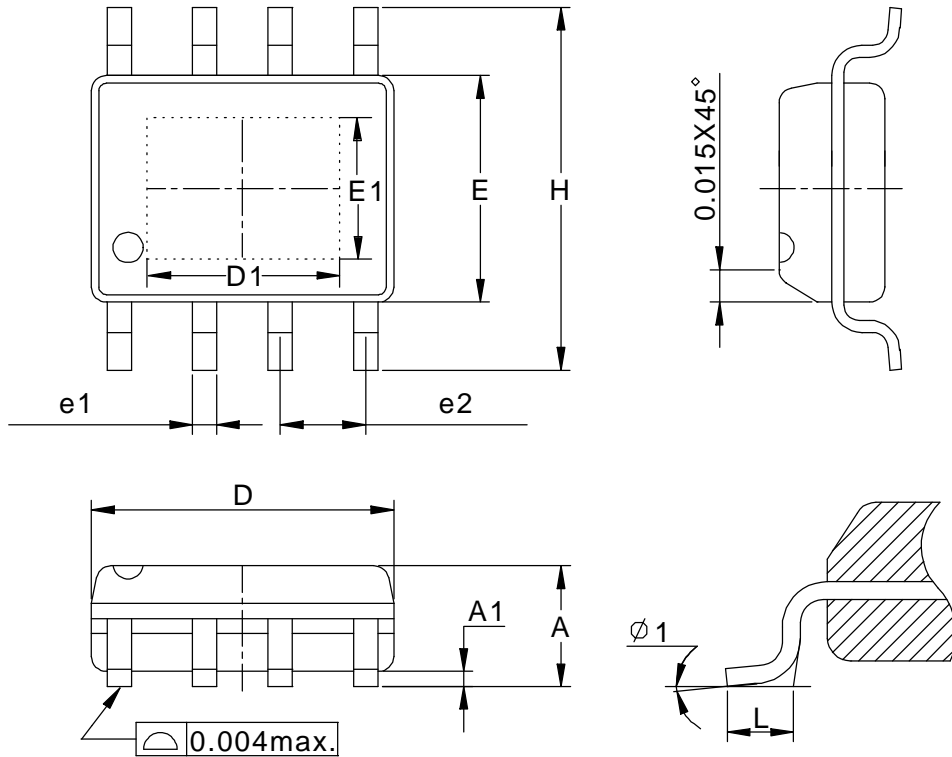


Figure 3

## Packaging Information

SOP-8-P pin ( Reference JEDEC Registration MS-012)



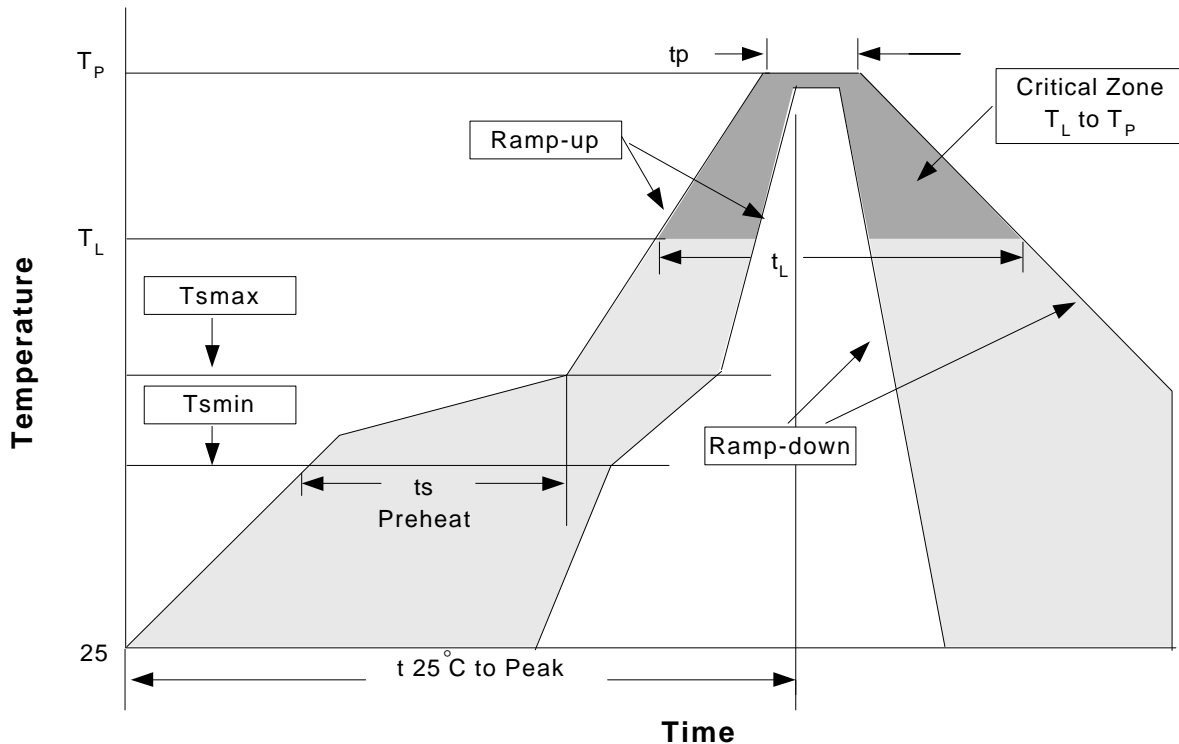
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
φ 1	8°		8°	



## Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

### Reflow Condition (IR/Convection or VPR Reflow)



### Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate ( $T_L$ to $T_P$ )	3°C/second max.	3°C/second max.
Preheat <ul style="list-style-type: none"> <li>- Temperature Min (<math>T_{smin}</math>)</li> <li>- Temperature Max (<math>T_{smax}</math>)</li> <li>- Time (min to max) (<math>t_s</math>)</li> </ul>	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: <ul style="list-style-type: none"> <li>- Temperature (<math>T_L</math>)</li> <li>- Time (<math>t_L</math>)</li> </ul>	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature ( $T_p$ )	See table 1	See table 2
Time within 5°C of actual Peak Temperature ( $t_p$ )	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

(mm)

## Classification Reflow Profiles(Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

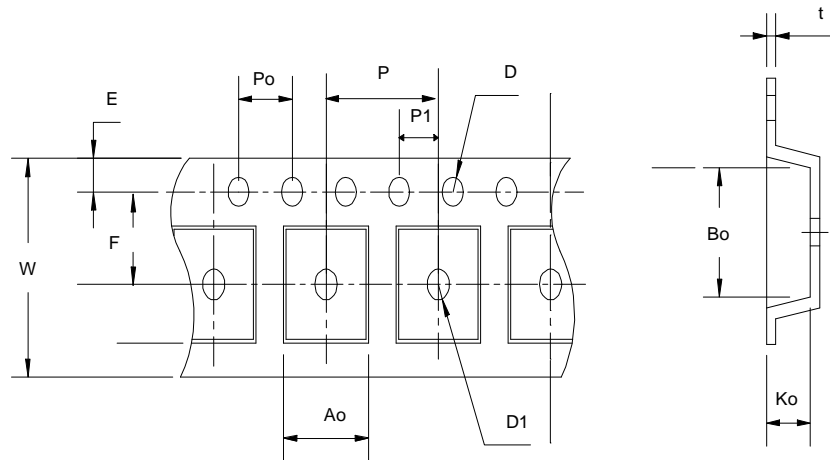
Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

\*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

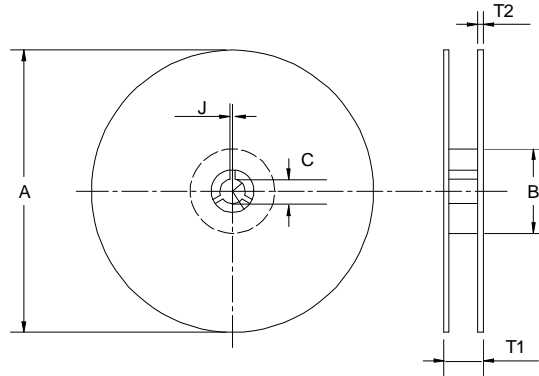
## Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> > 100mA

## Carrier Tape & Reel Dimensions



### Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8/-P	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0.3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0.1	2.1± 0.1	0.3±0.013

(mm)

### Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8/-P	12	9.3	2500

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