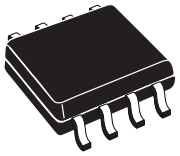
STSJ50NH3LL

N-channel 30V - 0.008Ω - 12A - PowerSO-8™
Ultra low gate charge STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STSJ50NH3LL	30V	< 0.0105Ω	12A(1)

- Optimal $R_{DS(on)}$ x Qg trade-off @ 4.5V
- Reduced switching losses
- Reduced conduction losses
- Improved junction-case thermal resistance

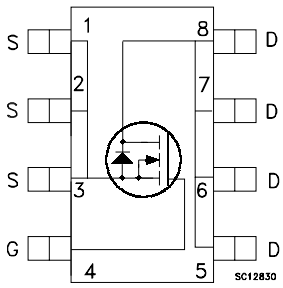


PowerSO-8™

Description

This series utilizes the latest advanced design rules of ST's proprietary STripFET™ technology, and a propriertary process for integrating a monolithic Scottky diode. The new Power MOSFET is optimized for the most demanding synchronous switch function in DC-DC converter for Computer and Telecom.

Internal schematic diagram



DRAIN CONTACT ALSO ON THE BACKSIDE

Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STSJ50NH3LL	50H3LL-	PowerSO-8	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}(1)	Gate-source voltage	±16	V
V_{GS}(2)	Gate-source voltage	±18	V
I_D(4)	Drain current (continuous) at T_C = 25°C	50	A
I_D(3)	Drain current (continuous) at T_C=25°C	12	A
I_D(4)	Drain current (continuous) at T_C=100°C	31.3	A
I_D(3)	Drain current (continuous) at T_C=100°C	7.5	A
I_{DM}(5)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25°C (3) Total dissipation at T_C = 25°C (4)	3 50	W W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Continuous mode
2. Guaranteed for test time ≤ 15ms
3. This value is rated accordingly to Rthj-pcb
4. This value is rated accordingly to Rthj-c
5. Pulse width limited by safe operating area

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}c}$	Thermal resistance junction-case Max	2.5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb Max	42	°C/W

1. When mounted on 1 inch² FR-4 board, 2oz Cu (t<10sec.)

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not repetitive avalanche current (pulse width limited by Tjmax)	6	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AV}, V_{DD}=24V)	800	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating T_C=125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D =250µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 6A V_{GS}= 4.5V, I_D= 6A		0.008 0.010	0.0105 0.013	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 6A @125°C V_{GS}= 4.5V, I_D= 6A @125°C		0.012 0.016		Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =10V, I_D = 12A		38		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1MHz, V_{GS}=0		965 285 38		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15V, I_D =12A V_{GS} =4.5V,(see Figure 15)		9 3.7 3	12	nC nC nC
R_G	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level =20mv open drain	0.5	1.5	2.5	Ω

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=15V, I_D=6A, R_G=4.7Ω, V_{GS}=4.5V (see Figure 14)		15 32		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=15V, I_D=6A, R_G=4.7Ω, V_{GS}=4.5V (see Figure 14)		18 8.5		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				12 48	A A
V_{SD}(2)	Forward on voltage	I_{SD}=12A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=12A, di/dt = 100A/µs, V_{DD}=20V, Tj=150°C (see Figure 19)		24 17.4 1.45		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

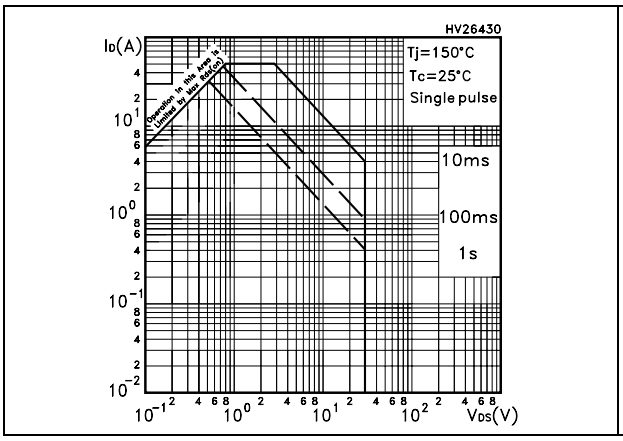


Figure 2. Thermal impedance

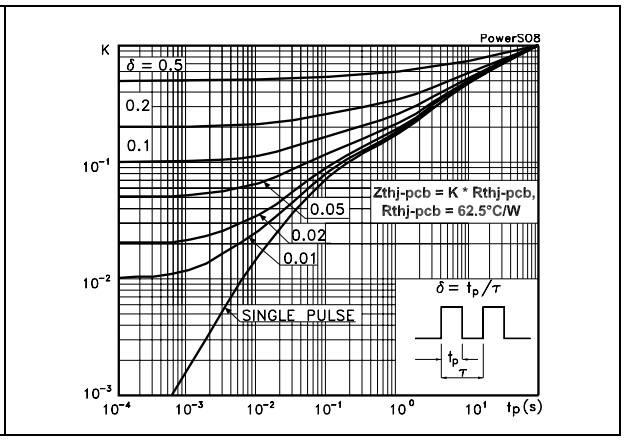


Figure 3. Output characterisics

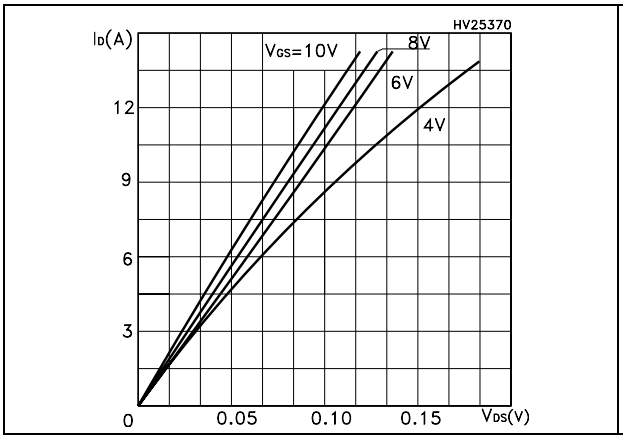


Figure 4. Transfer characteristics

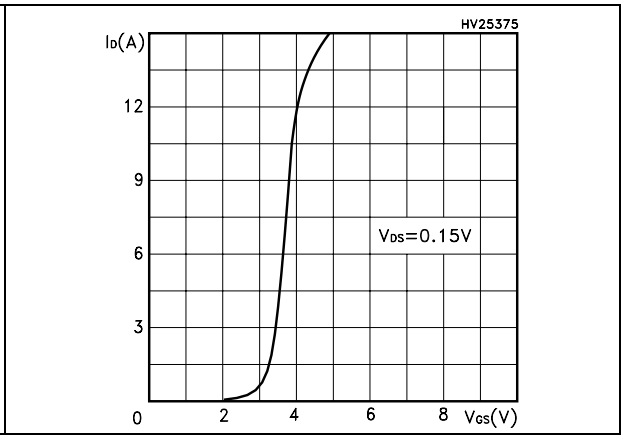


Figure 5. Transconductance

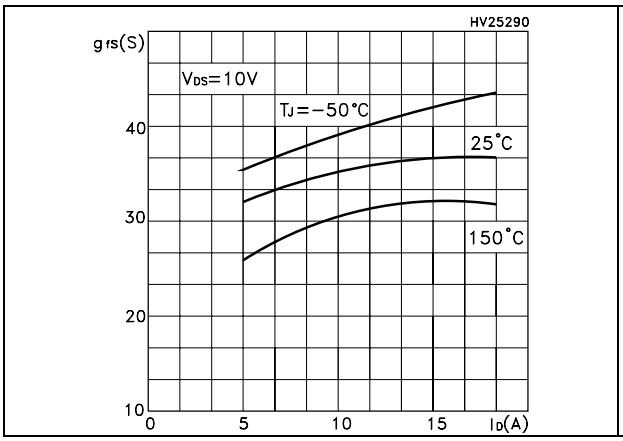


Figure 6. Static drain-source on resistance

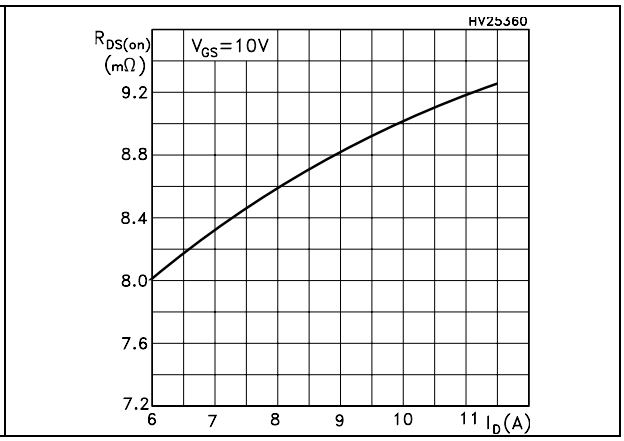


Figure 7. Gate charge vs gate-source voltage

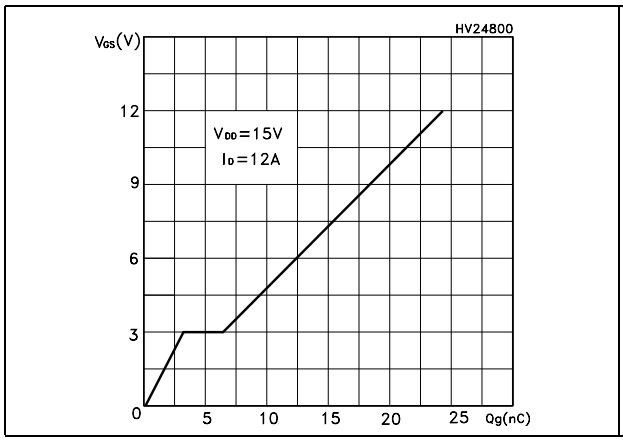


Figure 8. Capacitance variations

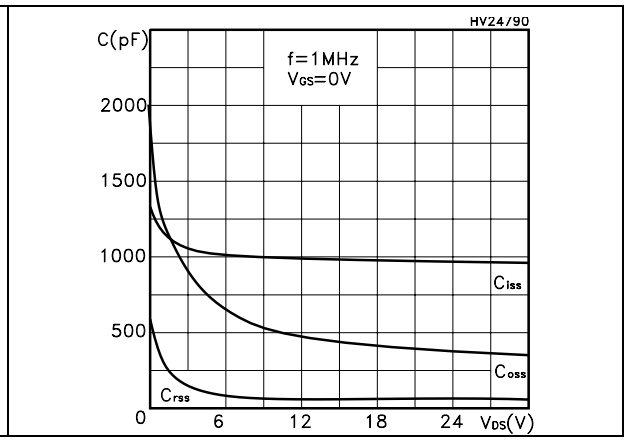


Figure 9. Normalized gate threshold voltage vs temperature

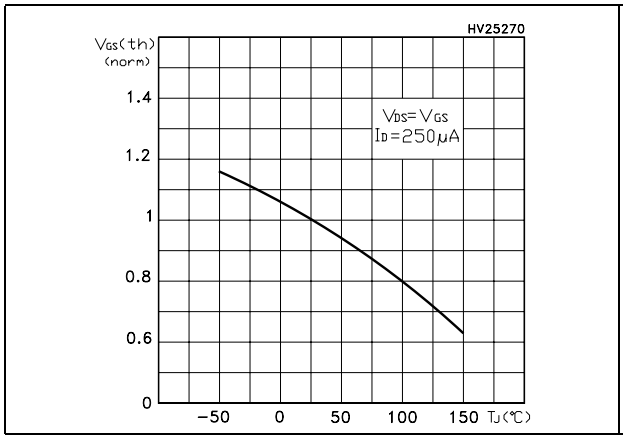


Figure 10. Normalized on resistance vs temperature

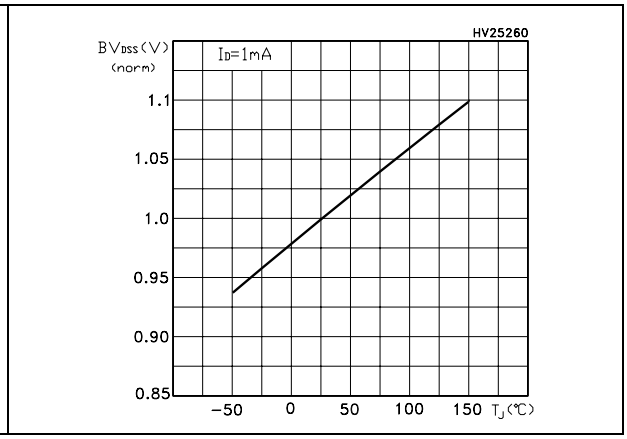


Figure 11. Source-drain diode forward characteristics

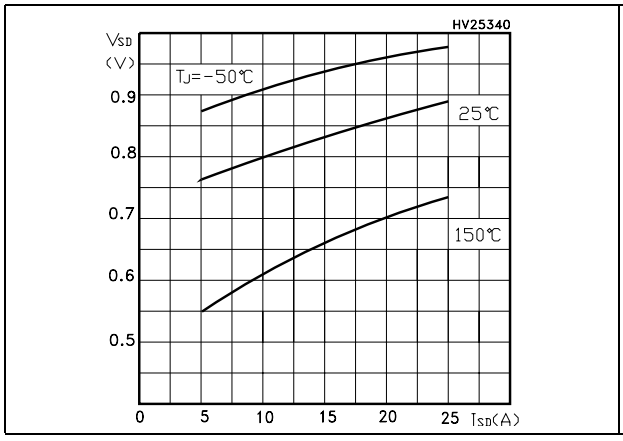


Figure 12. Normalized B_{VDSS} vs temperature

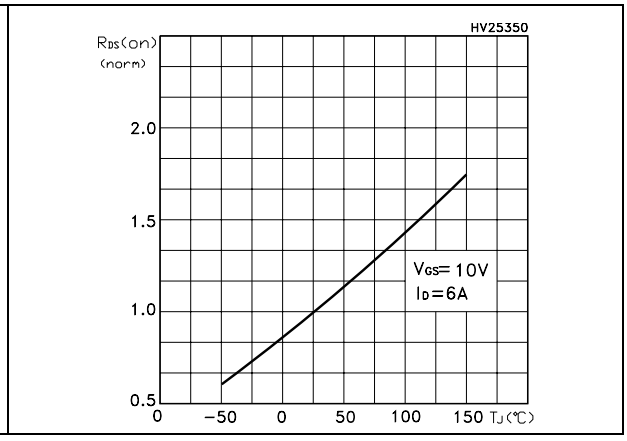
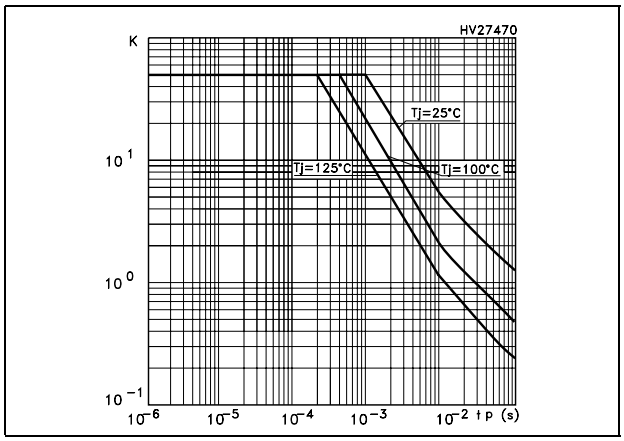


Figure 13. Allowable Iav vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads under the following conditions:

$P_{D(AVE)} = 0.5*(1.3*BV_{DSS} *I_{AV})$

$EAS_{(AR)} = P_{D(AVE)} *t_{AV}$

Where:

I_{AV} is the Allowable Current in Avalanche

$P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

3 Test circuit

Figure 14. Switching times test circuit for resistive load

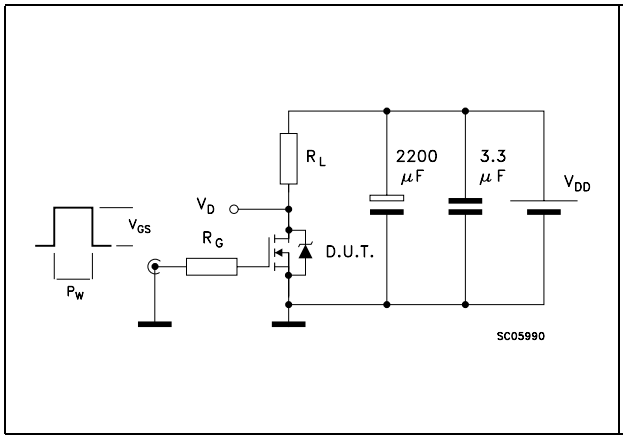


Figure 15. Gate charge test circuit

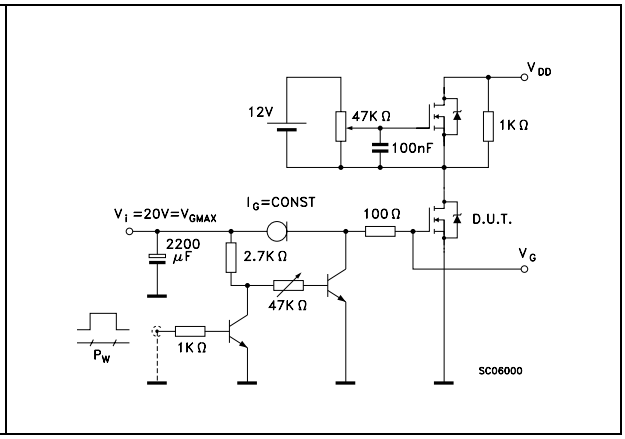


Figure 16. Test circuit for inductive load switching and diode recovery times

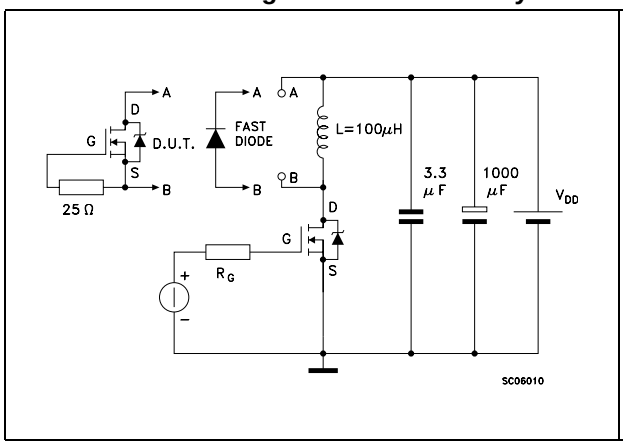


Figure 17. Unclamped inductive load test circuit

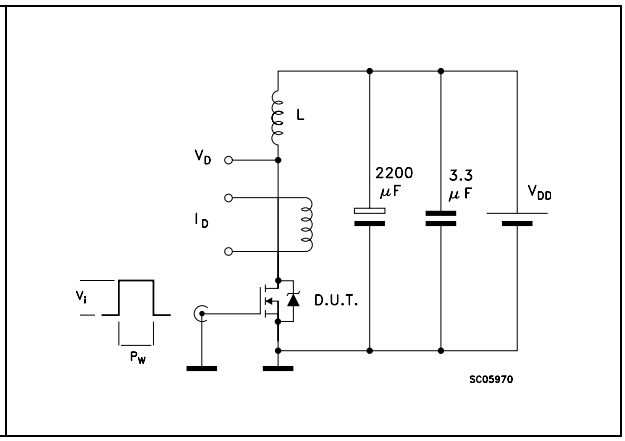


Figure 18. Unclamped inductive waveform

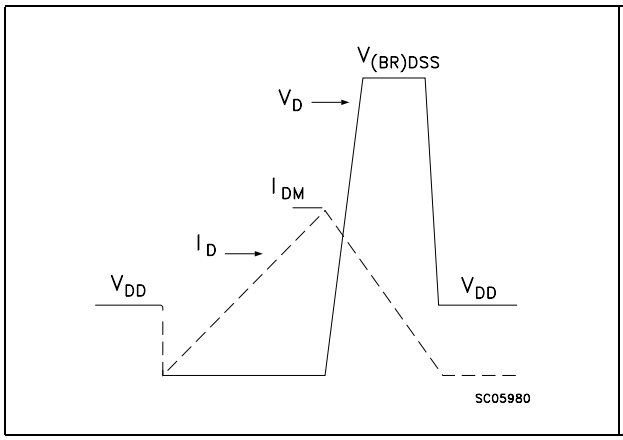
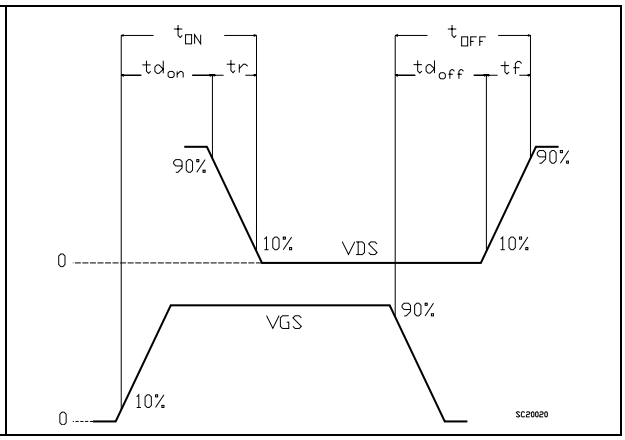


Figure 19. Switching time waveform

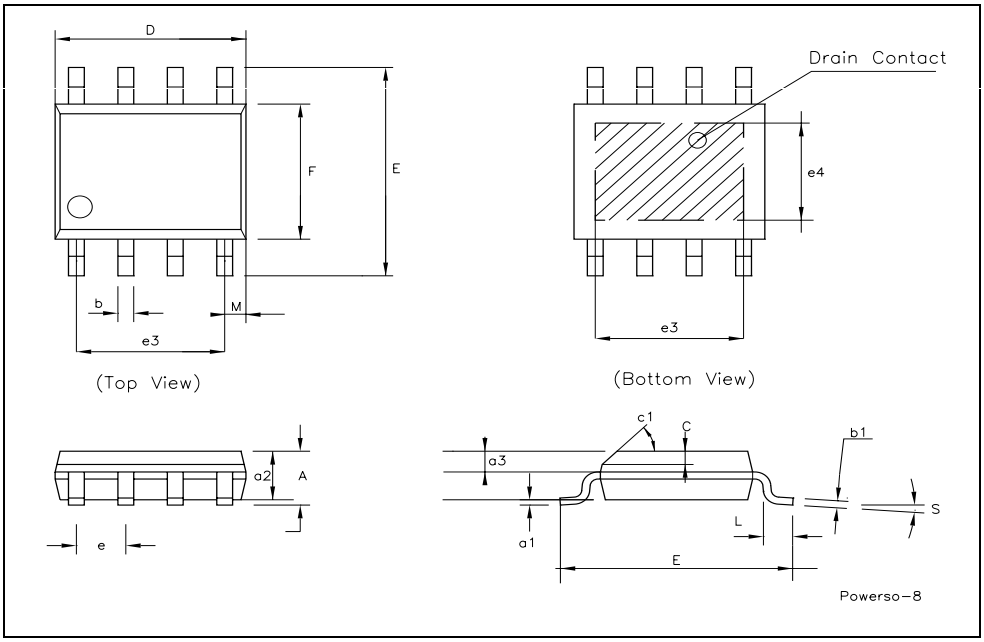


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerSO-8™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



5 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jul-2004	1	Initial release.
24-May-2005	2	New value on *Table 6*
23-Jun-2005	3	New Rg value on *Table 6*
16-Nov-2005	4	Complete version
03-Apr-2006	5	New template

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