

SP8720

300MHz ÷ 3/4

The SP8720 is an ECL two-modulus divider, with ECL10K compatible outputs. It divides by 3 when either of the ECL control inputs, PE1 or PE2, is in the high state and by 4 when both are low (or open circuit). An AC coupled input of 600mVp-p is required.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Input (Internal Bias)
- Control Inputs ECL III/10K Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
 - 55°C to +125°C (A Grade)
 - 30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

| | |
|---------------------------|-----------------|
| Supply voltage | -8V |
| Output current | 20mA |
| Storage temperature range | -65°C to +150°C |
| Max. junction temperature | +175°C |
| Max. clock input voltage | 2.5V p-p |

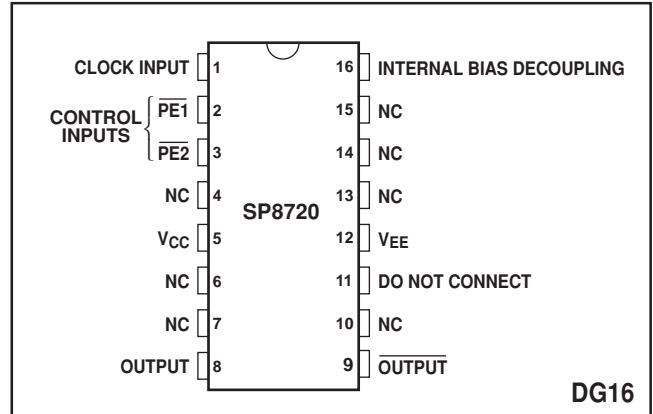


Fig. 1 Pin connections - top view

ORDERING INFORMATION

SP8720 A DG
SP8720 B DG
5962-90577 (SMD)

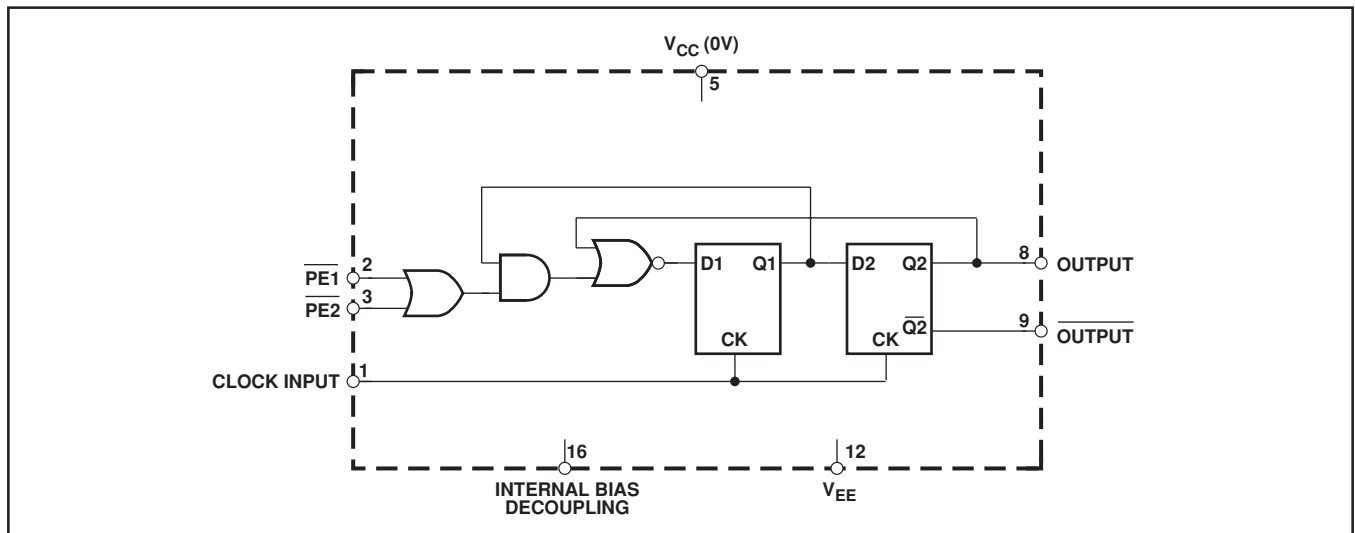


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage, $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 0.25V$

Temperature, $T_{AMB} = -55^{\circ}C$ to $+125^{\circ}C$ (A Grade), $-30^{\circ}C$ to $+70^{\circ}C$ (B Grade)

| Characteristic | Symbol | Value | | Units | Conditions | Notes |
|------------------------------------|-----------|-------|-------|-------|-------------------------|-------|
| | | Min. | Max. | | | |
| Maximum frequency (sinewave input) | f_{MAX} | 300 | | MHz | Input = 400-800mV p-p | 5 |
| Minimum frequency (sinewave input) | f_{MIN} | | 40 | MHz | Input = 400-800mV p-p | 5 |
| Power supply current | I_{EE} | | 65 | mA | $V_{EE} = -5.2V$ | 5 |
| Output high voltage | V_{OH} | -0.85 | -0.7 | V | $V_{EE} = -5.2V$ (25°C) | |
| Output low voltage | V_{OL} | -1.8 | -1.5 | V | $V_{EE} = -5.2V$ (25°C) | |
| PE input high voltage | V_{INH} | -0.93 | | V | $V_{EE} = -5.2V$ (25°C) | |
| PE input low voltage | V_{INL} | | -1.62 | V | $V_{EE} = -5.2V$ (25°C) | |
| Clock to output delay | t_p | | 6 | ns | | 6 |
| Set-up time | t_s | 2.5 | | ns | | 3, 6 |
| Release time | t_r | 3 | | ns | | 4, 6 |

NOTES

1. The temperature coefficients of $V_{OH} = +1.63mV/^{\circ}C$, $V_{OL} = +0.94mV/^{\circ}C$ and of $V_{IN} = +1.22mV/^{\circ}C$.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷3 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷4 mode is obtained.
5. SP8720B tested at 25°C only.
6. Guaranteed but not tested.

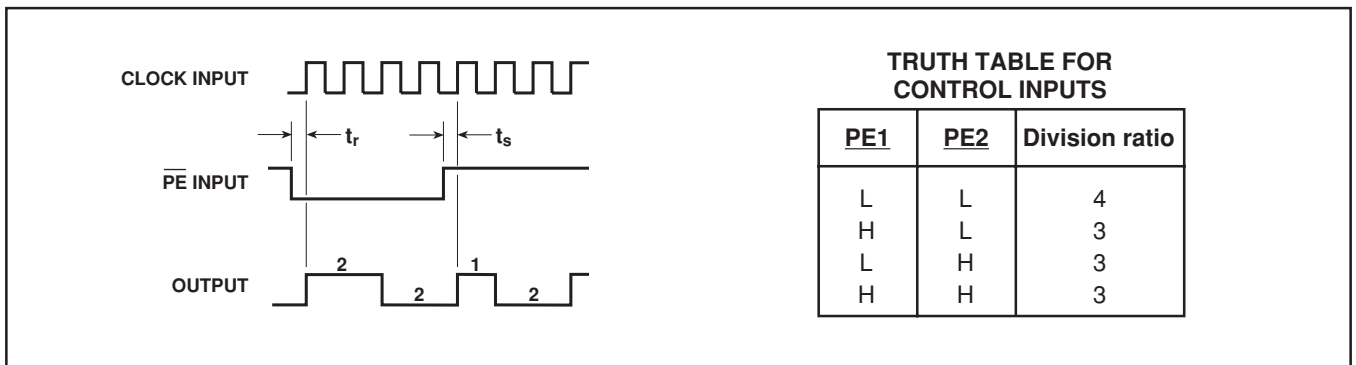


Fig. 3 Timing diagram

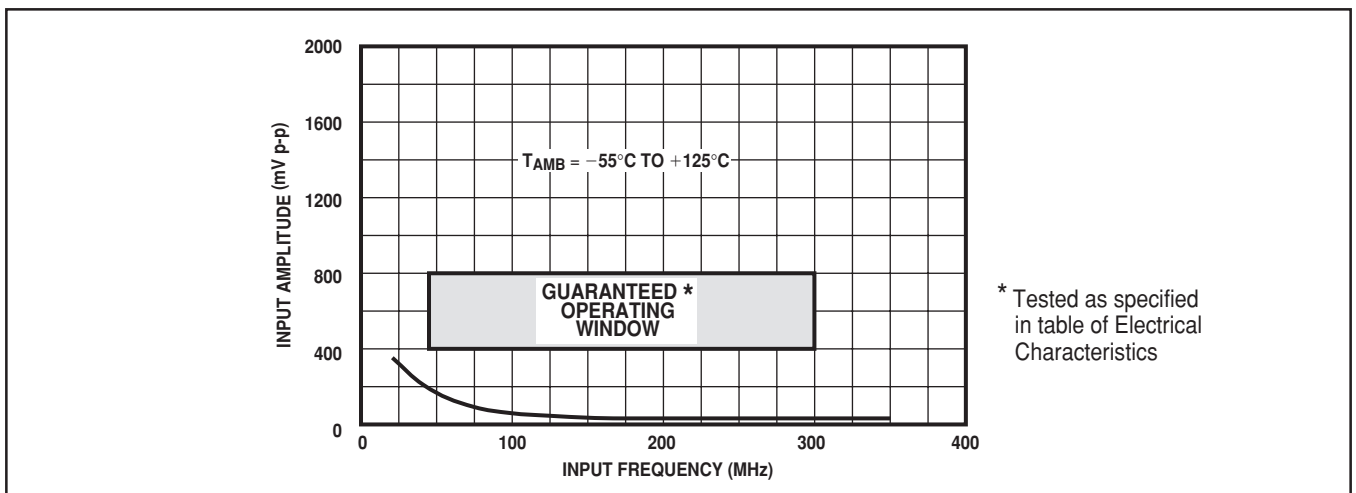


Fig. 4 Typical input characteristic of SP8720A

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected from pin 16 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the clock input (pin 1) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better

- than 100V/μs.
4. The Q and \bar{Q} outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2kΩ at each output.
5. The PE inputs are ECLIII/10K compatible and include 4.3kΩ pulldown resistors. Unused inputs can therefore be left open.
6. The input impedance of the SP8720 varies as a function of frequency, see Fig. 5.
7. All components should be suitable for the frequency in use.

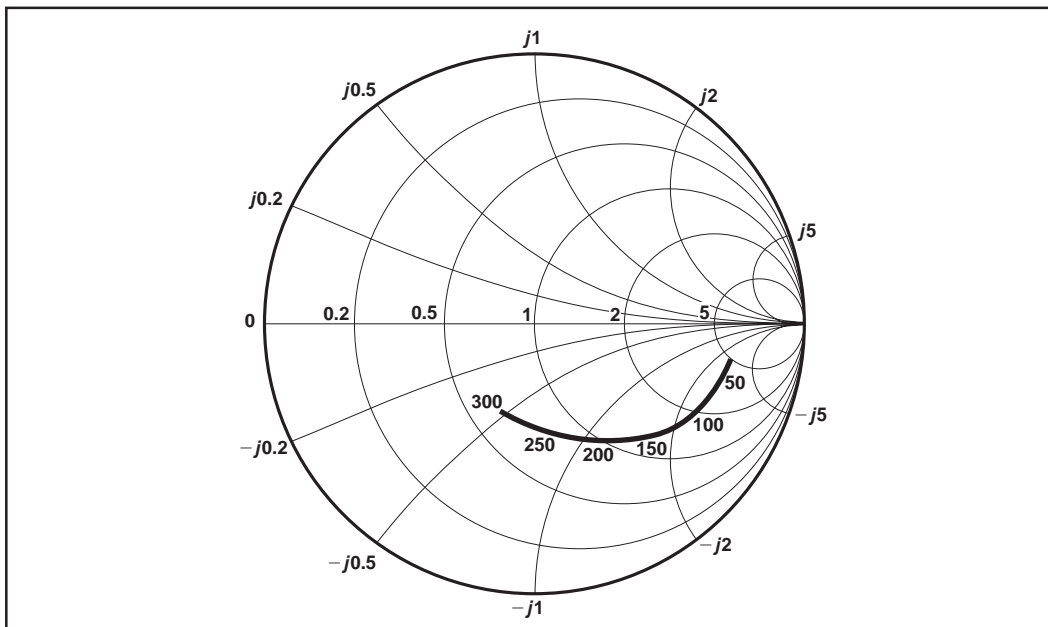


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = -5.2V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

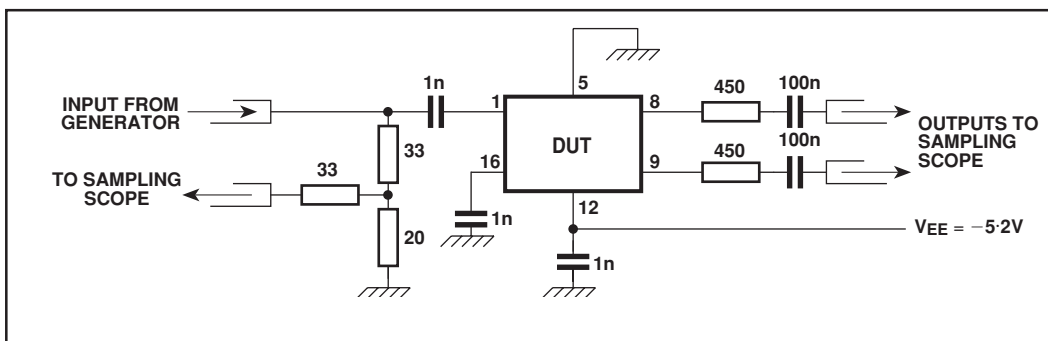


Fig. 6 Test circuit

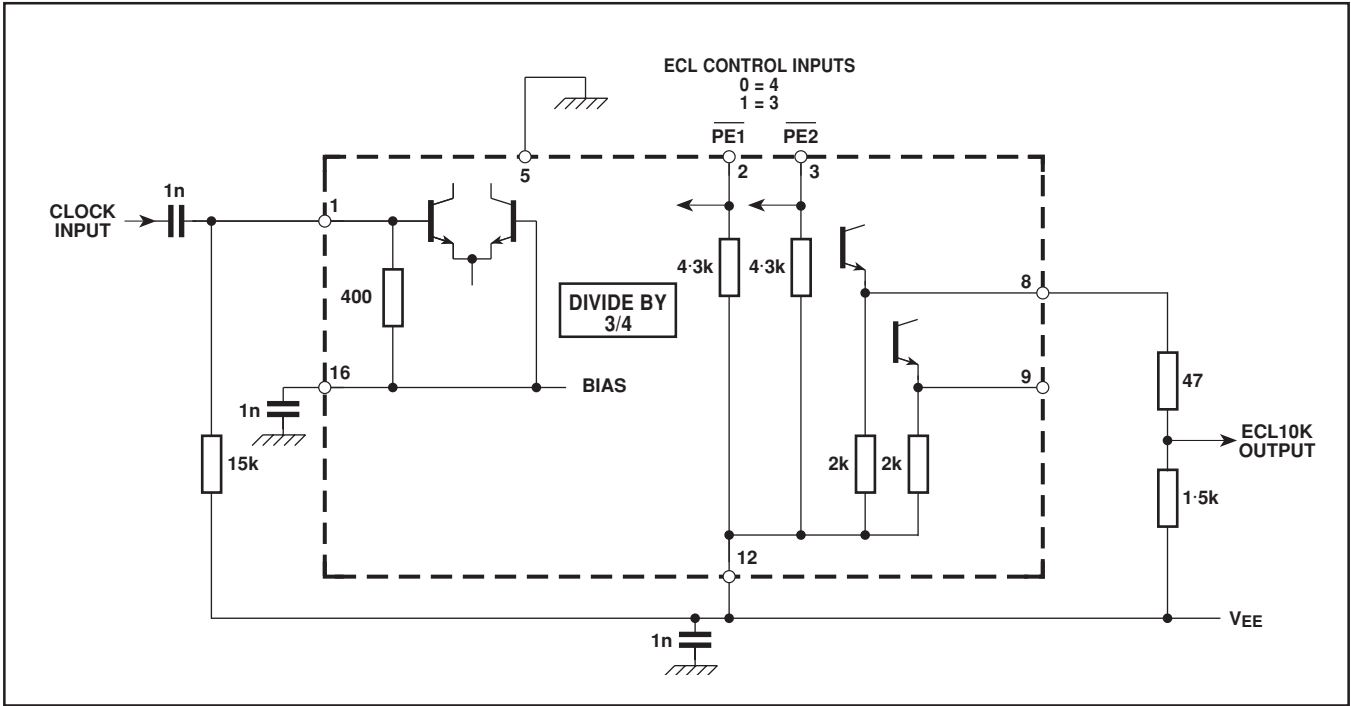
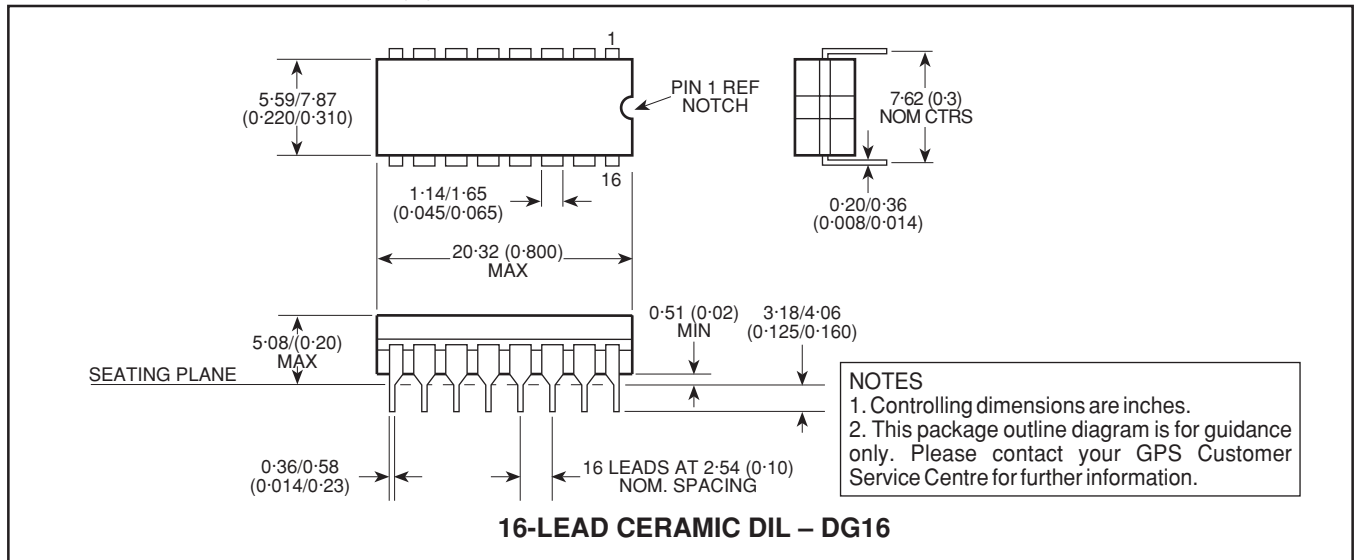


Fig. 7 Typical application circuit showing interfacing

NOTES

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



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