P-Channel JFET Switch

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J174 – J177 / SST174 – SST177

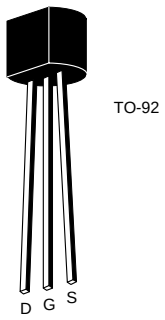
FEATURES

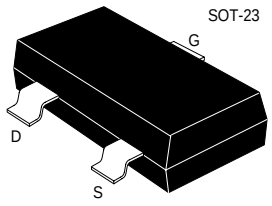
- **Low Insertion Loss**
- **No Offset or Error Generated By Closed Switch**
  - **Purely Resistive**
  - **High Isolation Resistance From Driver**
- **Short Sample and Hold Aperture Time**
- **Fast Switching**

APPLICATIONS

- **Analog Switches**
- **Choppers**
- **Commutators**

PIN CONFIGURATION





5508

PRODUCT MARKING (SOT-23)	
SST174	P04
SST175	P05
SST176	P06
SST177	P07

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage 30V
Gate Current 50mA
Storage Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -55°C to +135°C
Lead Temperature (Soldering, 10sec) . . . . . 300°C
Power Dissipation 350mW
Derate above 25°C . . . . . 3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
J174-J177	Plastic TO-92	-55°C to +135°C
SST174-SST177	Plastic SOT-23	-55°C to +135°C

For Sorted Chips in Carriers see 2N5114 series.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	J174			J175			J176			J177			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate Reverse Current (Note 1)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20V	
$V_{GS(off)}$	Gate Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15V, I_D = -10nA	
BV_{GSS}	Gate Source Breakdown Voltage	30			30			30			30				V_{DS} = 0, I_G = 1µA	
I_{DSS}	Drain Saturation Current (Note 2)	-20		-135	-7		-70	-2		-35	-1.5		-20	mA	V_{DS} = -15V, V_{GS} = 0	
$I_{D(off)}$	Drain Cutoff Current (Note 1)			-1			-1			-1			-1	nA	V_{DS} = -15V, V_{GS} = 10V	
$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = -0.1V	
$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10V	f = 1MHz (Note 3)
$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5				
$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source Gate ON Capacitance		32			32			32			32			V_{DS} = V_{GS} = 0	
$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions (Note 3)	
t_r	Rise Time		5			10			20			25				
$t_{d(off)}$	Turn Off Delay Time		5			10			15			20				
t_f	Fall Time		10			20			20			25				

	J174	J175	J176	J177
V_{DD}	-10V	-6V	-6V	-6V
$V_{GS(off)}$	12V	8V	3V	3V
R_L	560Ω	12kΩ	5.6kΩ	10kΩ
$V_{GS(on)}$	0V	0V	0V	0V

NOTES: **1.** Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration -300µs; duty cycle ≤3%.
3. For design reference only, not 100% tested.