SRAM MODULE 2Mbyte (512K x 32-Bit), 68-Pin JLCC Packaging
Part No. HMS51232J4A

GENERAL DESCRIPTION

The HMS51232J4A is a static random access memory (SRAM) module containing 524,288 words organized in a x32-bit configuration. The module consists of four 512K x 8 SRAMs mounted on a 68-pin, single-sided, FR4-printed circuit board. Four chip enable inputs, (/CE1, /CE2, /CE3 and /CE4) are used to enable the module's 4 bytes independently. Output enable(/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW. Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

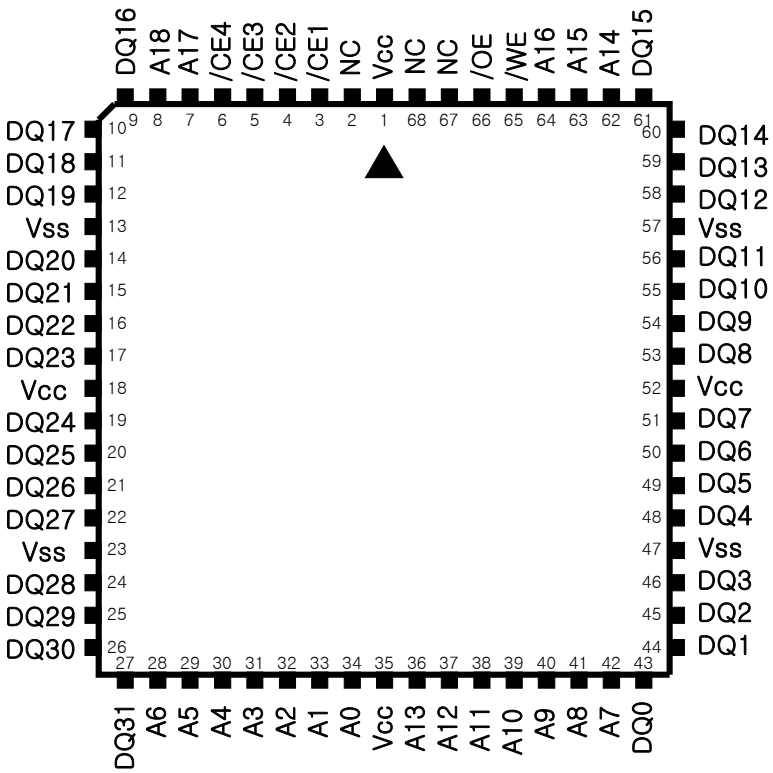
For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

FEATURES

- Access time : 10, 12 and 15ns
- High-density 2MByte design
- High-reliability, low-power design
- Single +5V ±0.5V power supply
- Three state output and TTL-compatible
- FR4-PCB design
- Low profile 68-Pin JLCC

OPTIONS	MARKING
◆ Timing	
10ns access	-10
12ns access	-12
15ns access	-15
◆ Packages	
68-pin JLCC	J

PIN ASSIGNMENT

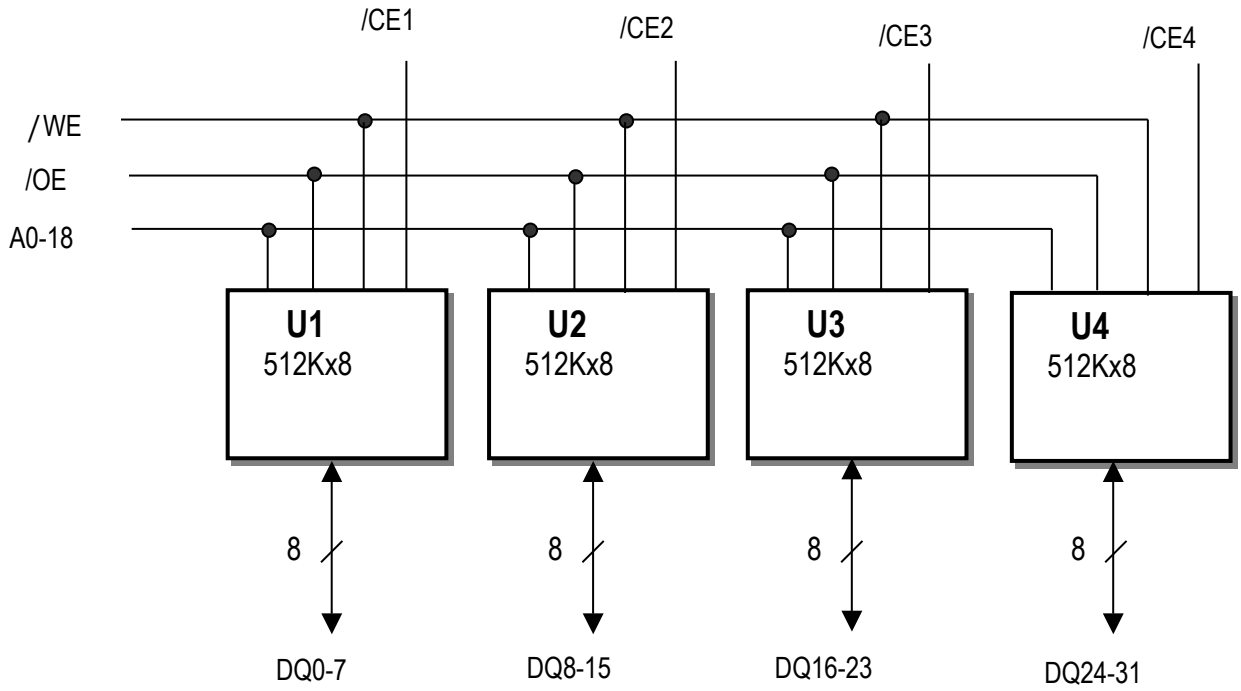


68-Pin JLCC
TOP VIEW

PIN DESCRIPTION

DQ0 – DQ31	Data Inputs/Outputs
A0 – A18	Address Inputs
/WE	Write Enable
/CE1-4	Chip Selects
/OE	Output Enable
Vcc	Power Supply
Vss	Ground

BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE	X	L	L	Din	ACTIVE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to +7.0V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +7.0V
Power Dissipation	P_D	4W
Storage Temperature	T_{STG}	-55°C to +125°C
Operating Temperature	T_A	0°C to +70°C

- Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 ° C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5V**
Input Low Voltage	V_{IL}	-0.5*	-	0.8V

* V_{IL}(Min.) = -2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

** V_{IH}(Max.) = Vcc+2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)(0°C ≤ T_A ≤ 70 °C ; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{IN} = Vss to Vcc	IL_I	-4	4	μA
Output Leakage Current	/CE=V_{IH} or /OE =V_{IH} or /WE=V_{IL} V_{OUT}=Vss to V_{CC}	IL_0	-4	4	μA
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4	-	V
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V

* Vcc=5.0V, Temp=25 °C

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX			UNIT
			-10	-12	-15	
Power Supply Current: Operating	Min. Cycle, 100% Duty /CE=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	I_{CC}	840	820	800	mA
Power Supply Current: Standby	Min. Cycle, /CE=V_{IH}	I_{SB}	200	200	200	mA
	f=0MHZ, /CE≥V_{CC}-0.2V, V_{IN}≥ V_{CC}-0.2V or V_{IN}≤0.2V	I_{SB1}	40	40	40	mA

CAPACITANCE

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	28	pF
Input Capacitance	V_{IN}=0V	C_{IN}	20	pF

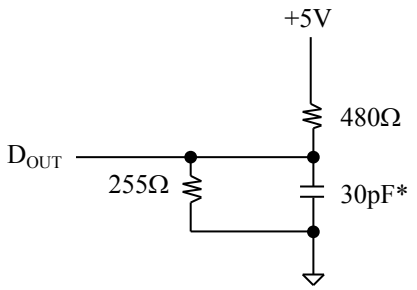
* **NOTE** : Capacitance is sampled and not 100% tested

AC CHARACTERISTICS ($0^{O}C \leq T_A \leq 70\ ^{O}C$; Vcc = 5V ± 0.5V, unless otherwise specified)

TEST CONDITIONS

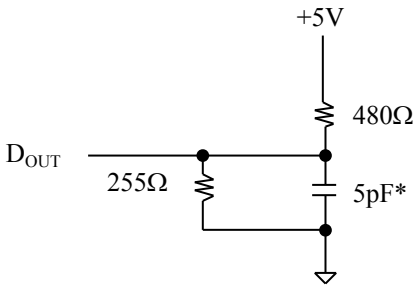
PARAMETER	VALUE
Input Pulse Level	0.V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Including scope and jig capacitance

READ CYCLE

PARAMETER	SYMBOL	-10		-12		-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	10	-	12	-	15	ns
Output Enable to Output	t_{OE}	-	5	-	6	-	7	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	5	0	6	0	7	ns
Chip Disable to High-Z Output	t_{HZ}	0	5	0	6	0	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Select to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Select to Power Down Time	t_{PD}	-	10	-	12	-	15	ns

WRITE CYCLE

PARAMETER	SYMBOL	-10		-12		-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	10	-	12	-	15	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	10	-	ns
Write Pulse Width (/OE=High)	t_{WP}	7	-	8	-	10	-	ns
Write Pulse Width(/OE=Low)	t_{WP1}	10	-	12	-	14	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WZ}	0	5	0	6	0	7	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

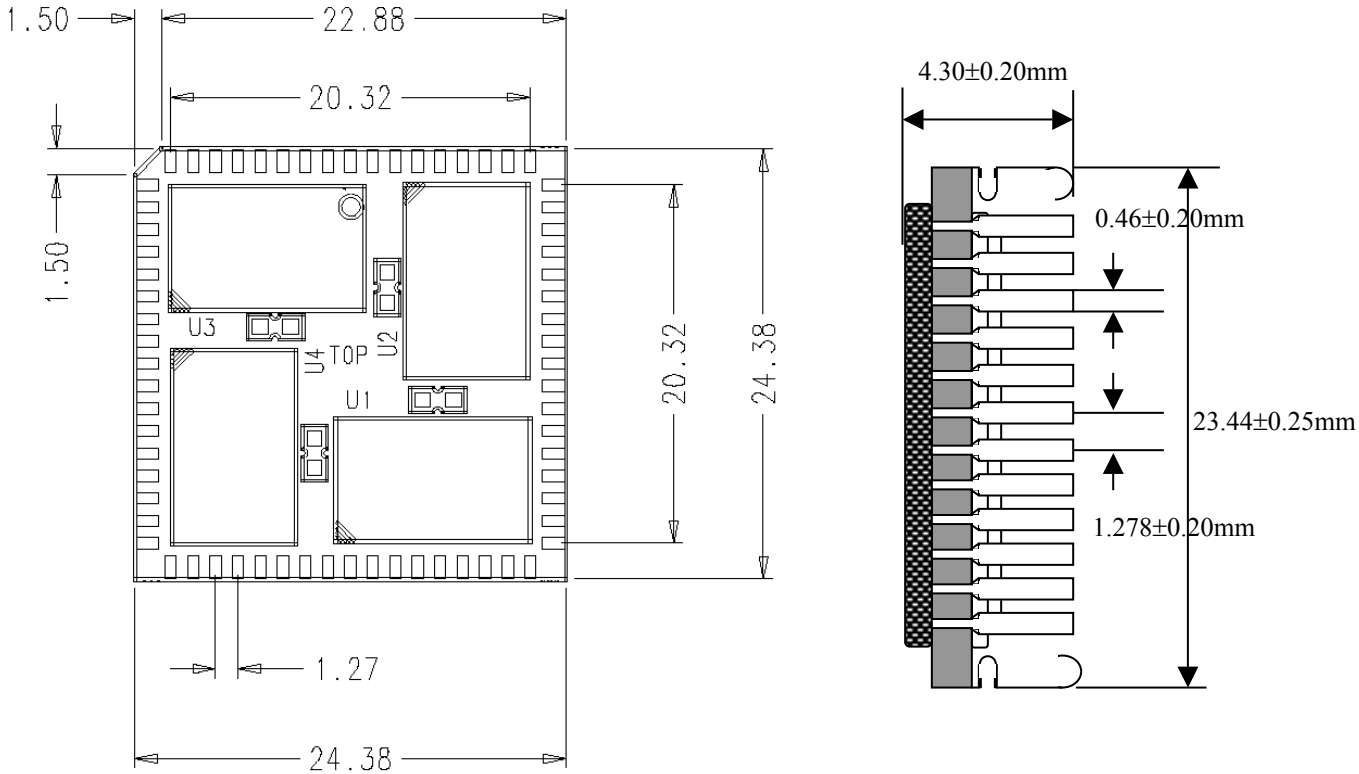
Please refer to timing diagram chart.

FUNCTIONAL DESCRIPTION

/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note: X means Don't Care

PACKAGE DIMENSIONS



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	Access time
HMS51232J4A-10	2MByte	512KX 32bit	68 Pin-JLCC	4EA	5V	10ns
HMS51232J4A-12	2MByte	512KX 32bit	68 Pin-JLCC	4EA	5V	12ns
HMS51232J4A-15	2MByte	512KX 32bit	68 Pin-JLCC	4EA	5V	15ns