H A N
B I T

High-Speed SRAM MODULE 4Mbyte(1M x 32-Bit)
Part No. HMS1M32M8S, HMS1M32Z8S

GENERAL DESCRIPTION

The HMS1M32M8S is a high-speed static random access memory (SRAM) module containing 1,048,576 words organized in a x32-bit configuration. The module consists of eight 512K x 8 SRAMs mounted on a 72-pin, double-sided, FR4-printed circuit board.

The HMS1M32M8S also support low data retention voltage for battery back-up operations with low data retention current. Eight chip enable inputs, (/CE_UU1, /CE_UM1, /CE_LM1, /CE_LL1, /CE_UU2, /CE_UM2, /CE_LM2, /CE_LL2) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW.

Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible

FEATURES

- Part identification
  - HMS1M32M8S : SIMM design
  - HMS1M32Z8S : ZIP design

Pin-Compatible with the HMS1M32M8S

- Access times : 10, 12, 15, 17 and 20ns
- High-density 4MByte design
- High-reliability, high-speed design
- Single + 5V ±0.5V power supply
- All inputs and outputs are TTL-compatible
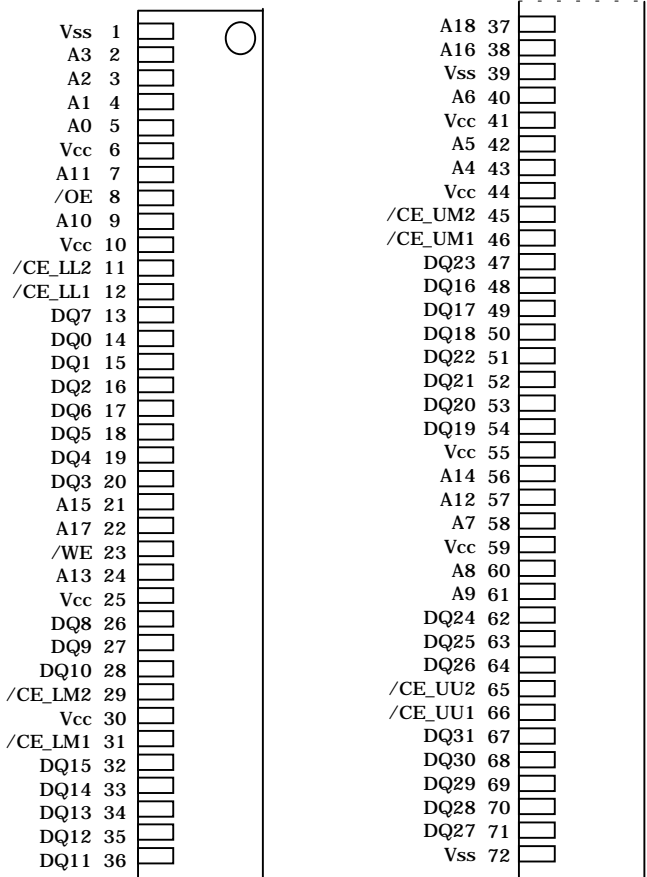- FR4-PCB design
- 72-Pin SIMM Design

OPTIONS   MARKING

- Timing

10ns access	-10
12ns access	-12
15ns access	-15
17ns access	-17
20ns access	-20

- Packages

72-pin SIMM	M

PIN ASSIGNMENT

Vss	1		A18	37
A3	2		A16	38
A2	3		Vss	39
A1	4		A6	40
A0	5		Vcc	41
Vcc	6		A5	42
A11	7		A4	43
/OE	8		Vcc	44
A10	9		/CE_UM2	45
Vcc	10		/CE_UM1	46
/CE_LL2	11		DQ23	47
/CE_LL1	12		DQ16	48
DQ7	13		DQ17	49
DQ0	14		DQ18	50
DQ1	15		DQ22	51
DQ2	16		DQ21	52
DQ6	17		DQ20	53
DQ5	18		DQ19	54
DQ4	19		Vcc	55
DQ3	20		A14	56
A15	21		A12	57
A17	22		A7	58
/WE	23		Vcc	59
A13	24		A8	60
Vcc	25		A9	61
DQ8	26		DQ24	62
DQ9	27		DQ25	63
DQ10	28		DQ26	64
/CE_LM2	29		/CE_UU2	65
Vcc	30		/CE_UU1	66
/CE_LM1	31		DQ31	67
DQ15	32		DQ30	68
DQ14	33		DQ29	69
DQ13	34		DQ28	70
DQ12	35		DQ27	71
DQ11	36		Vss	72

SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM
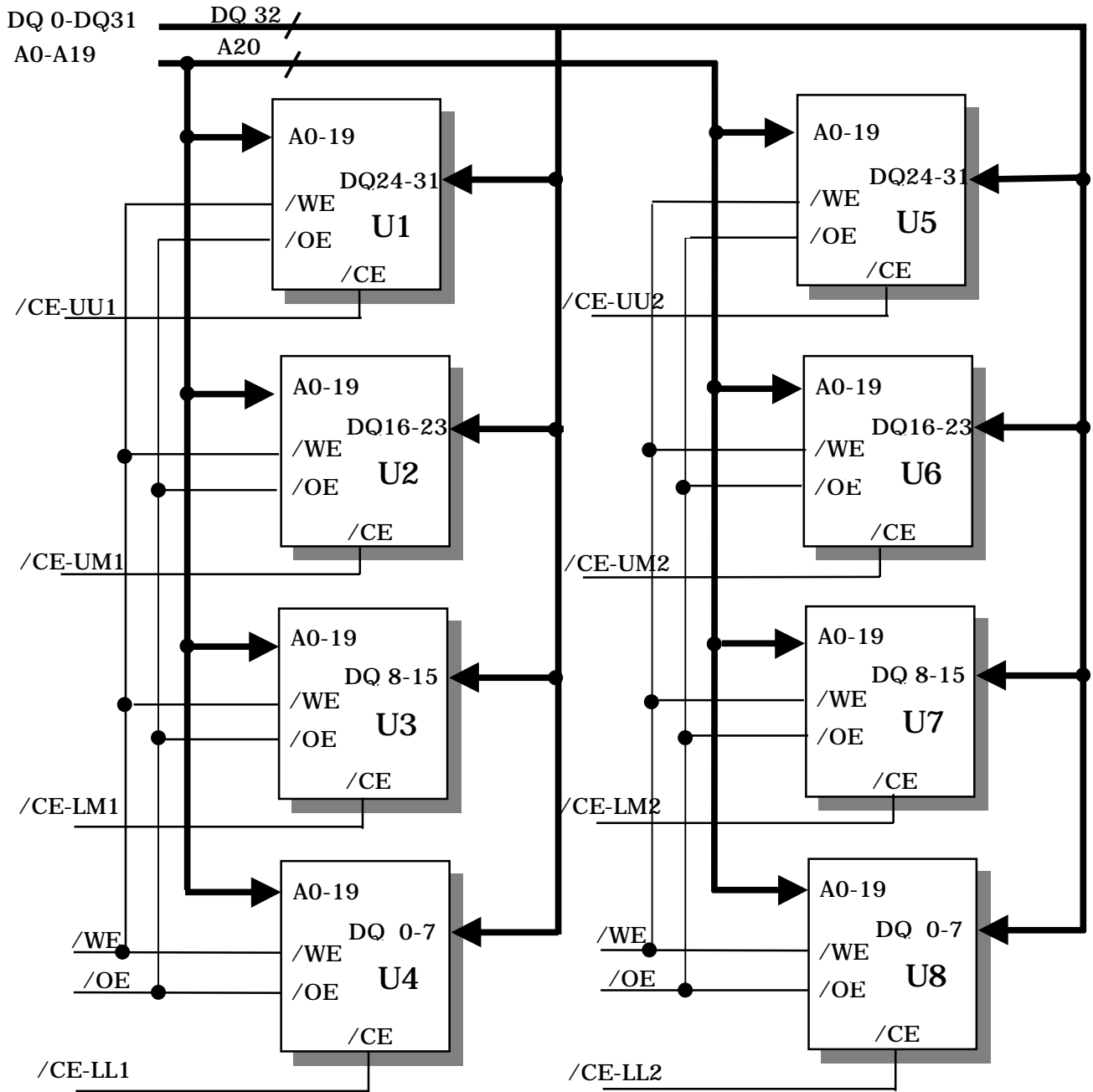
TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Q	ACTIVE
WRITE or ERASE	X	L	L	D	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to +7.0V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +7.0V
Power Dissipation	P_D	8W
Storage Temperature	T_{STG}	-55^oC to $+125^oC$
Operating Temperature	T_A	0^oC to $+70^oC$

♦ Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device.
  This is a stress rating only and functional operation of the device at these or any other conditions above those indicated
  in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended
  periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 ^{o} C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5V**
Input Low Voltage	V_{IL}	-0.5*	-	0.8V

* V_{IL}(Min.) = -2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

** V_{IH}(Max.) = Vcc+2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)

(0^oC ≤ T_A ≤ 70 ^{o}C ; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{IN} = Vss to Vcc	IL_I	-2	2	μA
Output Leakage Current	/CE=$V_{IH \, or \,}$/OE =V_{IH} or /WE=V_{IL} V_{OUT}=Vss to V_{CC}	IL_0	-2	2	μA
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4	-	V
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V

* Vcc=5.0V, Temp=25 ^oC

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX			UNIT
			-15	-17	-20	
Power Supply Current: Operating	Min. Cycle, 100% Duty /CE=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	I_{CC}	170	165	160	mA
Power Supply Current: Standby	Min. Cycle, /CE=V_{IH}	I_{SB}	50	50	50	mA
	f=0MHZ, /CE≥V_{CC}-0.2V, V_{IN}≥ V_{CC}-0.2V or V_{IN}≤0.2V	I_{SB1}	10	10	10	mA

CAPACITANCE

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	8	pF
Input Capacitance	V_{IN}=0V	C_{IN}	7	pF

* **NOTE** : Capacitance is sampled and not 100% tested

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70 °C ; Vcc = 5V ± 0.5V, unless otherwise specified)

TEST CONDITIONS

PARAMETER	VALUE
Input Pulse Level	0.V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output   Load

Output Load (B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}
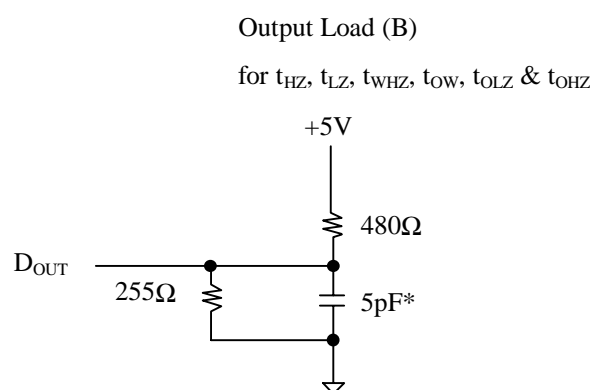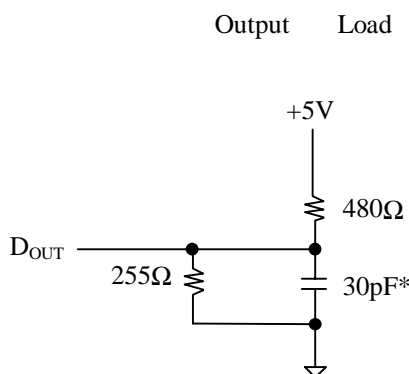
* Including scope and jig capacitance

READ CYCLE

PARAMETER	SYMBOL	-15		-17		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Output	t_{OE}	-	7	-	8	-	9	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	9	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Select to Power Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Select to Power Down Time	t_{PD}	-	15	-	17	-	20	ns

WRITE CYCLE

PARAMETER	SYMBOL	-15		-17		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	15	-	17	-	20	-	ns
Chip Select to End of Write	t_{CW}	12	-	13	-	14	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	12	-	13	-	14	-	ns
Write Pulse Width (/OE=High)	t_{WP}	12	-	13	-	14	-	ns
Write Recovery Time (/OE=Low)	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	8	-	9	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMING DIAGRAMS

## TIMING WAVEFORM OF READ CYCLE (Address Controlled) (/CE = /OE = V_{IL} , /WE = V_{IH})
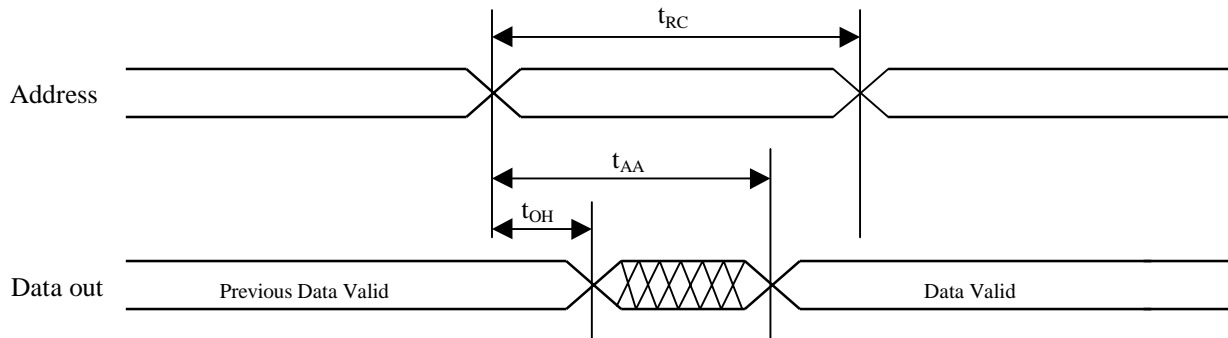

TIMING WAVEFORM OF READ CYCLE (/WE = V_{IH})
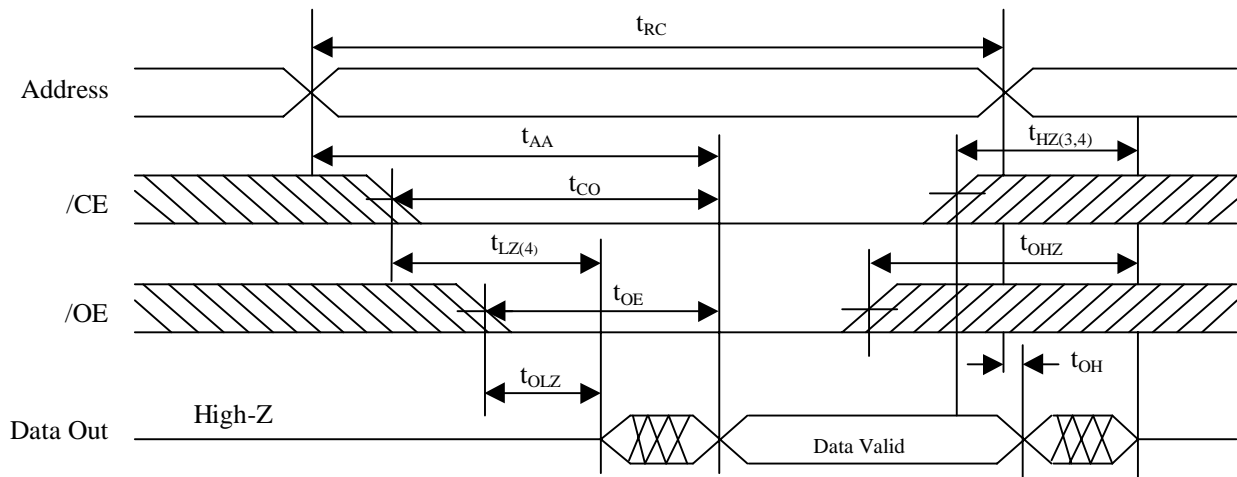
Notes (Read Cycle)

1. /WE is high for read cycle.

2. All read cycle timing is referenced from the last valid address to first transition address.

3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.

4. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)
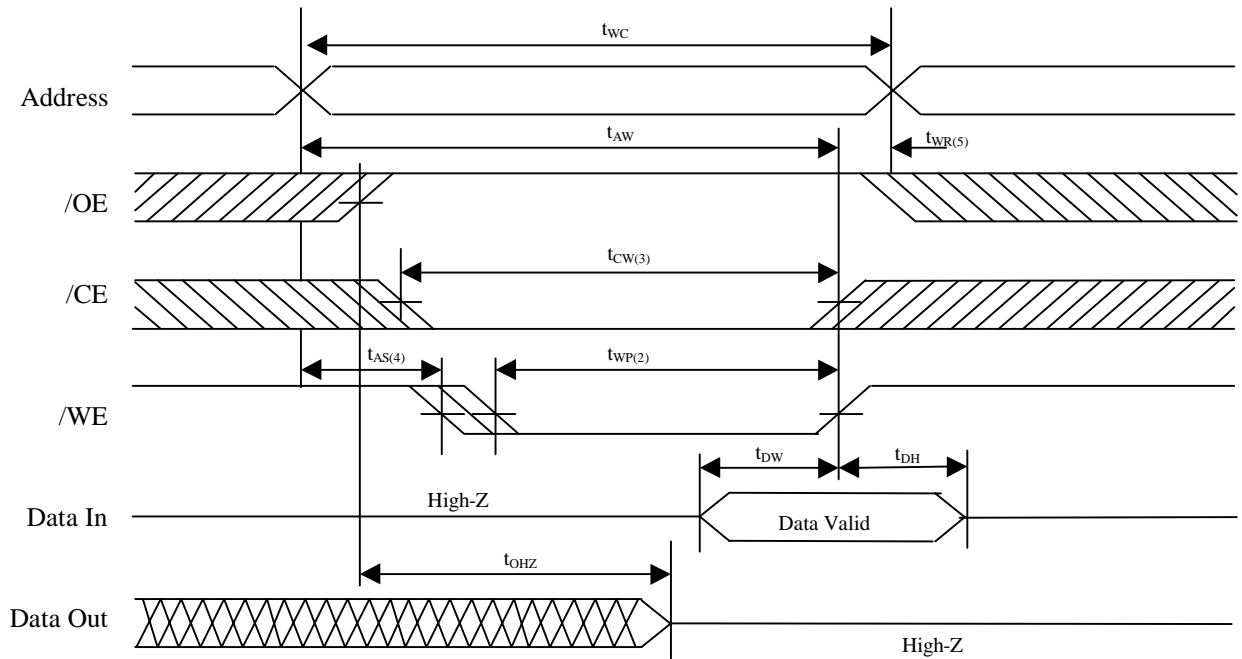
TIMING WAVEFORM OF WRITE CYCLE (/OE Low Fixed)
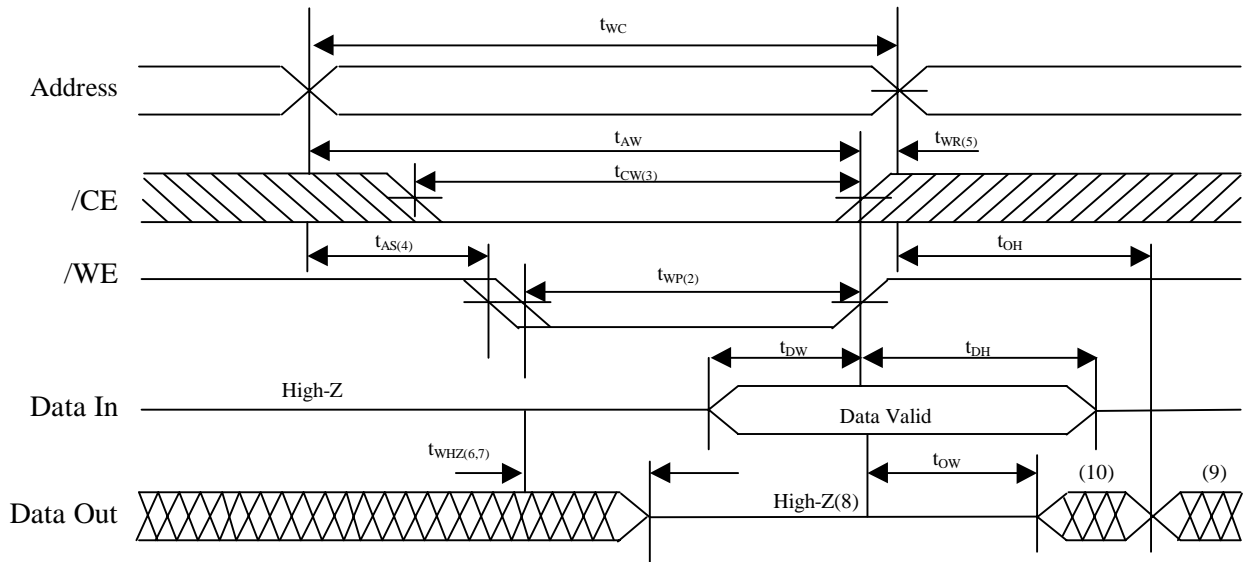
Notes(Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.

2. A write occurs during the overlap of a low /CE and a low /WE. A write begins at the latest transition among
   /CE going low and /WE going low: A write ends at the earliest transition among /CE going high and /WE going high.
   t_{WP} is measured from the beginning of write to the end of write.

3. t_{CW} is measured from the later of /CE going low to the end of write.

4. t_{AS} is measured from the address valid to the beginning of write.

5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CE, or /WE going high.

6. If /OE,/CE and /WE are in the read mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.

7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

8. If /CE goes low simultaneously with /WE going low or after /WE going low, the outputs remain high impedance state.

9. D_{OUT} is the read data of the new address.

10. When /CE is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
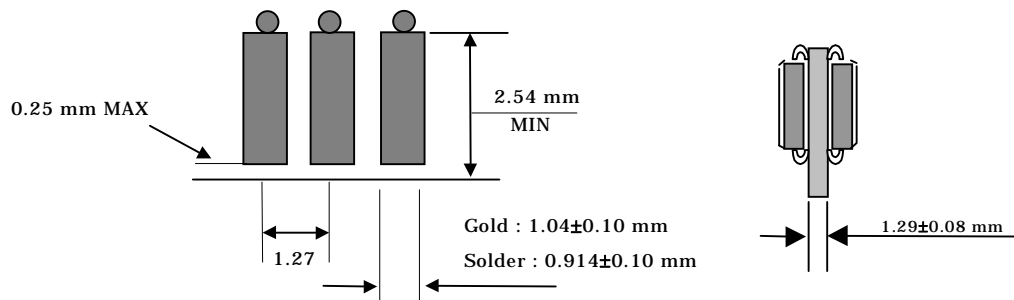
FUNCTIONAL DESCRIPTION

/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

Note: X means Don't Care

HANBit Electronics Co.,Ltd.

PACKAGING DIMMENSIONS

SIMM Design
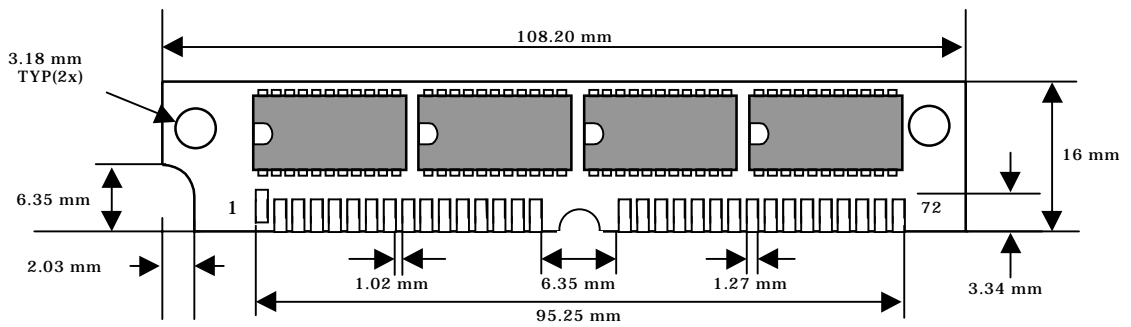
(Solder & Gold Plating Lead)

ORDERING INFORMATION

```
          1  2  3    4    5  6  7  8

          H  M  S   1M   32 M8S-15
                                    └── 15ns Access Time
   HANBit ──┘                  └──── Component, Customer
   Memory                   └─────── SIMM
   Modules ──┘           └────────── x32bit
   SRAM ────┘       └──────────────── 1M
```
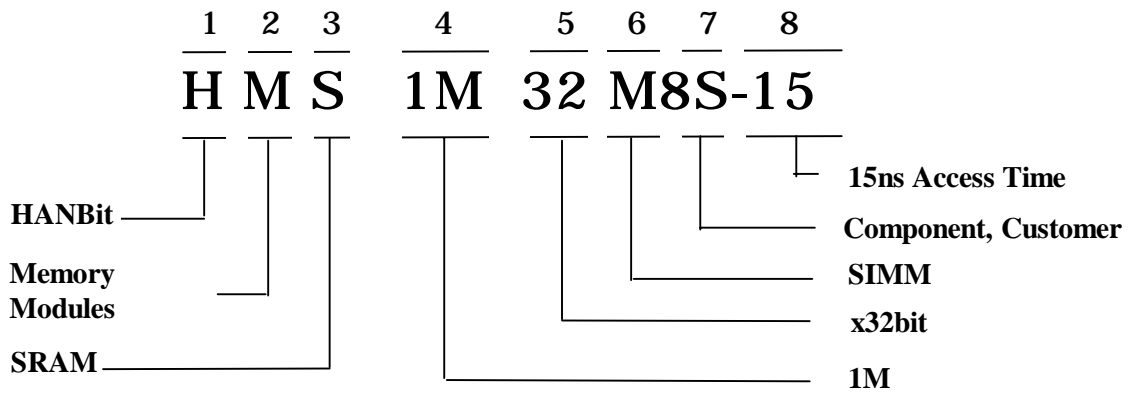
1. - **Product Line Identifier**
       HANBit Technology -------------------------------------- **H**
2. - **Memory Modules**
3. - **SRAM**
4. - **Depth : 1M**
5. - **Width : x 32bit**
6. - **Package Code**
       SIMM --- **M**
       ZIP   -- **Z**

7. - **Number of Memory Components---8, Customer-----S**
8. - **Access time**
       10 --- **10ns**
       12 --- **12ns**
       15 --- **15ns**
       17 --- **17ns**
       20 --- **20ns**