SRAM MODULE 4Mbyte(1Mx32Bit) ,LOW POWER,72Pin SIMM,5V
Part No. HMS1M32M8L, HMS1M32Z8L

GENERAL DESCRIPTION

The HMS1M32M8L is a static random access memory (SRAM) module containing 1,048,576 bits organized in a x32-bit configuration. The module consists of eight 512K x 8 SRAMs mounted on a 72-pin, double-sided, FR4-printed circuit board. The HMS1M32M8L also support low data retention voltage for battery back-up operations with low data retention current. Eight chip enable inputs, (/CE_UU1, /CE_UM1, /CE_LM1, /CE_LL1, /CE_UU2, /CE_UM2, /CE_LM2, /CE_LL2) are used to enable the module's 4M bytes independently. Output enable(/OE) and write enable(/WE) can set the memory input and output. Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW. Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

FEATURES

- Part identification
  - HMS1M32M8L : SIMM design
  - HMS1M32Z8L : ZIP design

  The both are Pin to Pin Compatible
- Access times : 55ns, 70ns
- High-density 4MByte design
- High-reliability, low-power design
- Single + 5V ±0.5V power supply
- Low data retention voltage : 2V(min)
- Three state output and TTL-compatible
- FR4-PCB design
- Low profile 72-Pin SIMM

OPTIONS MARKING

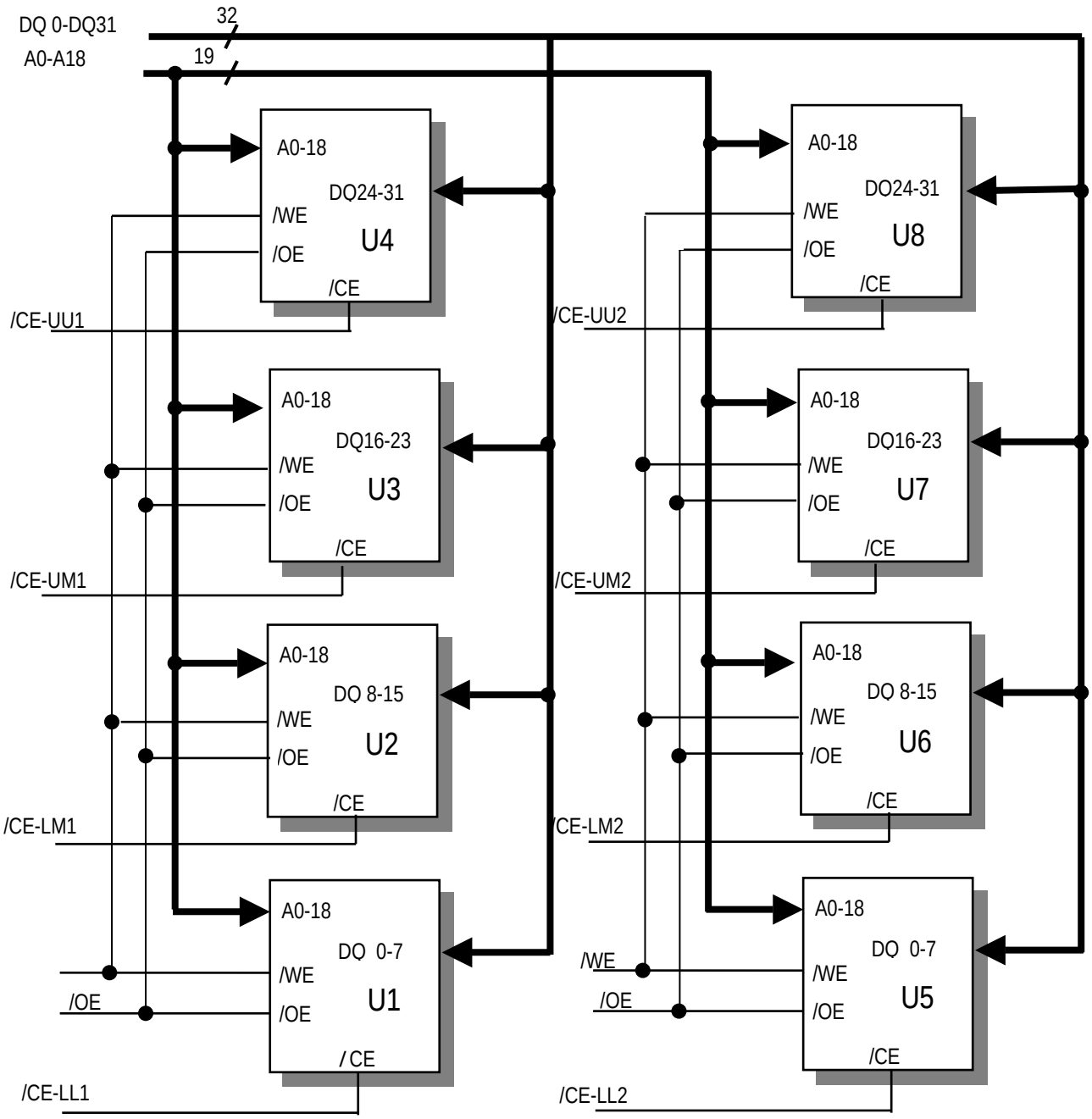
- Timing
  - 55ns access -55
  - 70ns access -70
- Packages
  - 72-pin SIMM M
  - 72-pin ZIP Z

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	Vcc	49	DQ17
2	A3	26	DQ8	50	DQ18
3	A2	27	DQ9	51	DQ22
4	A1	28	DQ10	52	DQ21
5	A0	29	/CE_LM2	53	DQ20
6	Vcc	30	Vcc	54	DQ19
7	A11	31	/CE_LM1	55	Vcc
8	/OE	32	DQ15	56	A14
9	A10	33	DQ14	57	A12
10	Vcc	34	DQ13	58	A7
11	/CE_LL2	35	DQ12	59	Vcc
12	/CE_LL1	36	DQ11	60	A8
13	DQ7	37	A18	61	A9
14	DQ0	38	A16	62	DQ24
15	DQ1	39	Vss	63	DQ25
16	DQ2	40	A6	64	DQ26
17	DQ6	41	Vcc	65	/CE_UU2
18	DQ5	42	A5	66	/CE_UU1
19	DQ4	43	A4	67	DQ31
20	DQ3	44	Vcc	68	DQ30
21	A15	45	/CE_UM2	69	DQ29
22	A17	46	/CE_UM1	70	DQ28
23	/WE	47	DQ23	71	DQ27
24	A13	48	DQ16	72	Vss

SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Q	ACTIVE
WRITE or ERASE	X	L	L	D	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to +7.0V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +7.0V
Power Dissipation	P_D	8W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	0°C to +70°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5V**
Input Low Voltage	V_{IL}	-0.5*	-	0.8V

* V_{IL}(Min.) = -2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

****** V_{IH}(Min.) = Vcc+2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)

(0°C ≤ T_A ≤ 70 °C ; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{IN} = Vss to Vcc	IL_I	-32	32	µA
Output Leakage Current	/CE=V_{IH} or /OE =V_{IH} or /WE=V_{IL} V_{OUT}=Vss to V_{CC}	IL_0	-32	32	µA
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V

* Vcc=5.0V, Temp=25 °C

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX		UNIT
			-55	-70	
Power Supply Current:Operating	I_{IO}=0mA,/CE=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read	I_{CC}	480	480	mA
Power Supply Current:Standby	/CE=V_{IH}, Other inputs=V_{IL} or V_{IH}	I_{SB}	96	96	mA
	/CE≥Vcc-0.2V, Other inputs=0~Vcc	I_{SB1}	400	400	μA

CAPACITANCE

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	248	pF
Input Capacitance	V_{IN}=0V	C_{IN}	320	pF

* NOTE : Capacitance is sampled and not 100% tested

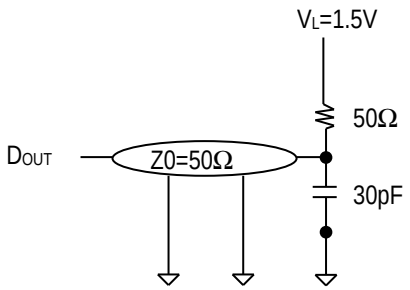
AC CHARACTERISTICS ($0^oC \le T_A \le 70\ ^oC$; Vcc = 5V ± 0.5V, unless otherwise specified)

Test conditions

PARAMETER	VALUE
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=100pF + 1TTL

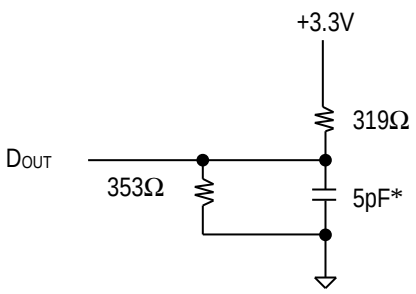
* See test condition of DC and Operating characteristics

Output Load (A)



Output Load (B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



READ CYCLE

PARAMETER	SYMBOL	-55		-70		UNIT
		MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	55		**70**		ns
Address Access Time	t_{AA}		55		70	ns
Chip Select to Output	t_{CO}		55		70	ns
Output Enable to Output	t_{OE}		25		35	ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	25	ns
Output Hold from Address Change	t_{OH}	10		10		ns

WRITE CYCLE

PARAMETER	SYMBOL	-55		-70		UNIT
		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	55		70		ns
Chip Select to End of Write	t_{CW}	45		60		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	45		60		ns
Write Pulse Width	t_{WP}	40		50		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	ns
Data to Write Time Overlap	t_{DW}	25		30		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		ns

TIMING DIAGRAMS

Please refer to timing diagram chart(II)

FUNCTIONAL DESCRIPTION

/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

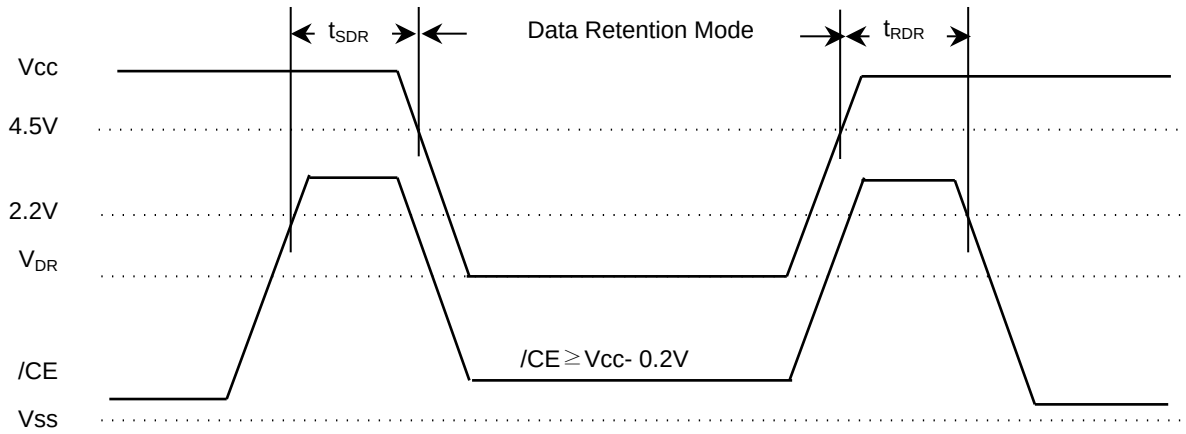
Note: X means Don't Care

DATA RETENTION CHARACTERISTICS* (TA = 0 to 70 ℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
V_{CC} for Data Retention	V_{DR}	/CE ≥ V_{CC}-0.2V	2	5.5	V
Data Retention Current	I_{DR}	V_{CC}=3.0V, /CE ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	-	400	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms(below)	0	-	ns
Recovery Time	t_{RDR}		5	-	ns

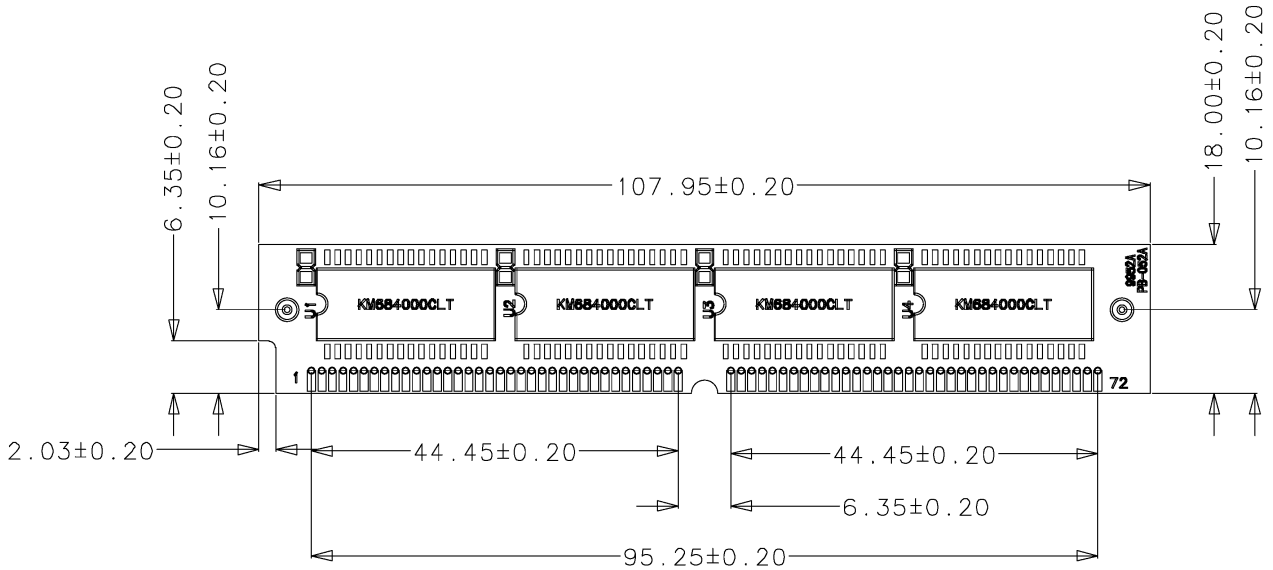
* L-Version Only

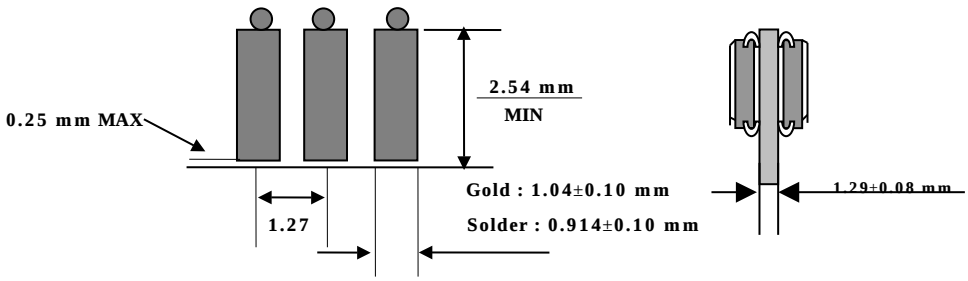
DATA RETENTION WAVEFORM 1 (/CE Controlled)



PACKAGING DIMENSIONS

SIMM Design





(Solder & Gold Plating Lead)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMS1M32M8L-55	4MByte	1M×32bit	72Pin-SIMM	8EA	5.0V	55ns
HMS1M32M8L-70	4MByte	1M×32bit	72Pin--SIMM	8EA	5.0V	70ns
HMS1M32Z8L-55	4MByte	1M×32bit	72Pin-ZIP	8EA	5.0V	55ns
HMS1M32Z8L-70	4MByte	1M×32bit	72Pin-ZIP	8EA	5.0V	70ns