EM65570S

68COM/98SEG 65K Color STN LCD Drivers

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

April 2006

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2005/12/06
0.2	1. Modified the pad drawing and pad sequence 2. Modified the Serial mode AC timing 3. Modified the DC electrical characteristics 4. Modified the pin dimensions table	2006/01/04
0.3	1. Corrected the error in the Control Register Table 2. Modified the OTP programming time 3. Modified the AC timing	2006/04/15
1.0	Removed the Preliminary mark on the background of every page.	2006/4/18

1 General Description

EM65570S is one of the industry's most advanced wide-screen STN-LCD drivers for 65K-color display. It also has a built-in display RAM, a power supply circuit for LCD drive, an LCD controller circuit, support for LCD cell tolerance compensation of VLCD and temperature compensation. It also supports OTP function for programming information to tune VLCD offset voltage to get the best contrast, hence enhancing the compact system design. Its partial display function"[1] contributes to the reduction of power consumption.

2 Feature

- 65K-color display
- LCD outputs: Segment 98RGB (294 outputs); Common 68 outputs
- Display RAM capacity: 98x68x16=106624 bits
- Built-in display RAM and power supply circuit
- Partial display functions
- Bus connection with 80-family/68-family MPU/ELAN MPU
- Logic power supply voltage: 2.2 to 3.3 V
- Analog power supply voltage: 2.4 to 3.3 V
- LCD driving voltage: 4.5 to 16 V
- Booster: 2 to 5 times
- Fast burst-RAM write function
- Screen scroll function
- Graphic function
- OTP function for tuning LCD operating voltage Vop
- System Write cycle: 200 ns
- Package:

Part Number	Package	Description	Package Information
EM65570SAGH	Gold bumped chip	NA	NA

Note: The EM65570S series has the following sub-codes, depending on their shapes.
H: Bare chip (Aluminum pad without bump); **GH**: Gold bumped chip
F: COF package; **T**: TAB (TCP) package

Example:

EM65570SAGH → EM65570S: Elan number; **A:** Package Version; **GH:** Gold bumped chip

[1] A function that allows the device to utilize only part of the screen, thus reducing power consumption.

3 Applications

- Mobile phone
- DECT phone
- Cordless phone
- Toy & Game display

4 Pin Configuration

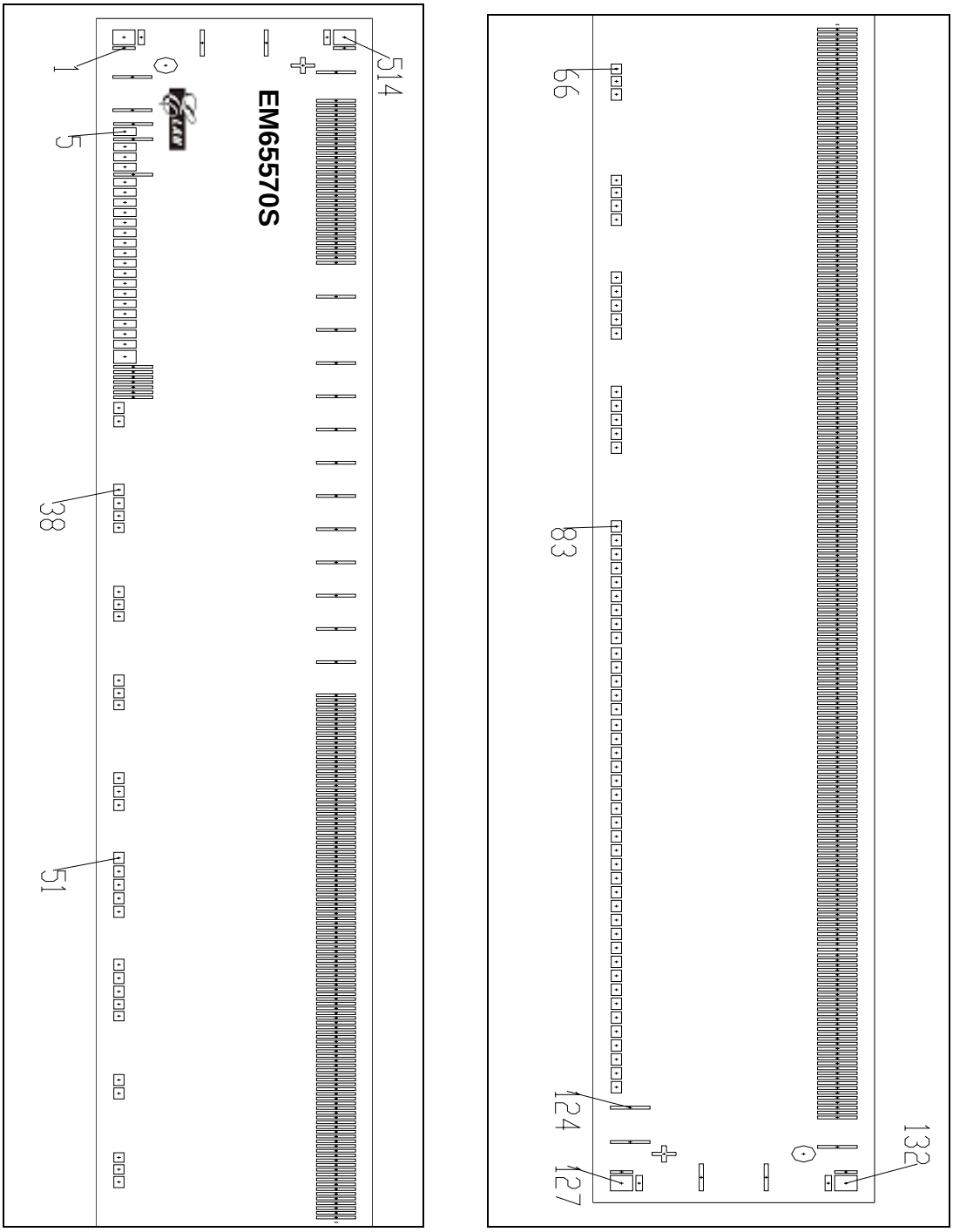


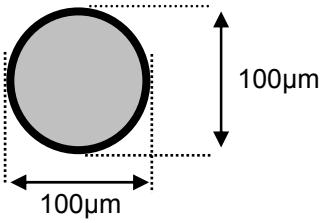
Figure 1 Pin Configuration

NOTE

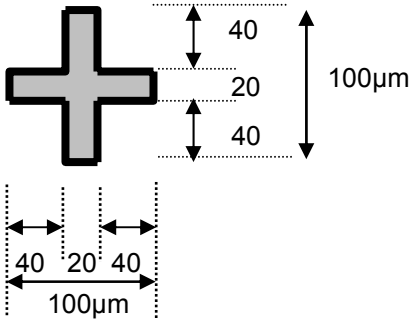
With the Elan logo at the left corner (as shown in the figure), Pin 1 is at the bottom left corner.

Mark	Coordinate (X, Y)	Mark	Coordinate (X, Y)
U-Left	-7043, 290.27	U-Right	7042.5, 290.27
D-Left	-7043, -289.58	D-Right	7042.5, -289.58

D-Left and U-Right:



U-Left and D-Right:



Pin Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	-	14680	1170	μm
Bump Size	1 , 126 , 133 , 513	17	94	
	2 ~ 4 , 6 , 10 , 29 ~ 35 , 124 ~ 125 , 134 ~ 512	17	165	
	5 , 7 ~ 9 , 11 ~ 27	49	94	
	28	81	94	
	36 ~ 39 , 42 , 45 , 48 ~ 58 , 61 ~ 62 , 65 , 68 , 71 ~ 123	70	43	
	40 ~ 41 , 43 ~ 44 , 46 ~ 47 , 59 ~ 60 , 63 ~ 64 , 66 ~ 67 , 69 ~ 70	60	43	
	129 , 130 , 516 , 517	165	17	
	127 , 132 , 514 , 519	93	94	
	128 , 131 , 515 , 518	93	27	
Pad Pitch	7 ~ 9 , 11 ~ 27	64		
	29 ~ 35	32		
	36 ~ 37 , 38 ~ 39 , 48 ~ 50 , 51 ~ 55 , 56 ~ 58 , 61 ~ 62 , 71 ~ 72 , 73 ~ 77 , 78 ~ 82 , 83 ~ 91 , 92 ~ 96 , 97 ~ 123	85		
	40 ~ 41 , 43 ~ 44 , 46 ~ 47 , 59 ~ 60 , 63 ~ 64 , 66 ~ 67 , 69 ~ 70	75		
	135 ~ 168 , 170 ~ 361 , 363 ~ 464 , 478 ~ 511	30		
	465 ~ 476	210		
	Minimum pitch	30		
Die thickness (excluding bumps)	20 ± 1 mil (500 ± 25 μm)			
Bump Height	17 ± 3 μm			
Bump coplanar within die	≤ 2μm			
Minimum Bump Gap	13 μm			
Coordinate Origin	Chip center			

Recommended COG ITO Traces Resistor

Interface	ITO Traces Resistances
V0~V4 CAP1+,CAP1-,CAP2+,CAP2-,CAP3+, CAP3-, CAP4+, V2x, Vout VDD1~VDD3,VEE VSS1~VSS5	Max=50Ω
WRB, RDB, CSB,…, D0~D7	Max=3KΩ
RESB	Max=5~10KΩ

Pin No	Pad Name	Coordinate		Pin No	Pad Name	Coordinate	
		X	Y			X	Y
1	NC1	-7153.28	-466	51	CAP3-	-2032.37	-487.5
2	NC2	-6970.2	-430.645	52	CAP3-	-1947.37	-487.5
3	NC3	-6760.2	-430.645	53	CAP3-	-1862.37	-487.5
4	NC4	-6673	-427.145	54	CAP2-	-1777.37	-487.5
5	CSB	-6625	-462.35	55	CAP2-	-1692.37	-487.5
6	RESB	-6577	-427.145	56	CAP2-	-1357.78	-487.5
7	RS	-6529	-462.35	57	CAP2-	-1272.78	-487.5
8	CK	-6465	-462.35	58	CAP2-	-1187.78	-487.5
9	WRB	-6401	-462.35	59	CAP2+	-1107.78	-487.5
10	VSS2	-6353	-427.145	60	CAP2+	-1032.78	-487.5
11	RDB	-6305	-462.35	61	CAP2+	-629.01	-487.5
12	D0	-6241	-462.35	62	CAP4+	-544.01	-487.5
13	D1	-6177	-462.35	63	CAP4+	-138.48	-487.5
14	D2	-6113	-462.35	64	CAP4+	-63.48	-487.5
15	D3	-6049	-462.35	65	NC11	16.52	-487.5
16	D4	-5985	-462.35	66	NC12	422.05	-487.5
17	D5	-5921	-462.35	67	NC13	497.05	-487.5
18	D6	-5857	-462.35	68	CAP1+	577.05	-487.5
19	D7	-5793	-462.35	69	CAP1+	1101.5	-487.5
20	D8	-5729	-462.35	70	CAP1+	1176.5	-487.5
21	D9	-5665	-462.35	71	CAP1-	1256.5	-487.5
22	D10	-5601	-462.35	72	CAP1-	1341.5	-487.5
23	D11	-5537	-462.35	73	CAP1-	1695.05	-487.5
24	D12	-5473	-462.35	74	CAP1-	1780.05	-487.5
25	D13	-5409	-462.35	75	CAP1-	1865.05	-487.5
26	D14	-5345	-462.35	76	V2X	1950.05	-487.5
27	D15	-5281	-462.35	77	V2X	2035.05	-487.5
28	VDD1	-5201	-462.35	78	V2X	2392.78	-487.5
29	PS	-5137	-427.145	79	V2X	2477.78	-487.5
30	CSL	-5105	-427.145	80	V2X	2562.78	-487.5
31	M86	-5073	-427.145	81	VEE	2647.78	-487.5
32	CKS	-5041	-427.145	82	VEE	2732.78	-487.5
33	TEST	-5009	-427.145	83	VEE	3213.75	-487.5
34	VSS2	-4977	-427.145	84	VEE	3298.75	-487.5
35	DUMMY	-4945	-427.145	85	VDD2	3383.75	-487.5
36	VOUT	-4878.25	-487.5	86	VDD3	3468.75	-487.5
37	VOUT	-4793.25	-487.5	87	VSS1	3553.75	-487.5
38	VOUT	-4360.61	-487.5	88	VSS1	3638.75	-487.5
39	VOUT	-4275.61	-487.5	89	VSS1	3723.75	-487.5
40	NC5	-4195.61	-487.5	90	VSS1	3808.75	-487.5
41	NC6	-4120.61	-487.5	91	VSS1	3893.75	-487.5
42	NC7	-3715.08	-487.5	92	VSS2	3989.45	-487.5
43	NC8	-3635.08	-487.5	93	VSS2	4074.45	-487.5
44	NC9	-3560.08	-487.5	94	VSS3	4159.45	-487.5
45	NC10	-3154.8	-487.5	95	VSS3	4244.45	-487.5
46	CAP3+	-3074.8	-487.5	96	VSS4	4329.45	-487.5
47	CAP3+	-2999.8	-487.5	97	VSS5	4425.45	-487.5
48	CAP3+	-2536.96	-487.5	98	VSS5	4510.45	-487.5
49	CAP3-	-2451.96	-487.5	99	VSS5	4595.45	-487.5
50	CAP3-	-2366.96	-487.5	100	VSS5	4680.45	-487.5

Pin No	Pad Name	Coordinate		Pin No	Pad Name	Coordinate	
		X	Y			X	Y
101	V0	4765.45	-487.5	151	COM34	6340.2	430.645
102	V0	4850.45	-487.5	152	COM32	6310.2	430.645
103	V0	4935.45	-487.5	153	COM30	6280.2	430.645
104	V0	5020.45	-487.5	154	COM28	6250.2	430.645
105	V0	5105.45	-487.5	155	COM26	6220.2	430.645
106	V0	5190.45	-487.5	156	COM24	6190.2	430.645
107	V0	5275.45	-487.5	157	COM22	6160.2	430.645
108	V1	5360.45	-487.5	158	COM20	6130.2	430.645
109	V1	5445.45	-487.5	159	COM18	6100.2	430.645
110	V1	5530.45	-487.5	160	COM16	6070.2	430.645
111	V1	5615.45	-487.5	161	COM14	6040.2	430.645
112	V1	5700.45	-487.5	162	COM12	6010.2	430.645
113	V1	5785.45	-487.5	163	COM10	5980.2	430.645
114	V2	5870.45	-487.5	164	COM8	5950.2	430.645
115	V2	5955.45	-487.5	165	COM6	5920.2	430.645
116	V2	6040.45	-487.5	166	COM4	5890.2	430.645
117	V3	6125.45	-487.5	167	COM2	5860.2	430.645
118	V3	6210.45	-487.5	168	COM0	5830.2	430.645
119	V3	6295.45	-487.5	169	NC25	5795.7	430.645
120	V4	6380.45	-487.5	170	SEGA0	5761.2	430.645
121	V4	6465.45	-487.5	171	SEGB0	5731.2	430.645
122	V4	6550.45	-487.5	172	SEGC0	5701.2	430.645
123	V4	6635.45	-487.5	173	SEGA1	5671.2	430.645
124	NC14	6760.2	-430.645	174	SEGB1	5641.2	430.645
125	NC15	6970.2	-430.645	175	SEGC1	5611.2	430.645
126	NC16	7153.28	-466	176	SEGA2	5581.2	430.645
127	NC17	7221.39	-466.25	177	SEGB2	5551.2	430.645
128	NC18	7221.39	-392.98	178	SEGC2	5521.2	430.645
129	NC19	7185.645	-135	179	SEGA3	5491.2	430.645
130	NC20	7185.645	135	180	SEGB3	5461.2	430.645
131	NC21	7221.39	392.98	181	SEGC3	5431.2	430.645
132	NC22	7221.39	466.25	182	SEGA4	5401.2	430.645
133	NC23	7153.28	466	183	SEGB4	5371.2	430.645
134	NC24	7000.2	430.645	184	SEGC4	5341.2	430.645
135	COM66	6820.2	430.645	185	SEGA5	5311.2	430.645
136	COM64	6790.2	430.645	186	SEGB5	5281.2	430.645
137	COM62	6760.2	430.645	187	SEGC5	5251.2	430.645
138	COM60	6730.2	430.645	188	SEGA6	5221.2	430.645
139	COM58	6700.2	430.645	189	SEGB6	5191.2	430.645
140	COM56	6670.2	430.645	190	SEGC6	5161.2	430.645
141	COM54	6640.2	430.645	191	SEGA7	5131.2	430.645
142	COM52	6610.2	430.645	192	SEGB7	5101.2	430.645
143	COM50	6580.2	430.645	193	SEGC7	5071.2	430.645
144	COM48	6550.2	430.645	194	SEGA8	5041.2	430.645
145	COM46	6520.2	430.645	195	SEGB8	5011.2	430.645
146	COM44	6490.2	430.645	196	SEGC8	4981.2	430.645
147	COM42	6460.2	430.645	197	SEGA9	4951.2	430.645
148	COM40	6430.2	430.645	198	SEGB9	4921.2	430.645
149	COM38	6400.2	430.645	199	SEGC9	4891.2	430.645
150	COM36	6370.2	430.645	200	SEGA10	4861.2	430.645

Pin No	Pad Name	Coordinate		PIN NO	Pad Name	Coordinate	
		X	Y			X	Y
201	SEGB10	4831.2	430.645	251	SEGA27	3331.2	430.645
202	SEGC10	4801.2	430.645	252	SEGB27	3301.2	430.645
203	SEGA11	4771.2	430.645	253	SEGC27	3271.2	430.645
204	SEGB11	4741.2	430.645	254	SEGA28	3241.2	430.645
205	SEGC11	4711.2	430.645	255	SEGB28	3211.2	430.645
206	SEGA12	4681.2	430.645	256	SEGC28	3181.2	430.645
207	SEGB12	4651.2	430.645	257	SEGA29	3151.2	430.645
208	SEGC12	4621.2	430.645	258	SEGB29	3121.2	430.645
209	SEGA13	4591.2	430.645	259	SEGC29	3091.2	430.645
210	SEGB13	4561.2	430.645	260	SEGA30	3061.2	430.645
211	SEGC13	4531.2	430.645	261	SEGB30	3031.2	430.645
212	SEGA14	4501.2	430.645	262	SEGC30	3001.2	430.645
213	SEGB14	4471.2	430.645	263	SEGA31	2971.2	430.645
214	SEGC14	4441.2	430.645	264	SEGB31	2941.2	430.645
215	SEGA15	4411.2	430.645	265	SEGC31	2911.2	430.645
216	SEGB15	4381.2	430.645	266	SEGA32	2881.2	430.645
217	SEGC15	4351.2	430.645	267	SEGB32	2851.2	430.645
218	SEGA16	4321.2	430.645	268	SEGC32	2821.2	430.645
219	SEGB16	4291.2	430.645	269	SEGA33	2791.2	430.645
220	SEGC16	4261.2	430.645	270	SEGB33	2761.2	430.645
221	SEGA17	4231.2	430.645	271	SEGC33	2731.2	430.645
222	SEGB17	4201.2	430.645	272	SEGA34	2701.2	430.645
223	SEGC17	4171.2	430.645	273	SEGB34	2671.2	430.645
224	SEGA18	4141.2	430.645	274	SEGC34	2641.2	430.645
225	SEGB18	4111.2	430.645	275	SEGA35	2611.2	430.645
226	SEGC18	4081.2	430.645	276	SEGB35	2581.2	430.645
227	SEGA19	4051.2	430.645	277	SEGC35	2551.2	430.645
228	SEGB19	4021.2	430.645	278	SEGA36	2521.2	430.645
229	SEGC19	3991.2	430.645	279	SEGB36	2491.2	430.645
230	SEGA20	3961.2	430.645	280	SEGC36	2461.2	430.645
231	SEGB20	3931.2	430.645	281	SEGA37	2431.2	430.645
232	SEGC20	3901.2	430.645	282	SEGB37	2401.2	430.645
233	SEGA21	3871.2	430.645	283	SEGC37	2371.2	430.645
234	SEGB21	3841.2	430.645	284	SEGA38	2341.2	430.645
235	SEGC21	3811.2	430.645	285	SEGB38	2311.2	430.645
236	SEGA22	3781.2	430.645	286	SEGC38	2281.2	430.645
237	SEGB22	3751.2	430.645	287	SEGA39	2251.2	430.645
238	SEGC22	3721.2	430.645	288	SEGB39	2221.2	430.645
239	SEGA23	3691.2	430.645	289	SEGC39	2191.2	430.645
240	SEGB23	3661.2	430.645	290	SEGA40	2161.2	430.645
241	SEGC23	3631.2	430.645	291	SEGB40	2131.2	430.645
242	SEGA24	3601.2	430.645	292	SEGC40	2101.2	430.645
243	SEGB24	3571.2	430.645	293	SEGA41	2071.2	430.645
244	SEGC24	3541.2	430.645	294	SEGB41	2041.2	430.645
245	SEGA25	3511.2	430.645	295	SEGC41	2011.2	430.645
246	SEGB25	3481.2	430.645	296	SEGA42	1981.2	430.645
247	SEGC25	3451.2	430.645	297	SEGB42	1951.2	430.645
248	SEGA26	3421.2	430.645	298	SEGC42	1921.2	430.645
249	SEGB26	3391.2	430.645	299	SEGA43	1891.2	430.645
250	SEGC26	3361.2	430.645	300	SEGB43	1861.2	430.645

Pin No	Pad Name	Coordinate		Pin No	Pad Name	Coordinate	
		X	Y			X	Y
301	SEGC43	1831.2	430.645	351	SEGB60	331.2	430.645
302	SEGA44	1801.2	430.645	352	SEGC60	301.2	430.645
303	SEGB44	1771.2	430.645	353	SEGA61	271.2	430.645
304	SEGC44	1741.2	430.645	354	SEGB61	241.2	430.645
305	SEGA45	1711.2	430.645	355	SEGC61	211.2	430.645
306	SEGB45	1681.2	430.645	356	SEGA62	181.2	430.645
307	SEGC45	1651.2	430.645	357	SEGB62	151.2	430.645
308	SEGA46	1621.2	430.645	358	SEGC62	121.2	430.645
309	SEGB46	1591.2	430.645	359	SEGA63	91.2	430.645
310	SEGC46	1561.2	430.645	360	SEGB63	61.2	430.645
311	SEGA47	1531.2	430.645	361	SEGC63	31.2	430.645
312	SEGB47	1501.2	430.645	362	NC26	0	430.645
313	SEGC47	1471.2	430.645	363	SEGA64	-31.2	430.645
314	SEGA48	1441.2	430.645	364	SEGB64	-61.2	430.645
315	SEGB48	1411.2	430.645	365	SEGC64	-91.2	430.645
316	SEGC48	1381.2	430.645	366	SEGA65	-121.2	430.645
317	SEGA49	1351.2	430.645	367	SEGB65	-151.2	430.645
318	SEGB49	1321.2	430.645	368	SEGC65	-181.2	430.645
319	SEGC49	1291.2	430.645	369	SEGA66	-211.2	430.645
320	SEGA50	1261.2	430.645	370	SEGB66	-241.2	430.645
321	SEGB50	1231.2	430.645	371	SEGC66	-271.2	430.645
322	SEGC50	1201.2	430.645	372	SEGA67	-301.2	430.645
323	SEGA51	1171.2	430.645	373	SEGB67	-331.2	430.645
324	SEGB51	1141.2	430.645	374	SEGC67	-361.2	430.645
325	SEGC51	1111.2	430.645	375	SEGA68	-391.2	430.645
326	SEGA52	1081.2	430.645	376	SEGB68	-421.2	430.645
327	SEGB52	1051.2	430.645	377	SEGC68	-451.2	430.645
328	SEGC52	1021.2	430.645	378	SEGA69	-481.2	430.645
329	SEGA53	991.2	430.645	379	SEGB69	-511.2	430.645
330	SEGB53	961.2	430.645	380	SEGC69	-541.2	430.645
331	SEGC53	931.2	430.645	381	SEGA70	-571.2	430.645
332	SEGA54	901.2	430.645	382	SEGB70	-601.2	430.645
333	SEGB54	871.2	430.645	383	SEGC70	-631.2	430.645
334	SEGC54	841.2	430.645	384	SEGA71	-661.2	430.645
335	SEGA55	811.2	430.645	385	SEGB71	-691.2	430.645
336	SEGB55	781.2	430.645	386	SEGC71	-721.2	430.645
337	SEGC55	751.2	430.645	387	SEGA72	-751.2	430.645
338	SEGA56	721.2	430.645	388	SEGB72	-781.2	430.645
339	SEGB56	691.2	430.645	389	SEGC72	-811.2	430.645
340	SEGC56	661.2	430.645	390	SEGA73	-841.2	430.645
341	SEGA57	631.2	430.645	391	SEGB73	-871.2	430.645
342	SEGB57	601.2	430.645	392	SEGC73	-901.2	430.645
343	SEGC57	571.2	430.645	393	SEGA74	-931.2	430.645
344	SEGA58	541.2	430.645	394	SEGB74	-961.2	430.645
345	SEGB58	511.2	430.645	395	SEGC74	-991.2	430.645
346	SEGC58	481.2	430.645	396	SEGA75	-1021.2	430.645
347	SEGA59	451.2	430.645	397	SEGB75	-1051.2	430.645
348	SEGB59	421.2	430.645	398	SEGC75	-1081.2	430.645
349	SEGC59	391.2	430.645	399	SEGA76	-1111.2	430.645
350	SEGA60	361.2	430.645	400	SEGB76	-1141.2	430.645

Pin No	Pad Name	Coordinate		Pin No	Pad Name	Coordinate	
		X	Y			X	Y
401	SEGC76	-1171.2	430.645	451	SEGB93	-2671.2	430.645
402	SEGA77	-1201.2	430.645	452	SEGC93	-2701.2	430.645
403	SEGB77	-1231.2	430.645	453	SEGA94	-2731.2	430.645
404	SEGC77	-1261.2	430.645	454	SEGB94	-2761.2	430.645
405	SEGA78	-1291.2	430.645	455	SEGC94	-2791.2	430.645
406	SEGB78	-1321.2	430.645	456	SEGA95	-2821.2	430.645
407	SEGC78	-1351.2	430.645	457	SEGB95	-2851.2	430.645
408	SEGA79	-1381.2	430.645	458	SEGC95	-2881.2	430.645
409	SEGB79	-1411.2	430.645	459	SEGA96	-2911.2	430.645
410	SEGC79	-1441.2	430.645	460	SEGB96	-2941.2	430.645
411	SEGA80	-1471.2	430.645	461	SEGC96	-2971.2	430.645
412	SEGB80	-1501.2	430.645	462	SEGA97	-3001.2	430.645
413	SEGC80	-1531.2	430.645	463	SEGB97	-3031.2	430.645
414	SEGA81	-1561.2	430.645	464	SEGC97	-3061.2	430.645
415	SEGB81	-1591.2	430.645	465	NC27	-3271.2	430.645
416	SEGC81	-1621.2	430.645	466	NC28	-3481.2	430.645
417	SEGA82	-1651.2	430.645	467	NC29	-3691.2	430.645
418	SEGB82	-1681.2	430.645	468	NC30	-3901.2	430.645
419	SEGC82	-1711.2	430.645	469	NC31	-4111.2	430.645
420	SEGA83	-1741.2	430.645	470	NC32	-4321.2	430.645
421	SEGB83	-1771.2	430.645	471	NC33	-4531.2	430.645
422	SEGC83	-1801.2	430.645	472	NC34	-4741.2	430.645
423	SEGA84	-1831.2	430.645	473	NC35	-4951.2	430.645
424	SEGB84	-1861.2	430.645	474	NC36	-5161.2	430.645
425	SEGC84	-1891.2	430.645	475	NC37	-5371.2	430.645
426	SEGA85	-1921.2	430.645	476	NC38	-5581.2	430.645
427	SEGB85	-1951.2	430.645	477	NC39	-5795.7	430.645
428	SEGC85	-1981.2	430.645	478	COM1	-5830.2	430.645
429	SEGA86	-2011.2	430.645	479	COM3	-5860.2	430.645
430	SEGB86	-2041.2	430.645	480	COM5	-5890.2	430.645
431	SEGC86	-2071.2	430.645	481	COM7	-5920.2	430.645
432	SEGA87	-2101.2	430.645	482	COM9	-5950.2	430.645
433	SEGB87	-2131.2	430.645	483	COM11	-5980.2	430.645
434	SEGC87	-2161.2	430.645	484	COM13	-6010.2	430.645
435	SEGA88	-2191.2	430.645	485	COM15	-6040.2	430.645
436	SEGB88	-2221.2	430.645	486	COM17	-6070.2	430.645
437	SEGC88	-2251.2	430.645	487	COM19	-6100.2	430.645
438	SEGA89	-2281.2	430.645	488	COM21	-6130.2	430.645
439	SEGB89	-2311.2	430.645	489	COM23	-6160.2	430.645
440	SEGC89	-2341.2	430.645	490	COM25	-6190.2	430.645
441	SEGA90	-2371.2	430.645	491	COM27	-6220.2	430.645
442	SEGB90	-2401.2	430.645	492	COM29	-6250.2	430.645
443	SEGC90	-2431.2	430.645	493	COM31	-6280.2	430.645
444	SEGA91	-2461.2	430.645	494	COM33	-6310.2	430.645
445	SEGB91	-2491.2	430.645	495	COM35	-6340.2	430.645
446	SEGC91	-2521.2	430.645	496	COM37	-6370.2	430.645
447	SEGA92	-2551.2	430.645	497	COM39	-6400.2	430.645
448	SEGB92	-2581.2	430.645	498	COM41	-6430.2	430.645
449	SEGC92	-2611.2	430.645	499	COM43	-6460.2	430.645
450	SEGA93	-2641.2	430.645	500	COM45	-6490.2	430.645

Pin No	Pad Name	Coordinate		Pin No	Pad Name	Coordinate	
		X	Y			X	Y
501	COM47	-6520.2	430.645				
502	COM49	-6550.2	430.645				
503	COM51	-6580.2	430.645				
504	COM53	-6610.2	430.645				
505	COM55	-6640.2	430.645				
506	COM57	-6670.2	430.645				
507	COM59	-6700.2	430.645				
508	COM61	-6730.2	430.645				
509	COM63	-6760.2	430.645				
510	COM65	-6790.2	430.645				
511	COM67	-6820.2	430.645				
512	NC40	-7000.2	430.645				
513	NC41	-7153.28	466				
514	NC42	-7221.39	466.25				
515	NC43	-7221.39	392.98				
516	NC44	-7185.645	135				
517	NC45	-7185.645	-135				
518	NC46	-7221.39	-392.98				
519	NC47	-7221.39	-466.25				

5 Functional Block Diagram

5.1 System Block Diagram

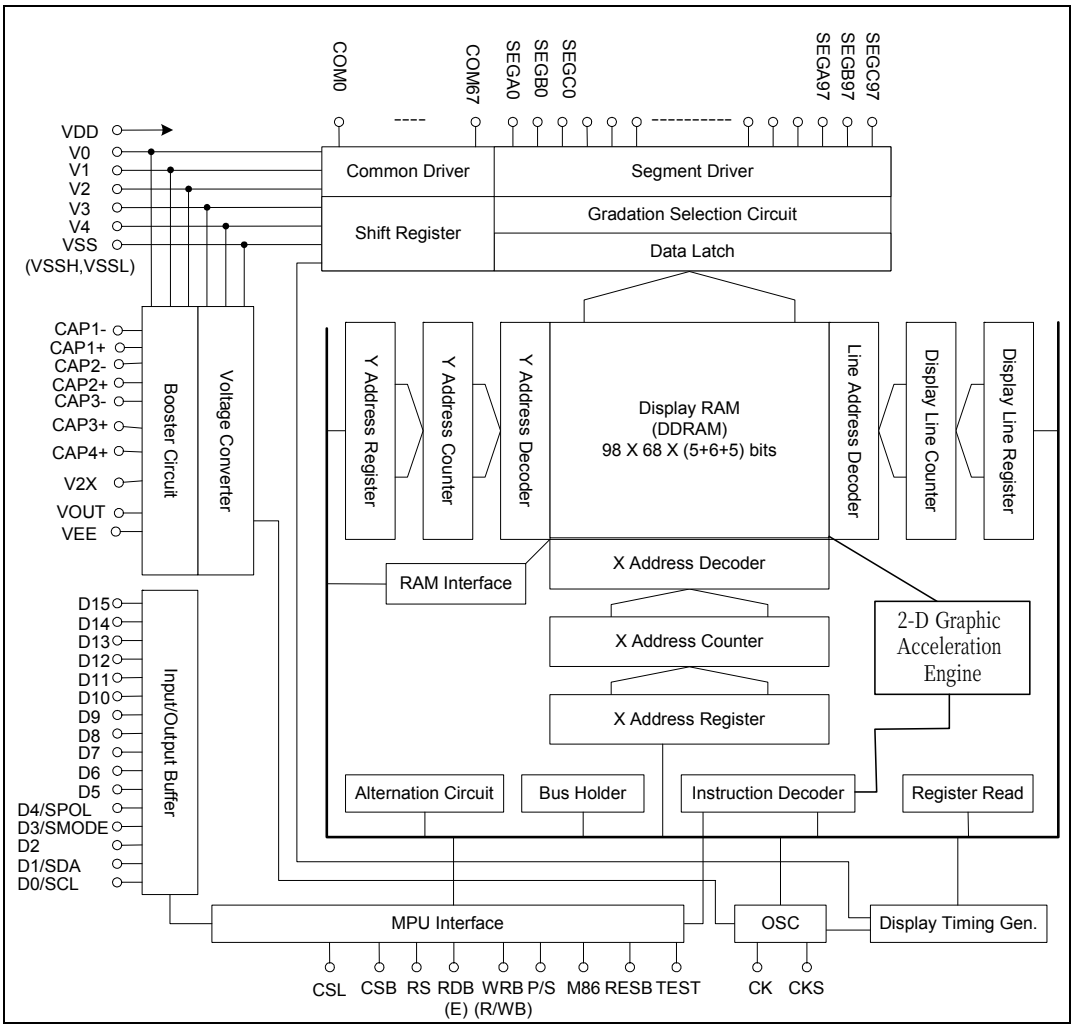


Figure 5 System Block Diagram

6 Pin Descriptions

6.1 Power Supply Pins

Symbol	I/O	Description
VDD1-VDD3	Power Supply	Power supply pin for logic circuit to +2.2 to 3.3V
VSS2-VSS4	Power Supply	Ground pin for logic circuit, connect to 0V
VSS1 VSS5	Power Supply	Ground pin for high voltage circuit, connected to 0V
V0-V4	Power Supply	Bias power supply pin for LCD drive voltage When the internal power supply circuit is active, these voltages are generated by the built-in booster and voltage converter. Then, must connect capacitor each to VSS.

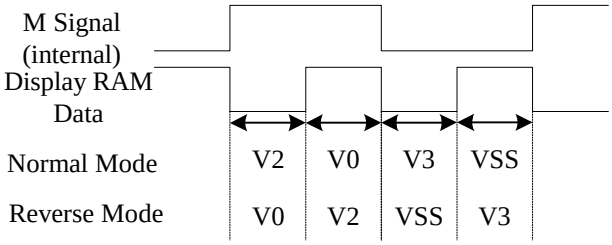
6.2 LCD Power Supply Circuit Pins

Symbol	I/O	Description
CAP1+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP1- and CAP1+.
CAP1-	O	Connecting pin for the built in booster's capacitor – side. The capacitor is connected between CAP1- and CAP1+.
CAP2+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP2- and CAP2+.
CAP2-	O	Connecting pin for the built in booster's capacitor – side. The capacitor is connected between CAP2- and CAP2+.
CAP3+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP3- and CAP3+.
CAP3-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP3- and CAP3+.
CAP4+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP2- and CAP4+.
VEE	Power Supply	Voltage supply pin for booster circuit. Usually the same voltage level as VDD. In the case of TCP, draw it as a separate terminal.
VOUT	O	Output pin of boosted voltage in the built-in booster. The capacitor must be connected between this pin and VSS.
V2X	O	Output pin which is equal to 2 x VEE. The capacitor must be connected between this pin and VSS.

6.3 System Bus Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin.
When RESB is “L”, initialization is executed.</td></tr>
<tr><td>D0/SCL
D1/SDA
D2
D3/SMODE
D4/SPOL
D5-D7</td><td>I/O</td><td>Data bus / Signal interface related pins.
When parallel interface is selected (P/S = “H”), The D7-D0 are 8-bits bi-directional data bus, connect to MPU data bus.
When serial interface is selected (P/S = “L”), D0 and D1 (SCL, SDA) are used as serial interface pins.
SCL: Input pin for data transfer clock
SDA: Serial data input pin
SMODE: Serial transfer mode select pin
SPOL: RS pole select pin when 3-wires serial interface is selected.
SDA data is latched at the rising edge of SCL.
Internal serial/parallel conversion into 8-bit data occurs at the rising edge of 8th clock of SCL
After completing data transferring, or when making no access, be sure to set SCL to “L”.
Useless pins (D7~D0) must be fixed to “H” or “L” on serial transfer mode.</td></tr>
<tr><td>D8-D15</td><td>I/O</td><td>8-bit bi-directional bus. Connected to MPU data bus.
Used as data bus for upper 8-pins in the 16-bits access mode.
Useless pins (D15~D8) must be fixed to “H” or “L” on 8-bits access mode.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip Select input pin.
CSB = “L”: accepts access from MPU
CSB = “H”: denies access from MPU</td></tr>
<tr><td>RS</td><td>I</td><td>RAM/Register select input pin.
RS = “0”: D7-D0 are display RAM data
RS = “1”: D7-D0 are control register data</td></tr>
<tr><td>RDB
(E)</td><td>I</td><td>Read/Write control pin
Select 80-family MPU type (M86 = “L”)
The RDB is a data read signal. When RDB is “L”, D7-D0 are in an output status.
Select 68-family MPU type (M86 = “H”)
R/WB = “H”: When E is “H”, D7-D0 are in an output status.
R/WB = “L”: The data on D7-D0 are latched at falling edge of the E signal.</td></tr>
<tr><td>WRB
(R/WB)</td><td>I</td><td>Read/Write control pin
Select 80-family MPU type (M86 = “L”)
The WRB is a data write signal. The data on D7-D0 are latched at rising edge of the WRB signal.
Select 68-family MPU type (M86 = “H”)
Read/Write control input pin.
R/W = “H”: Read
R/W = “L”: Write</td></tr>
<tr><td>M86</td><td>I</td><td>MPU interface type selecting input pin.
M86 = “H”: 68-family interface
M86 = “L”: 80-family interface
Fixed at either “H” or “L”</td></tr>
<tr><td>TEST</td><td>I</td><td>For testing. Fix to “L”.</td></tr>
<tr><td>DUMMY</td><td>I</td><td>“Floating”</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel/Serial interface select pin.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data identification</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>CSB</td><td>RS</td><td>D0-D7</td><td>RDB, WRB</td><td>-</td></tr>
<tr><td>L</td><td>CSB</td><td>RS</td><td>SDA</td><td>Write only</td><td>SCL</td></tr>
</table>
P/S = “H”: For parallel interface.
P/S = “L”: For serial interface. Fix D15-D5 pins are Hi-Z, RDB and WRB pins to either “H” or “L”.</td></tr>
<tr><td>CSL</td><td>I</td><td>Common output mode selecting input pin.
CSL = “H”: COM0, COM2, COM4, … , COM66 & COM1, COM3, COM5, … , COM67
CSL = “L”: COM0, COM1, COM2, … , COM65, COM66, COM67</td></tr>
</table>

6.4 LCD Drive Circuit Signals

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEGA0-A97
SEGB0-B97
SEGC0-C97</td><td>O</td><td>Segment output pins for LCD drives.
According to the data of the Display RAM data, non-lighted at “0”, lighted at “1” (Normal Mode). non-lighted at “1”, lighted at “0” (Reverse Mode) and, by a combination of M signal and display data, one signal level among V0,V2,V3 and VSS signal levels are selected.
 
</td></tr>
<tr><td>COM0-
COM67</td><td>O</td><td>Common output pins for LCD drivers. By a combination of the scanning data and M signal, one signal level among V0, V1, V4 and VSS signal level is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
</table>

6.5 Oscillating Circuit Pin

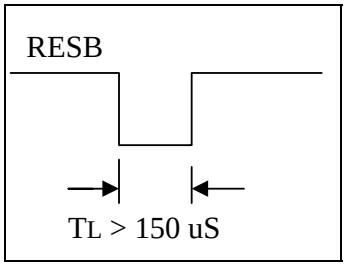
Symbol	I/O	Description
CKS	I	Display timing clock source select input pin. CKS = “H”: Use external clock from CK pin. CKS = “L”: Use internal oscillated clock.
CK	I/O	External clock input pin for display timing (CKS=1) or internal clock output pin for display timing (CKS=0). When using internal oscillated clock, CK must be floating (CKS=0)

7 Function Description

7.1 MPU Interface

7.1.1 Reset Pin Description (RESB)

Holding the RESB low for at least 150μs, then EM65570S accept this reset command.



7.1.2 Interface Type Selection

The EM65570S transfers data through 8-bit parallel I/O (D7-D0), 16-bit parallel I/O (D15-D0) or serial data input (SDA, SCL). The parallel interface or serial interface can select by state of P/S pin. When serial interface is selected, data reading cannot be performed, only data writing can operate.

P/S	I/F Type	CSB	RS	RDB	WRB	M86	SDA	SCL	Data
H	Parallel	CSB	RS	RDB	WRB	M86	-	-	D7~D0 (D15~D0)
L	Serial	CSB	RS	-	-	-	SDA	SCL	-

7.1.3 Parallel Input

When parallel interface is selected with the P/S pin, the EM65570S allows data to be transferred in parallel to an 8-bit/16-bit MPU through the data bus. For the 8-bit/16-bit MPU, either the 80-family MPU interface or the 68-family MPU interface can be selected with the M86 pin.

M86	MPU Type	CSB	RS	RDB	WRB	Data
H	68-family MPU	CSB	RS	E	R/WB	D7~D0 (D15~D0)
L	80-family MPU	CSB	RS	RDB	WRB	D0~D7 (D15~D0)

7.1.4 Read/Write functions of Register and display RAM

The EM65570S have four read/write functions at parallel interface mode. Each read/write function selecting by combinations of RS, RDB and WRB signals.

RS	68-family R/WB	80-family		Function
		RDB	WRB	
1	1	0	1	Read internal Register
1	0	1	0	Write internal Register
0	1	0	1	Read display data
0	0	1	0	Write display data

7.1.5 Serial Interface

EM65570S has two types serial interface, namely, 3-wire type serial interface; and 4-wire type serial interface, both are determined by the SMODE pin.

SMODE = “L”: 4-wires serial interface

SMODE = “H”: 3-wires serial interface

7.1.6 4-wire Serial Interface

When chip select is active (CSB = “L”), 4-wires type serial interface can work through the SDA and SCL input pins. When chip select is inactive (CSB = “H”), the internal shift register and counter are reset in the initial condition. Serial data SDA are input sequentially in order of D7 to D0 at the rising of serial clock (SCL) and are converted into 8-bit parallel data (by serial to parallel conversion) at the rising edge of the 8th serial clock, being processed in accordance with the data. The identification whether are serial data inputs (SDA) are display data or control register data is judged by input to RS pin.

RS = “L”: display RAM data

RS = “H”: control register data

After completing 8-bit data transfer, or when making no access, be sure to set serial clock input (SCL) to “L”. Cares of SDA and SCL signals against external noise should be taken in board writing. To prevent transfer error due to external noise, release chip select (CSB = “H”) every completion of 8-bit data transferring.

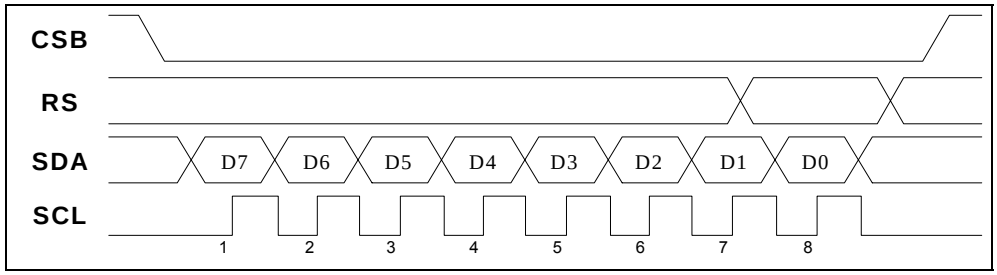


Figure 7-1 4-wire Type Serial Interface

7.1.7 3-wire Type Serial Interface

When chip select is active (CSB = “L”), 3-wires type serial interface can work through the SDA and SCL input pins. When chip select is inactive (CSB = “H”), the internal shift register and counter are reset in the initial condition. Serial data SDA are input sequentially in order of RS, D7 to D0 at the rising edge of serial clock (SCL) and are converter into 9-bit parallel data (by serial to parallel conversion) at the rising edge of the 9th serial clock.

The identification whether the serial data inputs (SDA) are display data or control register data is determined by first serial input data (RS) and SPOL pin as follows:

SPOL = "0"		SPOL = "1"	
RS	Display RAM/Register	RS	Display RAM/Register
0	Display RAM Data	0	Control Register Data
1	Control Register Data	1	Display RAM Data

After completing 9-bits data transfer, or when making no access, be sure to set serial clock input (SCL) to "L". Cares of SDA and SCL signals against external noise should be taken in board wiring. To prevent transfer error due to external noise, release chip select (CSB = "H") every completion of 9-bit data transferring.

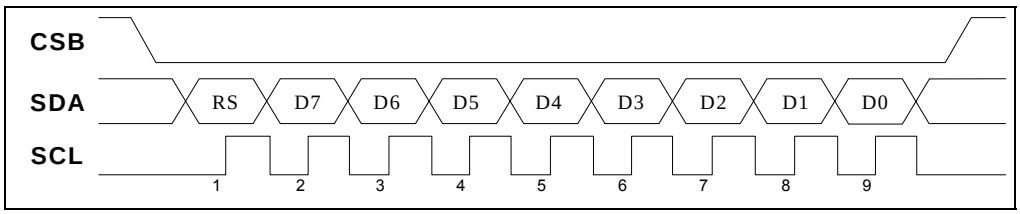


Figure 7-2 3-Wires Type Serial Interface

7.2 Data Write to Display RAM and Control Register

The data write to display RAM and Control Register use almost same procedure, only different setting of RS that select access object.

RS = "L": Display RAM data

RS = "H": Control register data

In the case of the 80-family MPU, the data is written at the rising edge of WRB. In the case of the 68-family MPU, the data is written at the falling edge of signal E.

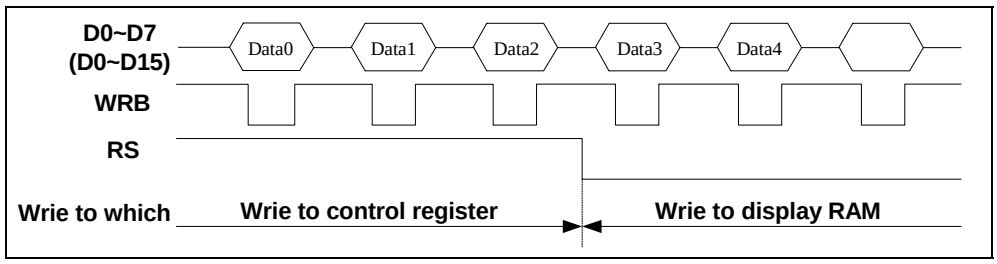


Figure 7-3 Data write operation

7.3 Display RAM Read and Control Register Read

In the case of display RAM read operation, need dummy read one time. The designated address data are not output to read operation immediately after the address set to AX or AY register, but are output when the second data read. Dummy read is always required one time after address set and write cycle.

Read display RAM operation

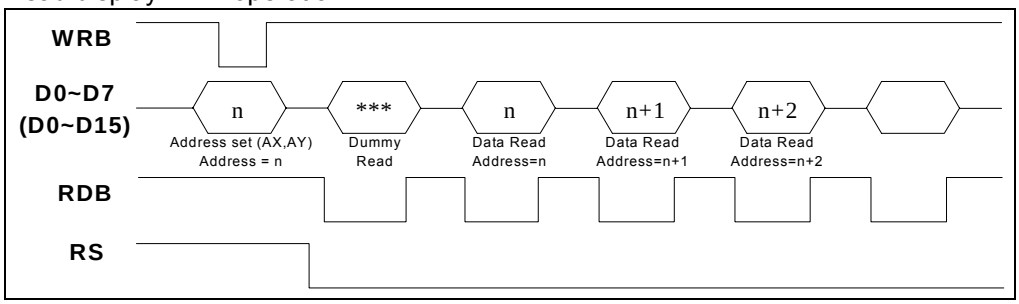


Figure 7-4 Read display RAM operation

The EM65570S can read the control registers, in case of control register read operation, data bus upper nibble (D7-D4) use for register address (0 to FH). In maximum, 16 registers can access directly. But number of register is more than 16 registers. Therefore, EM65570S has register bank control. The RE register is set bank number to access. And the RE address is 0FH, in any bank can access RE register. It is need 4-steps to read the specific register in maximum case.

(1) Write 04H to RE register for access to RA register.

(2) Writes specific register address to RA register.

(3) Write specific register bank to RE register.

(4) Read specific register contents.

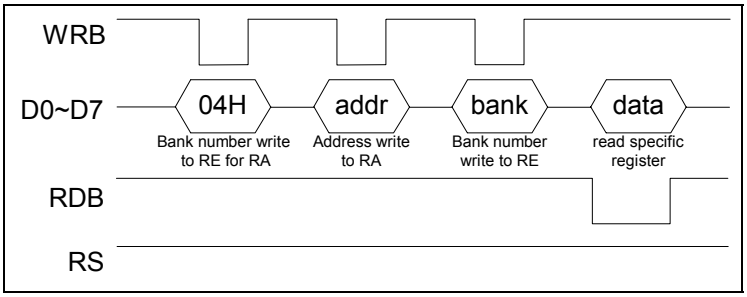


Figure 7-5 Register Read Operation

7.4 16-bit Data Access to Display RAM

The EM65570S correspond to 8-bits and 16-bits bus size access.

The data bus size can select by WLS register.

WLS = “0”: 8-bit bus size

WLS = “1”: 16-bit bus size

For 6-bit access mode, low-byte data bus (D7~D0) is used to access the control register. High byte data bus (D15~D8) are not used in internal circuit. When the control register is read using 16-bit bus, register values output to D3-D0 and D15-D4 output “H”.

7.5 Fast Burst RAM Write Function

The EM65570S has built-in fast burst RAM write function, because the burst mode transfer which transfers 32-bits data block at once, so it can decrease half the access time needed for common standard RAM write function (16 bits data bus). The burst RAM write function is suitable for frequently data rewriting such as displaying color animation.

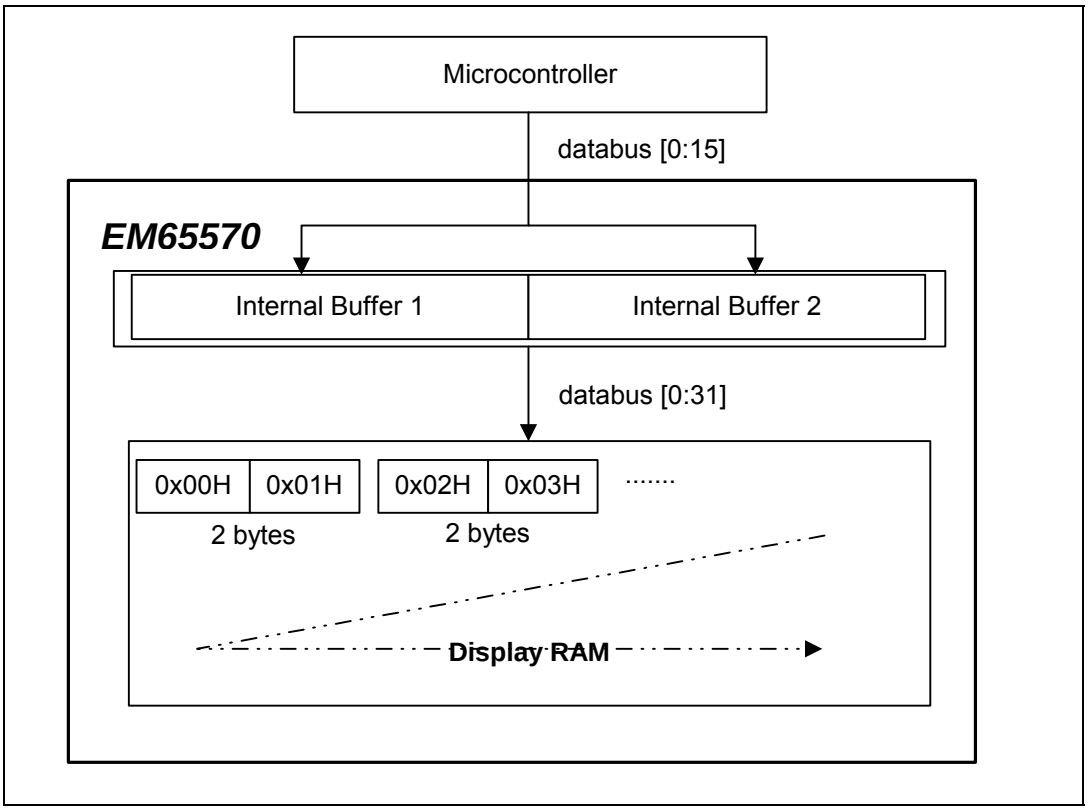


Figure 7-6 Burst RAM Write Operation

NOTE

Fast Burst RAM Write Function is used effectively only in horizontal RAM data writing mode, that is, RDWS[2]=0

7.6 Common Output Mode Selection

The EM65570S has two common output modes. You can select the correct common output mode to fit LCM ITO layout type. The common output mode can select by 'CSL' pin option.

CSL="0": COM0, COM1, COM2, … , COM65, COM66, COM67

CSL="1": COM0, COM2, … , COM66 & COM1, COM3, … , COM67

7.7 Display RAM Access Using Windows Function

The EM65570S has window area setting command for specified display RAM area access. In using the window function, it is required to set up two positions, X and Y address. It is also needed to set up auto increment mode (AXI="1", AYI="1"). Two position means window start position and window end position. The window start position's X and Y address set to normal X address (AX) and Y address (AY) registers. The window end position's X and Y address set to Window X End Address (EX) and Window Y End Address (EY) register. In window function access, can use modify write access with set to AIM="1". In case of using window function access, the following registers should be set before accessing the RAM.

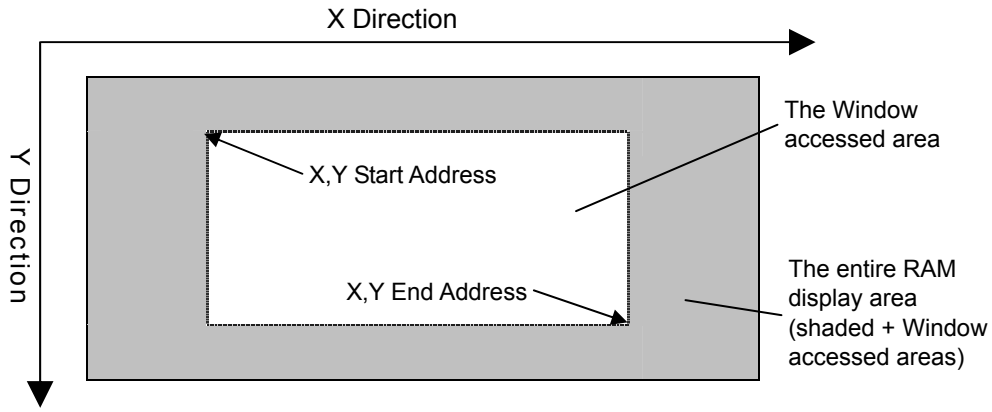
WIN = "1", AXI="1", AYI="1"

X Address, Y Address, Window X End Address, Window Y End Address

The following address conditions should also be kept.

Window end X address (EX) ≧ Window start X address (AX)

Window end Y address (EY) ≧ Window start Y address (AY)



7.8 Relationship between Display RAM and Address

The EM65570S execute address conversion that depends on control register setting. In case of auto increment mode, usually AX register is added one. For instance when REF and AXI are both "1", AX register is added one, but effective X address seems decrement because of address conversion. The effective Y address uses AY register values as it is.

7.8.1 Gradation Mode (256 Color), (C256=1, 65K=0)

8-bit mode (WLS=0)

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assignment															
*	*	0	0	X=00H									X=61H						
*	*	1	1	X=61H									X=00H						
				D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7
				SEG A0		SEG B0			SEG C0				SEG A97		SEG B97			SEG C97		

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assignment															
*	*	0	1	X=00H									X=61H						
*	*	1	0	X=61H									X=00H						
				D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7
				SEG C0		SEG B0			SEG A0				SEG C97		SEG B97			SEG A97		

16-bit mode(WLS=1)

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assignment																											
*	*	0	0	X=00H															X=30H												
*	*	1	1	X=30H															X=00H												
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				SEG A0		SEG B0		SEG C0		SEG A1		SEG B1		SEG C1						SEG A96		SEG B96		SEG C96		SEG A97		SEG B97		SEG C97			

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																											
*	*	0	1	X=00H															X=30H												
*	*	1	0	X=30H															X=00H												
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				SEG A1		SEG B1		SEG C1		SEG A0		SEG B0		SEG C0						SEG A97		SEG B97		SEG C97		SEG A96		SEG B96		SEG C96			

7.8.2 Gradation Mode (4096 colors), (C256=0, 65K=0)

8 bits mode (WLS="0")

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																			
0	*	0	0	X=00H				X=01H								X=C2H				X=C3H			
0	*	1	1	X=C2H				X=C3H								X=00H				X=01H			
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7
				SEG A0				SEG B0				SEG C0				SEG A97				SEG B97				SEG C97			

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																			
0	*	0	1	X=00H				X=01H								X=C2H				X=C3H			
0	*	1	0	X=C2H				X=C3H								X=00H				X=01H			
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7
				SEG C0				SEG B0				SEG A0				SEG C97				SEG B97				SEG A97			

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																			
1	*	0	0	X=00H								X=01H				X=91H				X=92H			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				SEG A0				SEG B0				SEG C0				SEG A97				SEG B97				SEG C97			

HSW	ABS	REF	SWAP	X Address / Data bus / Segment assign																			
1	*	1	1	X=91H				X=92H								X=00H							X=01H
				D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3
				SEG A0				SEG B0				SEG C0				SEG A97				SEG B97				SEG C97			

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																			
1	*	0	1	X=00H								X=01H				X=91H				X=92H			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				SEG C0				SEG B0				SEG A0				SEG C97				SEG B97				SEG A97			

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																											
1	*	1	0	X=91H				X=92H									X=00H								X=01H						
				D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3				
				SEG C0				SEG B0				SEG A0					SEG C97				SEG B97				SEG A97						

16 bits mode (WLS="1")

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																											
*	0	0	0	X=00H													X=61H														
*	0	1	1	X=61H													X=00H														
				D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15		D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15				
				SEG A0					SEG B0				SEG C0				SEG A97					SEG B97				SEG C97						

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																											
*	0	0	1	X=00H													X=61H														
*	0	1	0	X=61H													X=00H														
				D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15		D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15				
				SEG C0					SEG B0				SEG A0				SEG C97					SEG B97				SEG A97						

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																											
*	1	0	0	X=00H													X=61H														
*	1	1	1	X=61H													X=00H														
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11				
				SEG A0					SEG B0				SEG C0				SEG A97					SEG B97				SEG C97						

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign																											
*	1	0	1	X=00H													X=61H														
*	1	1	0	X=61H													X=00H														
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11				
				SEG C0					SEG B0				SEG A0				SEG C97					SEG B97				SEG A97						

7.8.3 Gradation mode (65K Color), (C256=0, 65K=1)

8-bit mode (WLS=0)

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign					
*	*	0	0	X=00H	X=01H	X=C2H	X=C3H		
*	*	1	1	X=C2H	X=C3H	X=00H	X=01H		
				D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7		
				SEG A0	SEG B0	SEG C0	SEG A97	SEG B97	SEG C97

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign					
*	*	0	1	X=00H	X=01H	X=C2H	X=C3H		
*	*	1	0	X=C2H	X=C3H	X=00H	X=01H		
				D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7		
				SEG C0	SEG B0	SEG A0	SEG C97	SEG B97	SEG A97

16-bit mode (WLS=1)

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign					
*	*	0	0	X=00H		X=61H			
*	*	1	1	X=61H		X=00H			
				D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15		D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15			
				SEG A0	SEG B0	SEG C0	SEG A97	SEG B97	SEG C97

HSW	ABS	REF	SWAP	X Address / Data Bus / Segment Assign					
*	*	0	1	X=00H		X=61H			
*	*	1	0	X=61H		X=00H			
				D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15		D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15			
				SEG C0	SEG B0	SEG A0	SEG C97	SEG B97	SEG A97

7.9 Display Data Structure and Gradation Control

For the purpose of gradation control, one pixel requires multiple bits of display RAM. The EM65570S has 5-bit data per output to achieve the gradation display.

The three outputs of the segment driver are used for one pixel of RGB, and the EM65570S is connected to an STN color LCD panel. It can display 98*68 pixels with 65K colors (5 bits * 6 bits [5+FRC] * 5 bits). In this case, since the gradation display data is processed by a single access to the memory, the data can be rewritten fast and naturally.

The weighting for each data bit is dependent on the status of the SWAP bit that is selected when data is written to the display RAM.

7.10 Gradation LSB Control

In 256 color mode (C256=1), the EM65570S provides segment driver output for 8-gradation display using 3-bits and that for 4-gradation display using 2-bits.

The segment driver output for the 4-gradation display uses 2-bits written to the corresponding RAM area and 1-bit supplemented by the gradation LSB circuit, and then selects 4-gradation from 8-gradation.

In 256 color mode (C256=1), the segment driver output for the 4-gradation display result in a gradation level of 0 regardless of the gradation LSB, when 2-bits of data on the display RAM are “00”. When 2-bits of data on the display RAM is “11”,a gradation level of 7/7 is selected regardless of the bit information of the gradation LSB. The other gradation levels are selected depending on 2-bits of data on the display RAM and the gradation LSB bits.

One bit of data is supplemented by setting the gradation LSB register (GLSB).
The Gradation LSB control bit applied to all 4-gradation segment drivers.
Gradation LSB = “0”: Selects 0 as the LSB information on the RAM for 4-gradation segment drivers.

Gradation LSB = “1”: Selects 1 as the LSB information on the RAM for 4-gradation segment drivers.

7.11 Generation of the Alternate Signal (M)

LCD alternated signal (M) is generated by the display clock (D_CK). The M generates alternated drive waveform to the LCD drive circuit. Normally, the M generates alternated drive waveform every frame (Frame-signal level is reversed every one frame). However, by setting up data (n-1) in an n-line reverse register and n-line alternated control bit (NLIN) at “1”, n-line reverse waveform is generated.

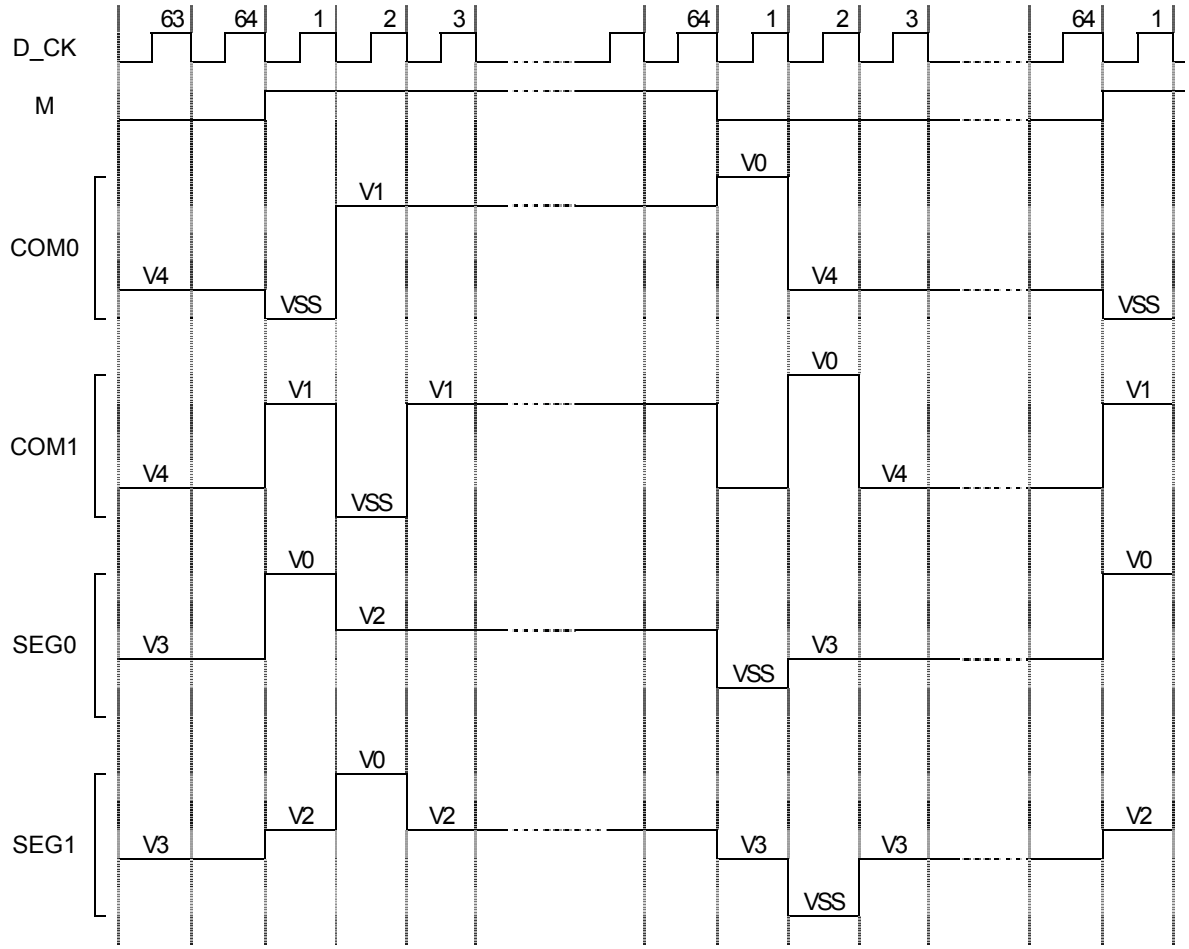
When NLIN = “H” :

EOR=0 M always reverses on the nth raster row regardless of whether the end of a frame is reached.

EOR=1 M reverses at the nth raster row and restarts the raster row count at the start of every frame.

7.12 Output Timing of LCD Driver

Display timing in Normal mode (not reverse mode), 1/64 duty.



7.13 Oscillating Circuit

The EM65570S has an RC oscillator. The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster.

When external clock is used, feed the clock to CK pin.

The duty cycle of the external clock must be 50%.

The resistance ratio of CR oscillator is programmable. If change this ratio, also change frame frequency for display.

7.14 Power Supply Circuit

This circuit supplies voltages necessary to drive an LCD. The circuit consists of booster and voltage converter.

Boosted voltage from the booster is fed to the voltage converter that converts this input voltage into V0, V1, V2, V3 and V4 that are used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many pixels. Otherwise, display quality will degrade considerably. The power circuit can be control by power circuit related register.

DCON	AMPON	Booster Circuit	Voltage Conversion Circuit
0	0	disable	disable
1	1	enable	enable

7.15 Booster Circuit

Placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3-, across CAP4+ and CAP2- and across VOUT and VSS boosts the voltage coming from VEE and VSS n-times and outputs the boosted voltage to VOUT pin. The twice, third, fourth or fifth boosted voltages are output to the VOUT pin by the boost step register set. The boost step registers set by the command.

When use built-in booster circuit, output voltage (VOUT) must less than recommended operating voltage (19 Volt). If output voltage (VOUT) is beyond the recommended operating voltage, proper function of the IC cannot be guaranteed.

7.16 Electronic Volume

The voltage conversion circuit has built-in an electronic volume, which allows VEV to be controlled with DV register setting. The DV registers are 7-bits, so can select 128 voltage values for the VEV voltage. The relationship between VEV and DV is given by follows equation:

VEV=K * (373 + (DV+CV)) ---------- (1)

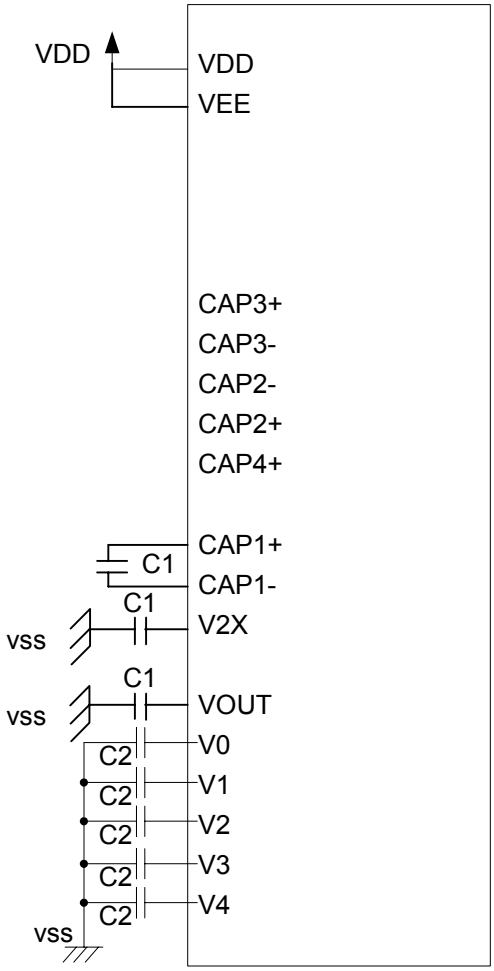
DV: Electronic volume setting value

CV: Vop offset setting value of OTP

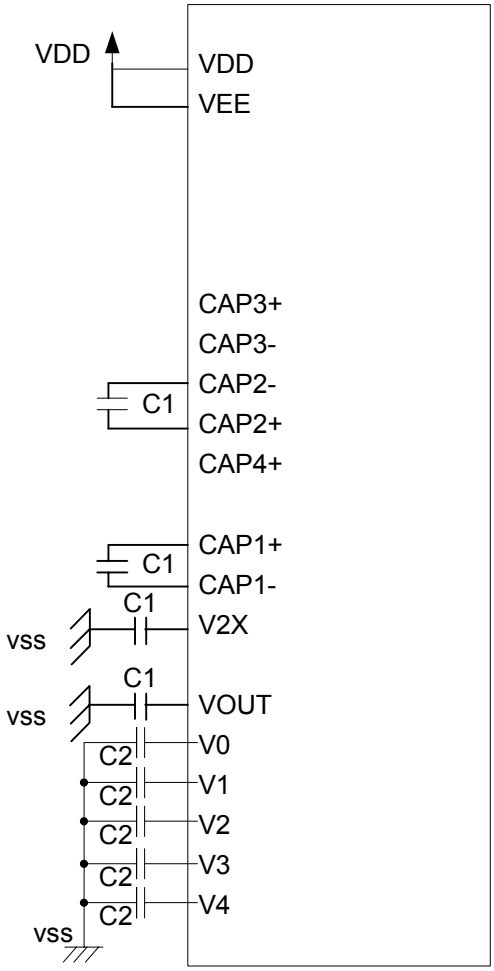
K: Coefficient 4.005 * 10^{-3}

7.17 Voltage Generation Circuit

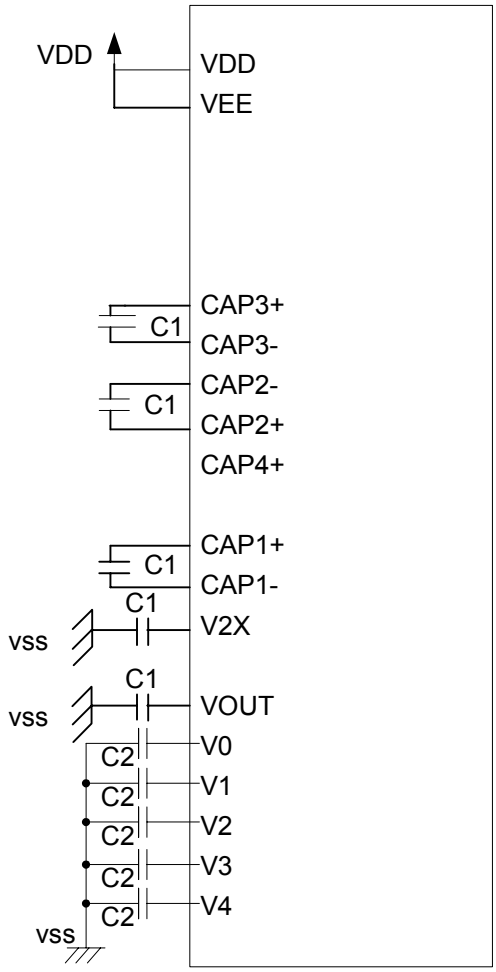
The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V0, i.e., V1, V2, V3 and V4 are obtained by dividing V0 through a resistor network. The LCD drive voltage from EM65570S is biased at 1/4, 1/5, 1/6, 1/7, 1/8, 1/9. When using the internal power supply, connect a stabilizing capacitor C2 to each of pins V0 to V4. The capacitance of C2 should be determined while observing the LCD panel to be used.



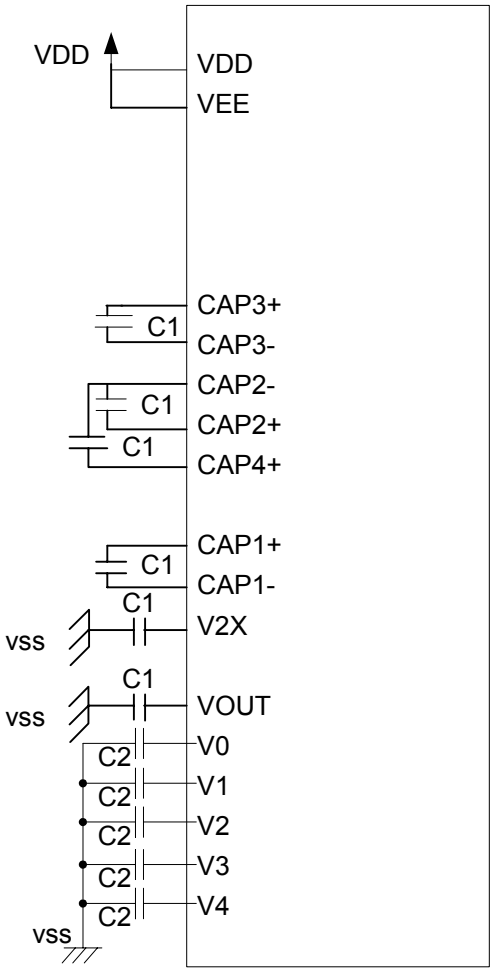
When using internal power circuit.
(2 times boosting)



When using internal power circuit.
(3 times boosting)



When using internal power circuit
(4 times boosting)



When using internal power circuit
(5 times boosting)

Recommended value

C1	1.0 to 1.5 μf
C2	1.0 to 1.5 μf

7.18 2-D Graphic Acceleration Engine

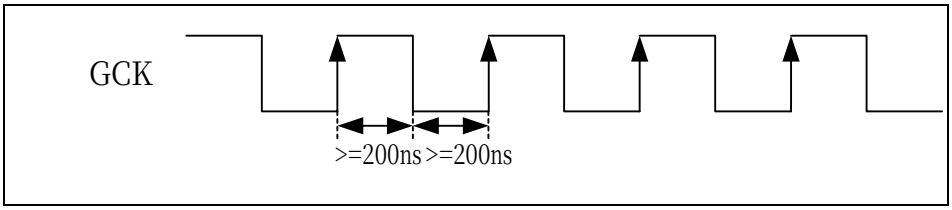
EM65570S has 2-D graphic acceleration engine to support graphic functions including “Draw Rectangle”, “Dim function”, “Copy function”, and “Clear function”. User must generate clock yourself to support to graphic engine in all graphic function. Hardware will write data to display RAM at rising edge of GCK signal. The GCK signal can be ‘WRB’, ‘E’, ‘SCL’ as shown below:

Interface	GCK Signal Definition
Parallel 80-family	WRB
Parallel 68-family	E
Serial	SCL

NOTE

1: Time of 'H' or 'L' level of GCK must be larger than 200 ns.

*2: **The sequence of generating clock code must be setting GCK to '0' first, then setting to '1'. That is**, GCK=0 → GCK=1 → GCK=0 → GCK=1 ……*



The RAM writing mode of graphic function is fixed to column address increasing and row address increasing, that is RDWS[2:0]=000 of RAM writing mode. It is unconcerned with the RAM writing mode user selected.

(1) Draw Rectangle

Give the starting point (X1, Y1) and the ending point (X2, Y2), then set line color and fill color, graphic engine will draw rectangle with the specified line color and fill color. If 'FILL' control bit is disabled, the enclosed area will not be filled. Remarks: X1<= X2; Y1<= Y2; X2 <= 97; Y2 <= 67

It should be noted that the generated clock numbers for graphic engine must be based on the rectangle size, the pixel numbers are also enclosed by a rectangle area, the formula is shown below:

Draw rectangle & fill enable

GCK clock numbers = (End X – Start X + 1) * (End Y – Start Y + 1) + dummy clock numbers ……equation (1)

Draw rectangle & fill disable

GCK clock numbers = [(End X – Start X + 1) + (End Y – Start Y + 1)] * 2 + dummy clock numbers ……equation (2)

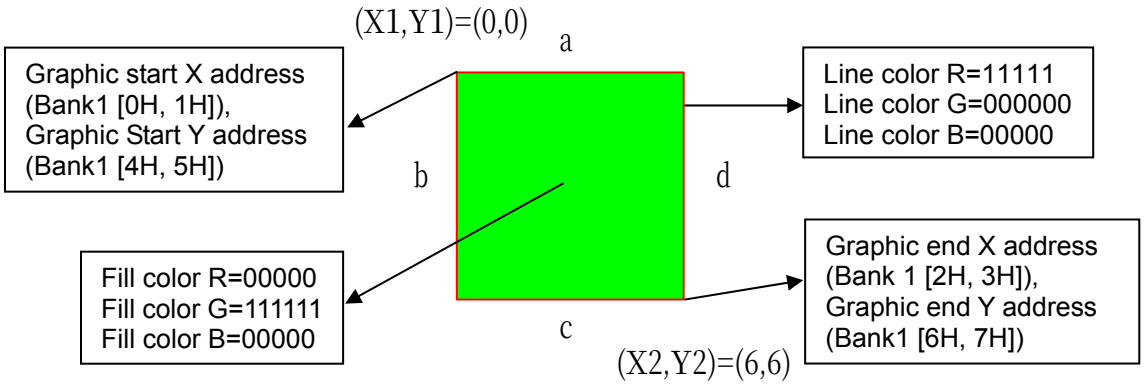
The required dummy clock numbers for graphic function is shown below:

Function	Dummy Clock Numbers
FILL & RECT	7
COPY	1
DIM	1
CLR	1
RECT	2

NOTE

1. *When drawing is completed, GCK signal must be disabled to prevent other un-wanted data writing.*
2. *The sequence of hardware operation is "fill color" → "draw 'a'" → "draw 'c'" → "draw 'b'" → "draw 'd'"*
3. *The draw rectangle and fill function can use mixed, but fill color only but not to draw rectangle is not permitted.*

Fill	Rect	Condition
0	0	Initial value
0	1	Draw rectangle but not fill color
1	0	Inhibited to use
1	1	Draw rectangle and fill color

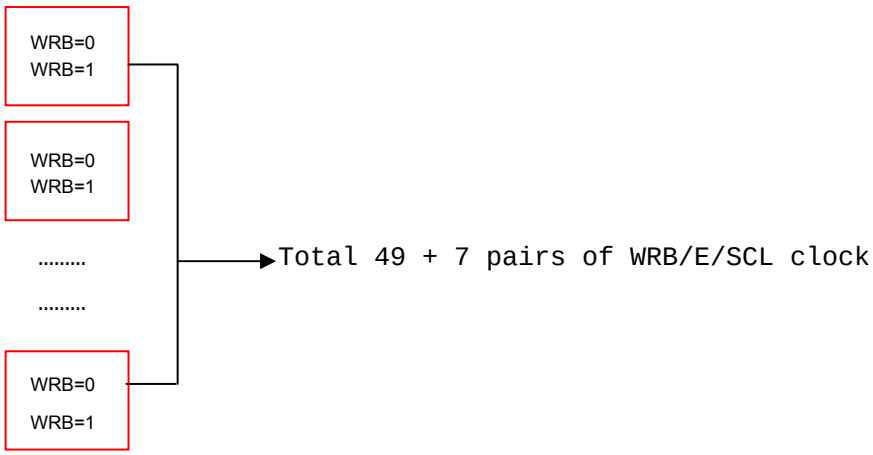


Sample code:

```
---- set starting point (X1,Y1) and ending point (X2,Y2)-------
WRITE 0xF1     //Bank 1
WRITE 0x10     //Graphic start X address (up nibble)
WRITE 0x00     //Graphic start X address (low nibble)
WRITE 0x30     //Graphic end X address (up nibble)
WRITE 0x26     //Graphic end X address (low nibble)
WRITE 0x50     //Graphic start Y address (up nibble)
WRITE 0x40     //Graphic start Y address (low nibble)
WRITE 0x70     //Graphic end Y address (up nibble)
WRITE 0x66     //Graphic end Y address (low nibble)
------------- set line color RGB ------------------------
WRITE 0xA1    //Line color R (up nibble)
```

```
WRITE 0x9F    //Line color R (low nibble)
WRITE 0xC0    //Line color G (up nibble)
WRITE 0xB0    //Line color G (low nibble)
WRITE 0xE0    //Line color B (up nibble)
WRITE 0xD0    //Line color B (low nibble)
---------------- set fill color RGB -------------------
WRITE 0xF2    //Bank 2
WRITE 0x10    //Fill color R (up nibble)
WRITE 0x00    //Fill color R (low nibble)
WRITE 0x33    //Fill color G (up nibble)
WRITE 0x2F    //Fill color G (low nibble)
WRITE 0x50    //Fill color B (up nibble)
WRITE 0x40    //Fill color B (low nibble)
--- set FILL enable/disable and RECT enable to start drawing --
WRITE 0xF1    //Bank 1
WRITE 0x83    //Fill enable; Draw rectangle enable (hardware start
drawing operation

-------- generate graphic engine timing clock(WRB/E/SCL) --------
```




```
-------------------- Disable WRB signal ------------------
WRB=1  //WRB signal disable to prevent other un-wanted data writing
```

(2) Dim

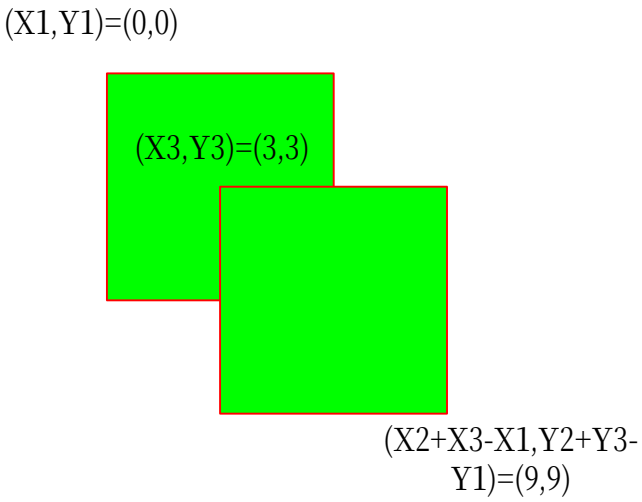
When the 'DIM' control bit of Bank 2 [6H] is set to 1, this function will dim the window area specify by starting point (X1, Y1) and the ending point (X2, Y2). After Dimming operation, the selected window area will be dimmed by 50% black or 50% white according to 'DBW' control bit of Bank 2[6H].

DIM=0, Dim function disable ; DIM=1, Dim function enable

DBW=0, dim 50% black ; DBW=1, dim 50% white

It should be noted that the needed clock numbers generated is the same as that in equation (1)

(3) Copy



When 'COPY' control bit of Bank 2 [6H] is set to 1, copy function will copy the rectangle defined by the starting point (X1, Y1) and the ending point (X2,Y2) to the destination point (X3,Y3). Remarks: X1 <= X2; Y1 <= Y2; X2 <= 127; Y2 <= 127

NOTE

1: As long as the copy destination address ≧ 0, user can copy to anywhere on the display area (or in RAM) by copy function.

2: When the rectangle area exceeds the display panel area (or RAM) using copy function, the parts that exceeded will not be displayed.

3: The needed clock numbers generated is the same with equation (1)

(4) Clear

When 'CLR' control bit of Bank 2 [6H] is set to 1, this function will clear the window area display defined by starting point (X1, Y1) and the ending point (X2, Y2). The Display RAM contents of the window will be set to 0.

It should be noted that the needed clock numbers generated is the same as that in equation (1)

7.19 OTP Function

EM65570S supports OTP function to tune (1) LCD operating voltage Vop. It can also select OTP operating mode, and OTP power from internal or external. In OTP select register (Bank5 [AH]), using (M1, M0) to select the operating mode for OTP, (M1, M0)=00 → Read information from OTP; (M1, M0)=01 → Program information to OTP; (M1, M0)=10 → Reserved; (M1, M0)=11 → OTP standby mode.

(M1, M0)	OTP Operating Mode
00	Read
01	Program
10	Reserve
11	Standby

In program mode, the delay time needed is more than 1 ms.

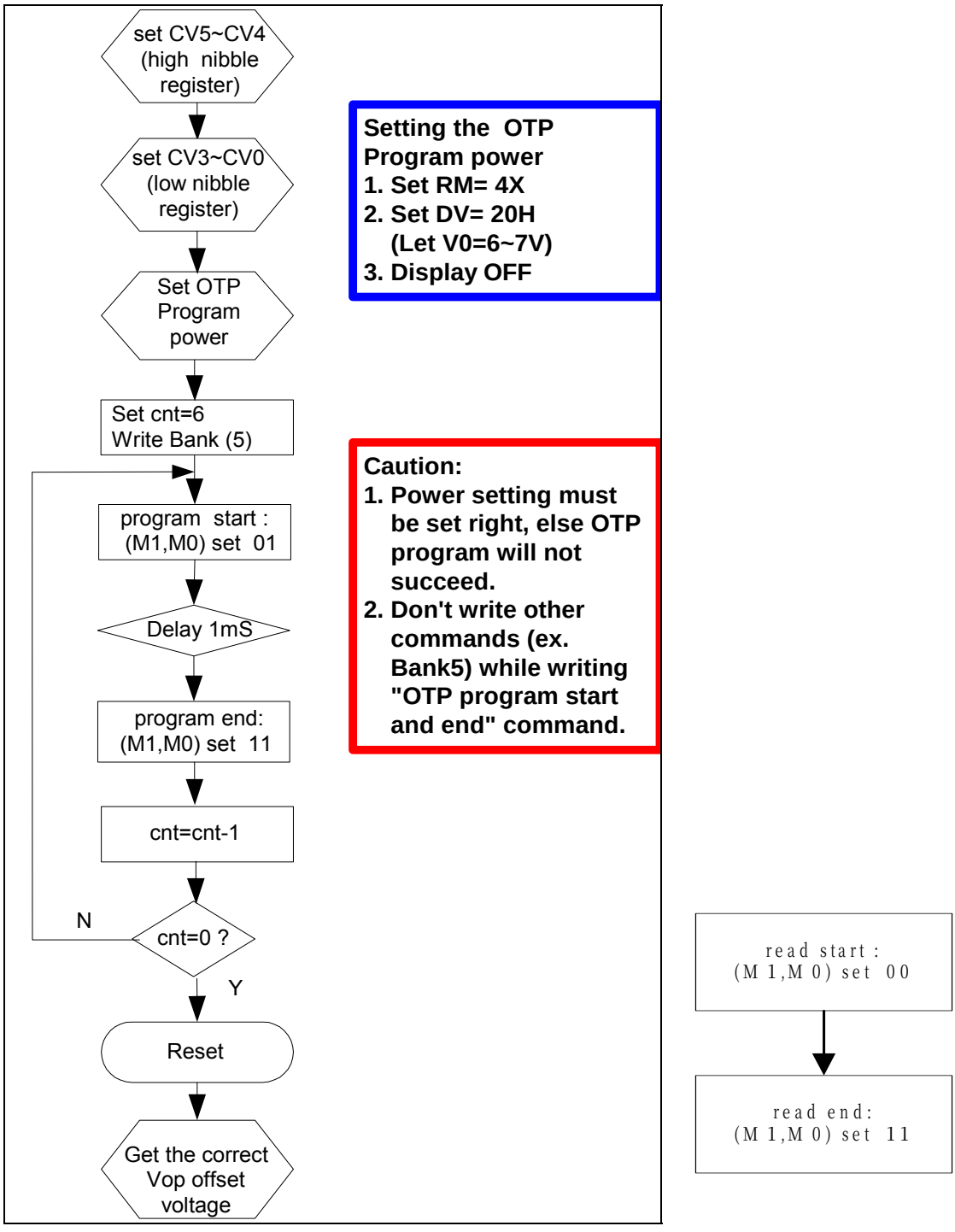
Vop calibration offset voltage can be achieved by setting the Vop calibration offset register (Bank 5 [BH & EH]).

CV5~CV0	Calibration Offset
011111	+31
011110	+30
…	…
000001	+1
000000	0
100000	-32
100001	-31
…	…
111111	-1

VEV=K*(373+(DV+CV)) K=4.005 * 10^{-3}

V0 = VEV * N N : RM register setting

The program flow chart of reading the OTP to get the correct Vop offset voltage are shown as follows:



Program **Read**

7.20 Partial Display Function

The EM65570S has a partial display function, which can display part of the graphic display area. This function is used be set lower bias ratio, lower boost step, and lower LCD drive voltage. Since setting partial display function, EM65570S provides low power consumption. Partial display function is the most suitable for clock indication or calendar indication when a portable equipment is stand-by.

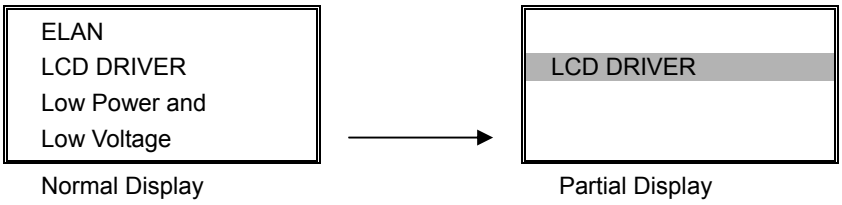
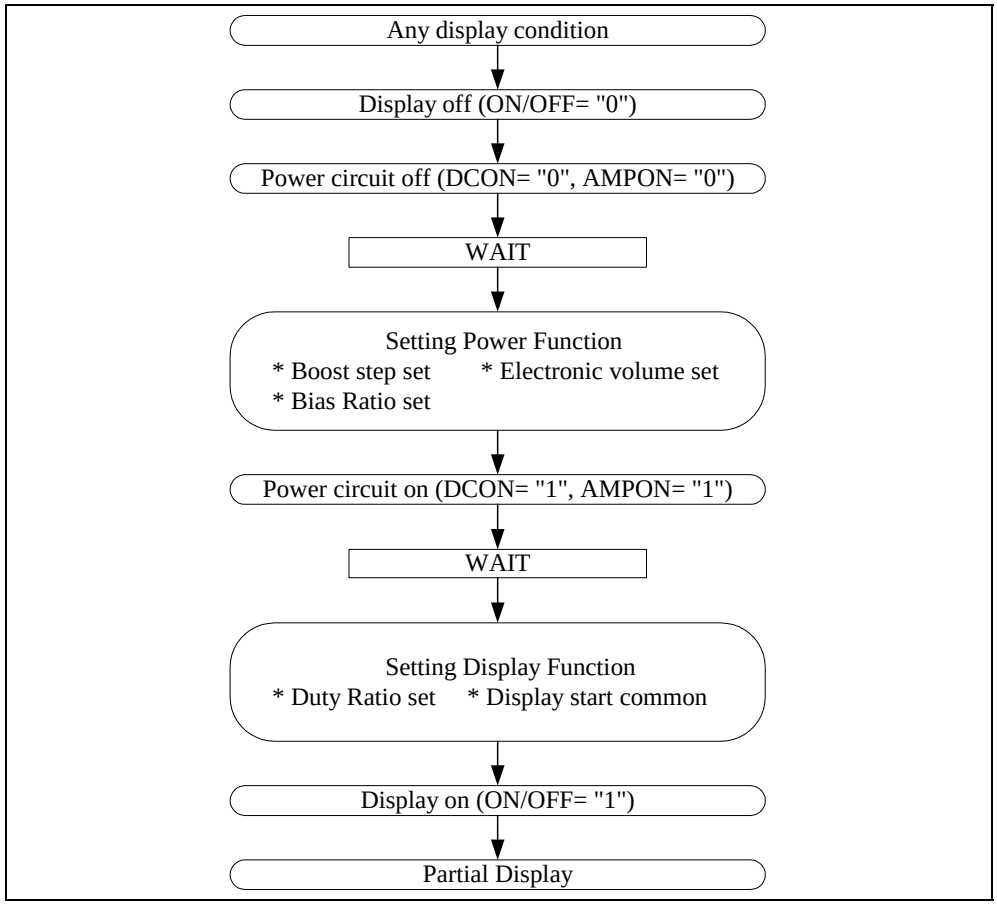


Figure 7-7 Image of Partial Display

When using the partial display function, it is necessary to keep following sequence.



Select a display duty ratio for the partial display from 1/8 to 1/72 using the DS (LCD duty ratio) register.

Set the most suitable values for LCD drive bias ratio, LCD drive voltage, electronic volume, the number of boosting steps, and others according to the actually used LCD panel and the selected duty ratio.

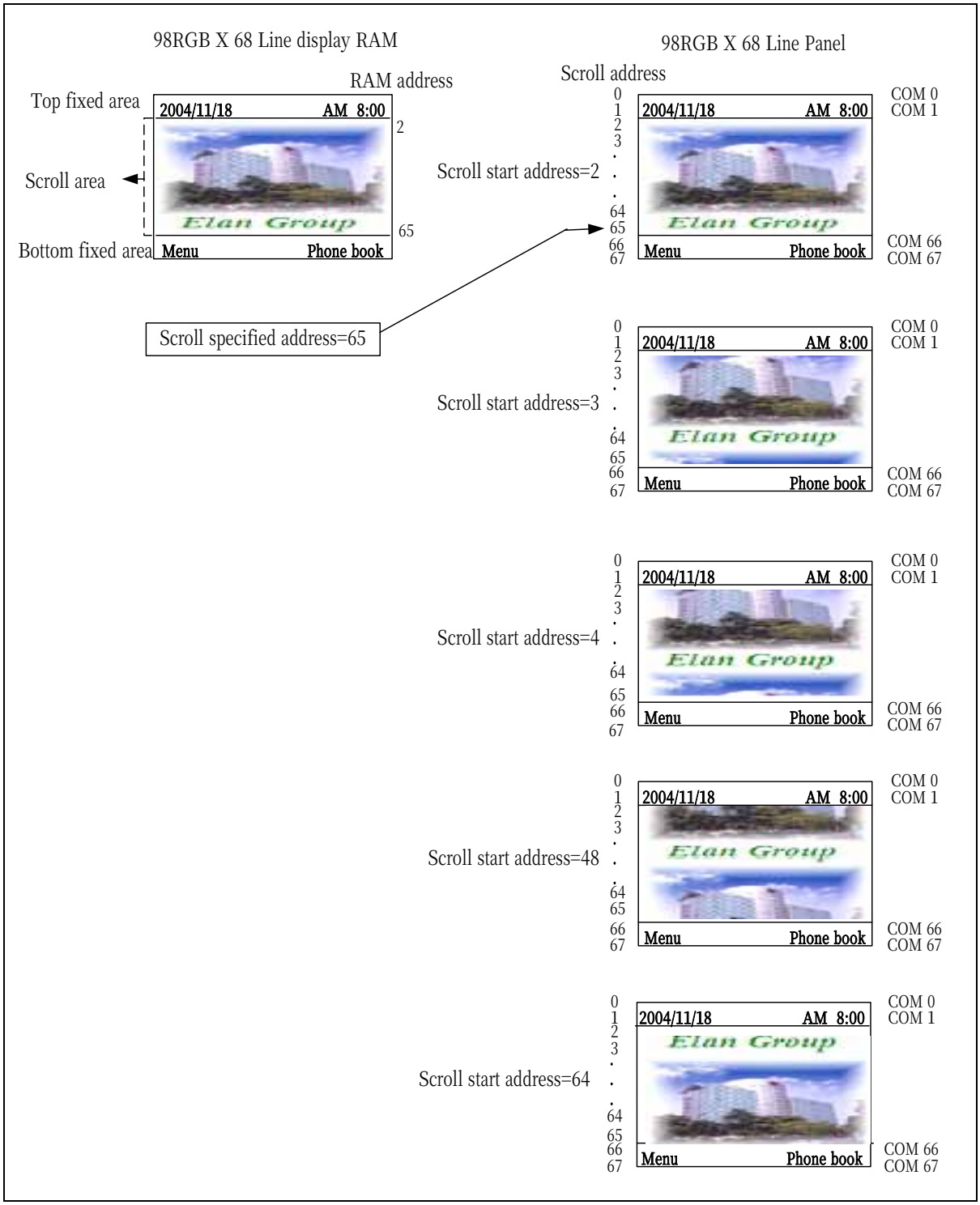
7.21 Discharge Circuit

The EM65570S has built-in the discharge circuit, which discharges electricity from capacitors for a stability of power sources (V0~V4).

The discharge circuit is valid, while the DIS register is set to “1”. When the built-in power supply is used, should be set DIS=”1” after the power source is turned off (DCON, AMPON)=(0, 0). And don’t turn on both the built-in power source and the external power source (V0~V4, VOUT) while DIS=”1”.

7.22 Scroll Function

This function specifies the portion of screen for scrolling. It sets scroll top address, scroll bottom address, scroll specified address, scroll mode of the area scrolling, and scroll start address. Please be noted that the scroll top address should be smaller than the scroll bottom address. Remarks: 0 <= scroll top address, scroll bottom address, scroll specified address <= 67; scroll top address <= scroll start address <= scroll bottom address.



Sample code:

```
-----------------set duty ratio=1/72 --------------------
WRITE 0xF0      //Bank 0
WRITE 0xC6      //duty=1/72
```

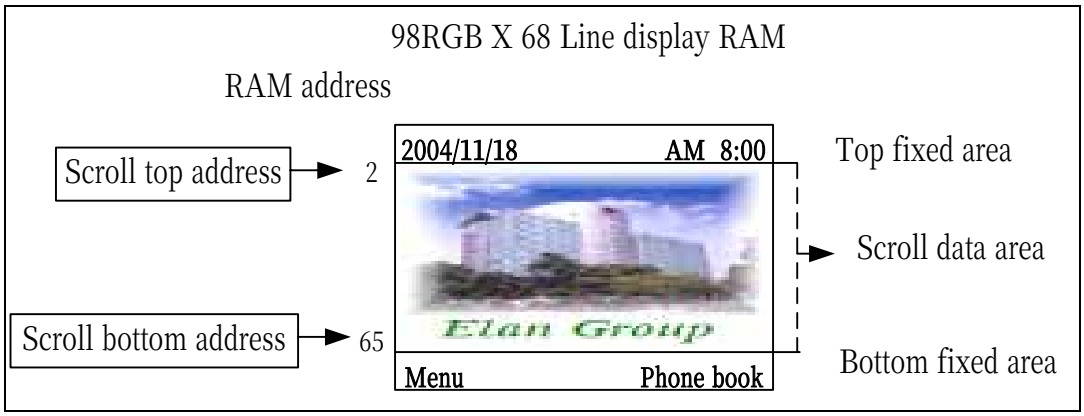
```
--------------- scroll function setting ------------------
WRITE 0xF3     //Bank 3
WRITE 0x10     //Scroll top address (up nibble)
WRITE 0x02     //Scroll top address (low nibble)
WRITE 0x34     //Scroll bottom address (up nibble)
WRITE 0x21     //Scroll bottom address (low nibble)
WRITE 0x54     //Scroll specified address (up nibble)
WRITE 0x41     //Scroll specified address (low nibble)
WRITE 0x80     //Center scroll mode
-------------------- scroll start ------------------
MOV  A, #2
MOV  INDEX1, A
LOOP1:
  WRITE (0x70)
  WRITE (0x60 + INDEX1)
INC_INDEX_1:
  INC  INDEX1
  MOV  A, INDEX1
  JLE  A, #15, LOOP1
  MOV  A, #1
  MOV  INDEX2, A
LOOP2:
  MOV  A, #0
  MOV  INDEX1, A
LOOP3:
  WRITE (0x70 + INDEX2)
  WRITE (0x60 + INDEX1)
INC_INDEX_2:
  INC  INDEX1
  MOV  A, INDEX1
```

```
  JLE  A, #15, LOOP3
  INC  INDEX2
  MOV  A, INDEX2
  JLE  A, #3, LOOP2
  MOV  A, #0
  MOV  INDEX1, A
LOOP4:
  WRITE (0x77)
  WRITE (0x60 + INDEX1)
INC_INDEX_3:
  INC  INDEX1
  MOV  A, INDEX1
  JLE  A, #13, LOOP4
```

NOTE

Set the scroll top address and scroll bottom address to define the area of scrolling data in RAM.

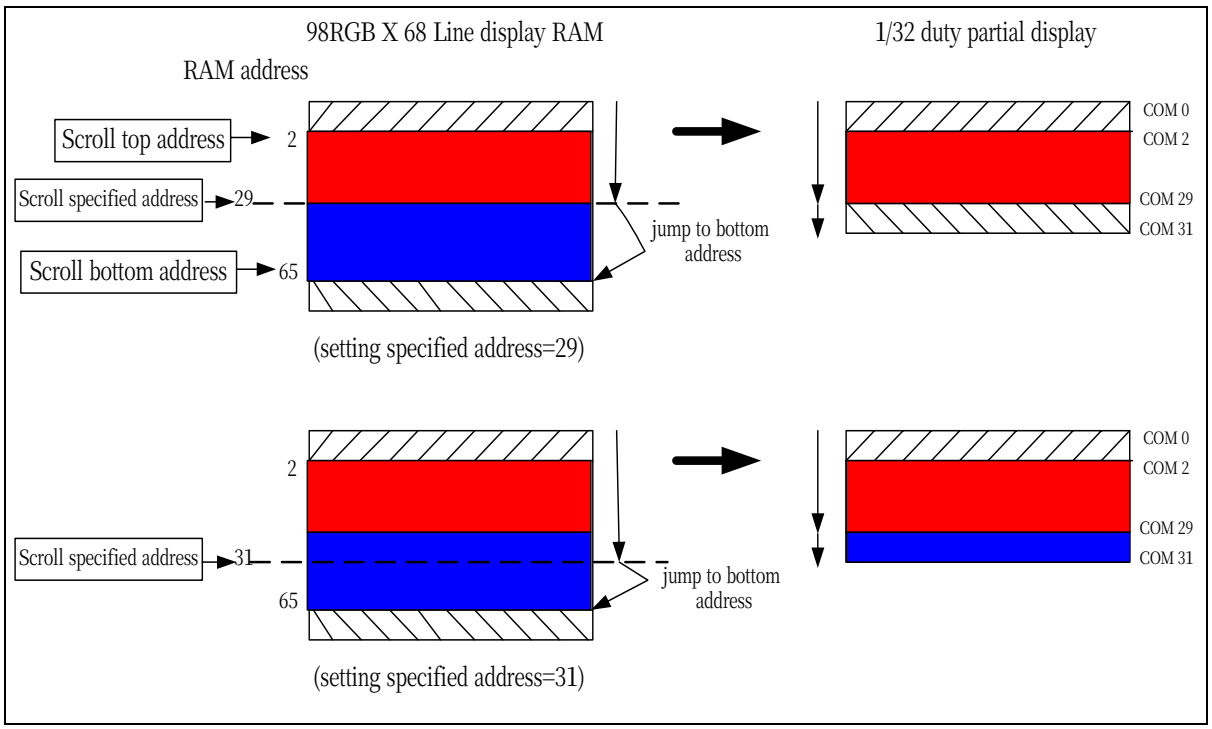
Example



NOTE

Set the scroll specified address according to panel size and duty selection, to define the address where to jump or to scroll bottom address. Then display the bottom fixed data area. Remark: Scroll specified address = scroll top address + panel scroll area – 1

Ex: (98RGB x 68 Line panel; 1/32 duty, partial display)



Attention: If the scroll specified address is not set or wrongly set, unpredictable scrolling results may occur.

NOTE

Set the scroll top address, scroll bottom address, scroll specified address, and scroll start address carefully when using scroll function. In case of error, follow the rules shown below:

※Scroll top address <= Scroll bottom address

※Scroll specified address = Scroll top address + panel scroll area – 1

※Scroll top address <= Scroll start address <= Scroll bottom address

7.23 Initialization

Setting RESB pin to “L” initializes the EM65570S. Normally, RESB pin is initialized together with MPU by connecting to the reset pin of MPU. When power ON, be sure to make RESB=”L”.

65K color mode

Item	Initial Value
Display RAM	Not fixed
X Address	00H set
Y Address	00H set
Display starting common	Set at the first common (0H)
Display ON/OFF	Display OFF
Display Normal/Reverse	Normal
n-line alternated	Every frame unit
(BF1,BF0)	(0, 1)
Common shift direction	COM0 → COM67
Increment mode	Increment OFF
Data SWAP Mode	OFF
Register in electronic volume	(0, 0, 0, 0, 0, 0, 0)
Power Supply	OFF
Display mode	65K color mode
Gradation LSB	0
RAM access data length	8-bit mode
Discharge Register	0

7.24 Precaution when Setting Power ON and Power OFF

High current may flow if a voltage is supplied to the LCD driver power supply while the system power supply is floating and may permanently damage this LSI. The detailed description is as follows.

7.24.1 When Using the Built-in Power Supply

Procedure in Setting the Power ON

Logic system (VDD) power ON

Booster circuit system (VEE) power ON

Reset the operation, booster and voltage conversion circuit enable.

If VDD and VEE voltages aren’t same potential, power on logic system (VDD) first.

Procedure in Setting the Power OFF

Set the HALT register to “1” or make reset operation.

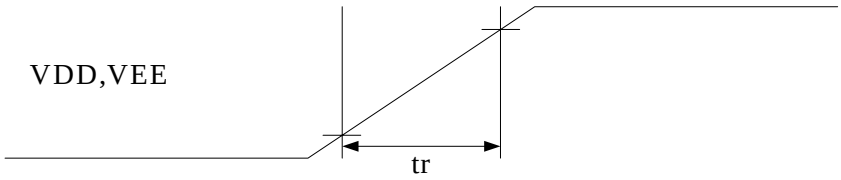
Set the Booster circuit system (VEE) power OFF.

Set the Logic system (VDD) power OFF.

If VDD and VEE are not of the same potential, cut off VEE first. After VEE, VOUT, V0, V1, V2, V3 and V4 voltages are below LCD ON voltage (threshold voltage for Liquid crystal turn on), power off logic system (VDD).

7.24.2 Power Supply Rising Time

Though usually there is no constraint on the rising time of the power supply, the following tr (rising time) is recommended in this practical use.

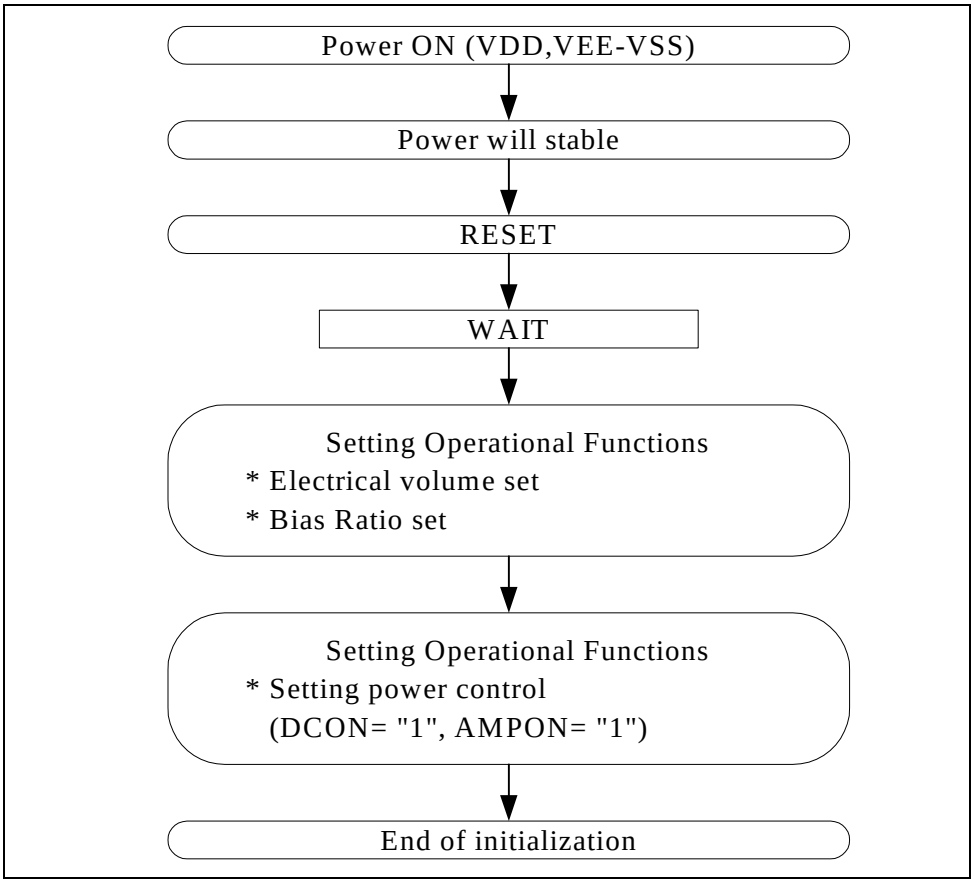


Item	Recommended Rising Time	Applicable Power
tr	30 µs ~10 ms	VDD, VEE

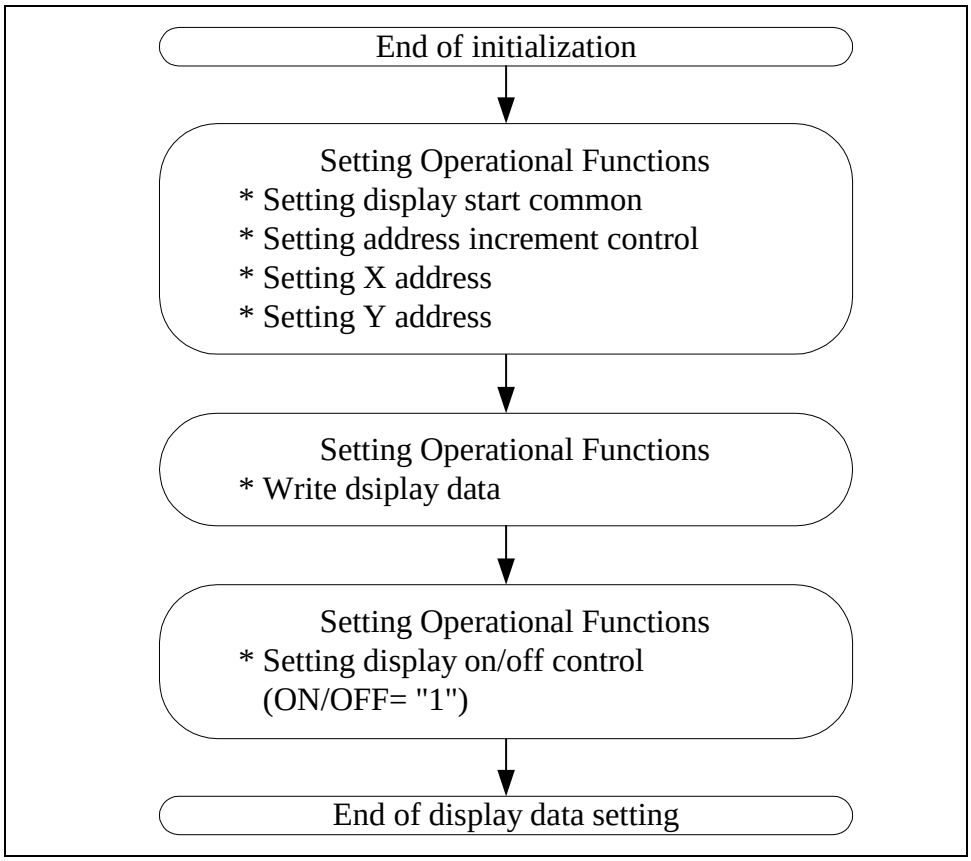
Note: The rising time is initially from 10% of VDD, VEE to 90%

7.25 Example of Registers Setting

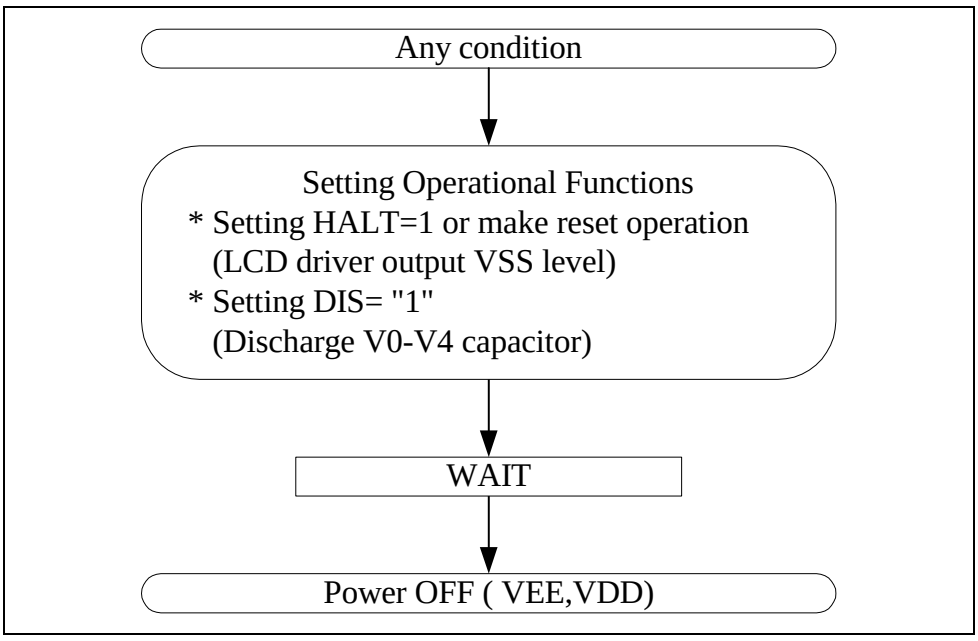
7.25.1 Initialization



7.25.2 Display Data



7.25.3 Power OFF



8 Control Registers

8.1 Control Register

Control Register Table (Bank 0)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
X Address (Lower nibble) [0H]	0	1	0	1	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
X Address (Upper nibble) [1H]	0	1	0	1	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Set of X direction Address in display RAM
Y Address (Lower nibble) [2H]	0	1	0	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Set of Y direction Address in display RAM
Y Address (Upper nibble) [3H]	0	1	0	1	0	0	0	0	0	1	1	AY7	AY6	AY5	AY4	Set of Y direction Address in display RAM
Reserved [4H]	0	1	0	1	0	0	0	0	1	0	0	*	*	*	*	Reserved
Reserved [5H]	0	1	0	1	0	0	0	0	1	0	1	*	*	*	*	Reserved
n-line alternation (Lower nibble) [6H]	0	1	0	1	0	0	0	0	1	1	0	N3	N2	N1	N0	Set the number of alternated reverse line
n-line alternation (Upper nibble) [7H]	0	1	0	1	0	0	0	0	1	1	1	N7	N6	N5	N4	Set the number of alternated reverse line
Display control (1) [8H]	0	1	0	1	0	0	0	1	0	0	0	SHIFT	65K	ALLON	ON/OFF	SHIFT: Select common shift direction 65K: Select 65K gradation ALLON: All display ON ON/OFF: Display ON or OFF
Display control (2) [9H]	0	1	0	1	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Display normal/reverse NLIN: n line reverse control SWAP: Display data swapping
Increment control [AH]	0	1	0	1	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Select window. AIM: Select increment mode AYI: Y increment, AXI: X increment
Power control [BH]	0	1	0	1	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: Internal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting
LCD Duty Ratio [CH]	0	1	0	1	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Set LCD drive duty ratio
Booster [DH]	0	1	0	1	0	0	0	1	1	0	1	SHP	VU2	VU1	VU0	Set number of boosting step for booster circuit
Bias ratio control [EH]	0	1	0	1	0	0	0	1	1	1	0	B3	B2	B1	B0	Set bias ratio for LCD driving voltage
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

NOTE

The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 1)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Graphic start X address (Lower nibble) [0H]	0	1	0	1	0	0	1	0	0	0	0	GSX3	GSX2	GSX1	GSX0	Set graphic function X start addres
Graphic start X address (Upper nibble) [1H]	0	1	0	1	0	0	1	0	0	0	1	*	GSX6	GSX5	GSX4	Set graphic function X start addres
Graphic end X address (Lower nibble) [2H]	0	1	0	1	0	0	1	0	0	1	0	GEX3	GEX2	GEX1	GEX0	Set graphic function X end address
Graphic end X address (Upper nibble) [3H]	0	1	0	1	0	0	1	0	0	1	1	*	GEX6	GEX5	GEX4	Set graphic function X end address
Graphic start Y address (Lower nibble) [4H]	0	1	0	1	0	0	1	0	1	0	0	GSY3	GSY2	GSY1	GSY0	Set graphic function Y start addres
Graphic start Y address (Upper nibble) [5H]	0	1	0	1	0	0	1	0	1	0	1	GSY7	GSY6	GSY5	GSY4	Set graphic function Y start addres
Graphic end Y address (Lower nibble) [6H]	0	1	0	1	0	0	1	0	1	1	0	GEY3	GEY2	GEY1	GEY0	Set graphic function Y end address
Graphic end Y address (Upper nibble) [7H]	0	1	0	1	0	0	1	0	1	1	1	GEY7	GEY6	GEY5	GEY4	Set graphic function Y end address
Draw rectangle control [8H]	0	1	0	1	0	0	1	1	0	0	0	*	*	FILL	RECT	Fill color enable Draw rectangle enable
Line color R (Lower nibble) [9H]	0	1	0	1	0	0	1	1	0	0	1	LR3	LR2	LR1	LR0	Set line color R of rectangle
Line color R (Upper nibble) [AH]	0	1	0	1	0	0	1	1	0	1	0	*	*	*	LR4	Set line color R of rectangle
Line color G (Lower nibble) [BH]	0	1	0	1	0	0	1	1	0	1	1	LG3	LG2	LG1	LG0	Set line color G of rectangle
Line color G (Upper nibble) [CH]	0	1	0	1	0	0	1	1	1	0	0	*	*	LG5	LG4	Set line color G of rectangle
Line color B (Lower nibble) [DH]	0	1	0	1	0	0	1	1	1	0	1	LB3	LB2	LB1	LB0	Set line color B of rectangle
Line color B (Upper nibble) [EH]	0	1	0	1	0	0	1	1	1	1	0	*	*	*	LB4	Set line color B of rectangle
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0:for LS1 test,must set to "0" RE:set register bank number

NOTE

The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 2)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSE	RS	WRE	RDE	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Fill color R (Lower nibble) [0H]	0	1	0	1	0	1	0	0	0	0	0	FR3	FR2	FR1	FR0	Set fill color R of rectangle
Fill color R (Upper nibble) [1H]	0	1	0	1	0	1	0	0	0	0	1	*	*	*	FR4	Set fill color R of rectangle
Fill color G (Lower nibble) [2H]	0	1	0	1	0	1	0	0	0	1	0	FG3	FG2	FG1	FG0	Set fill color G of rectangle
Fill color G (Upper nibble) [3H]	0	1	0	1	0	1	0	0	0	1	1	*	*	FG5	FG4	Set fill color G of rectangle
Fill color B (Lower nibble) [4H]	0	1	0	1	0	1	0	0	1	0	0	FB3	FB2	FB1	FB0	Set fill color B of rectangle
Fill color B (Upper nibble) [5H]	0	1	0	1	0	1	0	0	1	0	1	*	*	*	FB4	Set fill color B of rectangle
Dim&Copy&Clear function control [6H]	0	1	0	1	0	1	0	0	1	1	0	CLR	COPY	DBW	DIM	Dim & Copy & Clear function control
Copy destination X address (Lower nibble) [7H]	0	1	0	1	0	1	0	0	1	1	1	CDX3	CDX2	CDX1	CDX0	Set destination X address of copy function
Copy destination X address (Upper nibble) [8H]	0	1	0	1	0	1	0	1	0	0	0	*	CDX6	CDX5	CDX4	Set destination X address of copy function
Copy destination Y address (Lower nibble) [9H]	0	1	0	1	0	1	0	1	0	0	1	CDY3	CDY2	CDY1	CDY0	Set destination Y address of copy function
Copy destination Y address (Upper nibble) [AH]	0	1	0	1	0	1	0	1	0	1	0	CDY7	CDY6	CDY5	CDY4	Set destination Y address of copy function
Reserved [BH]	0	1	0	1	0	1	0	1	0	1	1	*	*	*	*	Reserved
Reserved [CH]	0	1	0	1	0	1	0	1	1	0	0	*	*	*	*	Reserved
Reserved [DH]	0	1	0	1	0	1	0	1	1	0	1	*	*	*	*	Reserved
Reserved [EH]	0	1	0	1	0	1	0	1	1	1	0	*	*	*	*	Reserved
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0:for LS1 test,must set to "0" RE:set register bank number

NOTE

The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 3)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Scroll top address (Lower nibble) [0H]	0	1	0	1	0	1	1	0	0	0	0	STA3	STA2	STA1	STA0	Set scroll top address
Scroll top address (Upper nibble) [1H]	0	1	0	1	0	1	1	0	0	0	1	STA7	STA6	STA5	STA4	Set scroll top address
Scroll bottom address (Lower nibble) [2H]	0	1	0	1	0	1	1	0	0	1	0	SBA3	SBA2	SBA1	SBA0	Set scroll bottom address
Scroll bottom address (Upper nibble) [3H]	0	1	0	1	0	1	1	0	0	1	1	SBA7	SBA6	SBA5	SBA4	Set scroll bottom address
Scroll specified address (Lower nibble) [4H]	0	1	0	1	0	1	1	0	1	0	0	SSA3	SSA2	SSA1	SSA0	Set scroll specified address
Scroll specified address (Upper nibble) [5H]	0	1	0	1	0	1	1	0	1	0	1	SSA7	SSA6	SSA5	SSA4	Set scroll specified address
Scroll start address (Lower nibble) [6H]	0	1	0	1	0	1	1	0	1	1	0	SAY3	SAY2	SAY1	SAY0	Set scroll start address
Scroll start address (Upper nibble) [7H]	0	1	0	1	0	1	1	0	1	1	1	SAY7	SAY6	SAY5	SAY4	Set scroll start address
Scroll mode select [8H]	0	1	0	1	0	1	1	1	0	0	0	*	*	SM1	SM0	Scroll mode select
Reserved [9H]	0	1	0	1	0	1	1	1	0	0	1	*	*	*	*	Reserved
Reserved [AH]	0	1	0	1	0	1	1	1	0	1	0	*	*	*	*	Reserved
Reserved [BH]	0	1	0	1	0	1	1	1	0	1	1	*	*	*	*	Reserved
Reserved [CH]	0	1	0	1	0	1	1	1	1	0	0	*	*	*	*	Reserved
Reserved [DH]	0	1	0	1	0	1	1	1	1	0	1	*	*	*	*	Reserved
Reserved [EH]	0	1	0	1	0	1	1	1	1	1	0	*	*	*	*	Reserved
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0:for LS1 test,must set to "0" RE:set register bank number

NOTE

The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 4)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Reserved [0H]	0	1	0	1	1	0	0	0	0	0	0	*	*	*	*	Reserved
Reserved [1H]	0	1	0	1	1	0	0	0	0	0	1	*	*	*	*	Reserved
Reserved [2H]	0	1	0	1	1	0	0	0	0	1	0	*	*	*	*	Reserved
RAM data writing select Control [3H]	0	1	0	1	1	0	0	0	0	1	1	WBS	RD WS2	RD WS1	RD WS0	Set RAM data writing mode
Reserved [4H]	0	1	0	1	1	0	0	0	1	0	0	*	*	*	*	Reserved *
Reserved [5H]	0	1	0	1	1	0	0	0	1	0	1	*	*	*	*	Reserved
Display start common [6H]	0	1	0	1	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Set Common Driver Start Line
Temperature Compensation [7H]	0	1	0	1	1	0	0	0	1	1	1	*	*	TCS1	TCS0	Temperature Compensation set
Display Select Control [8H]	0	1	0	1	1	0	0	1	0	0	0	*	GLSB	*	*	Set Gradation LSB bit of 256 color mode
RAM Data length set [9H]	0	1	0	1	1	0	0	1	0	0	1	C256	HSW	ABS	WLS	Set data length on RAM access 8-bit access or 16-bit access
Electronic Volume (Lower nibble) [AH]	0	1	0	1	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Set electronic volume register
Electronic Volume (Upper nibble) [BH]	0	1	0	1	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Set electronic volume register
Register read control [CH]	0	1	0	1	1	0	0	1	1	0	0	RA3	RA2	RA1	RA0	Set register address for read
Select RF [DH]	0	1	0	1	1	0	0	1	1	0	1	RF3	RF2	RF1	RF0	Select RF ratio of OSC circuit
Booster Frequency control [EH]	0	1	0	1	1	0	0	1	1	1	0	BF1	BF0	HPM	DIS	Set booster frequnecy Discharge capacitances of V0~V4
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0:for LS1 test,must set to "0" RE:set register bank number

NOTE

The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 5)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Window X End Address (Lower nibble) [0H]	0	1	0	1	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Set X end address for window function
Window X End Address (Upper nibble) [1H]	0	1	0	1	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Set X end address for window function
Window Y End Address (Lower nibble) [2H]	0	1	0	1	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Set Y end address for window function
Window Y End Address (Upper nibble) [3H]	0	1	0	1	1	0	1	0	0	1	1	EY7	EY6	EY5	EY4	Set Y end address for window function
Start address for line reverse (Lower nibble) [4H]	0	1	0	1	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	set start line for line reverse display
Start address for line reverse (Upper nibble) [5H]	0	1	0	1	1	0	1	0	1	0	1	LS7	LS6	LS5	LS4	set start line for line reverse display
End address for line reverse (Lower nibble) [6H]	0	1	0	1	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	set end line for line reverse display
End address for line reverse (Upper nibble) [7H]	0	1	0	1	1	0	1	0	1	1	1	LE7	LE6	LE5	LE4	set end line for line reverse display
Line reverse control Burst RAM write control [8H]	0	1	0	1	1	0	1	1	0	0	0	EOR	BST	BT	LREV	set line reverse control, burst RAM write control
Regulator multiple ratio control register [9H]	0	1	0	1	1	0	1	1	0	0	1	RM3	RM2	RM1	RM0	set regulator multiple ratio
OTP mode select [AH]	0	1	0	1	1	0	1	1	0	1	0	M1	M0	— *	*	EEPROM mode select
Vop calibration offset (Lower nibble) [BH]	0	1	0	1	1	0	1	1	0	1	1	CV3	CV2	CV1	CV0	Vop calibration offset select
Reserved [CH]	0	1	0	1	1	0	1	1	1	0	0	*	*	*	*	Reserved
Reserved [DH]	0	1	0	1	1	0	1	1	1	0	1	*	*	*	*	Reserved
Vop calibration offset (Upper nibble) [EH]	0	1	0	1	1	0	1	1	1	1	0	*	*	CV5	CV4	Vop calibration offset select
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0:for LS1 test,must set to "0" RE:set register bank number

NOTE

The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

8.2 Control Registers Functions

The EM65570S has many control registers. In case of control register access, upper nibble of data bus (D7~D4) represent register address, lower nibble of data bus (D3~D0) represent data. The access example is shown in the following. The Pins (CSB, RS, RDB, WRB) setting is for 80-family MPU interface. Only the setting of terminal (RDB, WRB) is different, when it is accessed by the 68-fanily MPU.

(Example) X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

Register address | Data

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Pins setting | Register Bank

In the writing to the control register, it is used directly as addressing D7~D4 of the data bus. In case of register read, first set RA register for specific register address, next can read specific register. Therefore, it is need 2-step for register read. Then, specific register output to D3~D0 of data bus. Except D3~D0 of data bus are all “H”. Prohibit access to undefined register address area. When RS is “L”, all read/write operations are accessed to display RAM. Then data bus doesn’t include register address. In case of write, D3~D0 data is written to the register designated at D7~D4 in rising edge of the WRB signal. In case of read, register can output to data bus is RDB active period. Control register and display RAM are the equal access timing.

8.2.1 X Address Register (AX)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX3, AX2, AX1, AX0}= 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AX7	AX6	AX5	AX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX7, AX6, AX5, AX4}= 0H, read address: 1H)

The AX register set to X-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 4-bit respectively. 00H to 61H are applicable to the values for AX7 to AX0, and 62H to FFH are not permitted.

8.2.2 Y Address Register (AY)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	AY3	AY2	AY1	AY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AY3, AY2, AY1, AY0}=0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	AY7	AY6	AY5	AY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AY7, AY6, AY5, AY4}=0H, read address: 3H)

※ Mark shows “Don’t care”

The AY register set to Y-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 4-bit respectively. 00H to 43H are applicable to the values for AY7 to AY0, and 44H to FFH are not permitted.

8.2.3 n Line Alternate Register (N)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	N3	N2	N1	N0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {N3, N2, N1, N0}=0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	N7	N6	N5	N4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {N7, N6, N5, N4}=0H, read address: 7H)

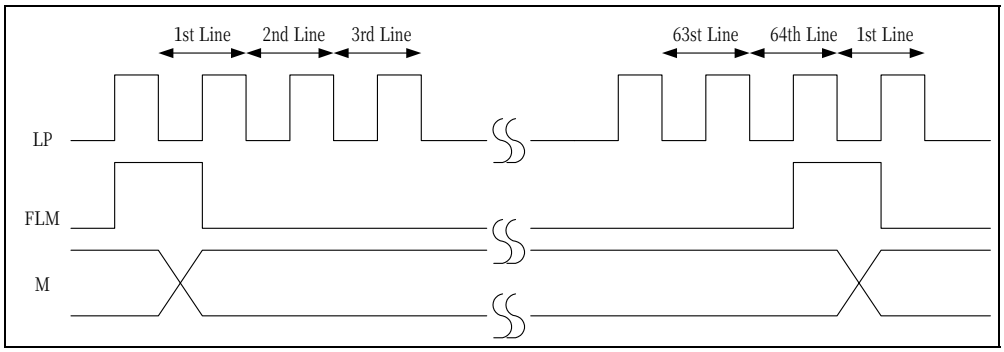
※ Mark shows “Don’t care”

The reverse line number of LCD alternated drive is required to set in the register. The line number has a limit, must keeps between from 2 to 67 lines. The values set up by the alternated register become enable when NLIN control bit is “1”. When NLIN control bit is “0”, alternated drive waveform reverses by each frame is generated.

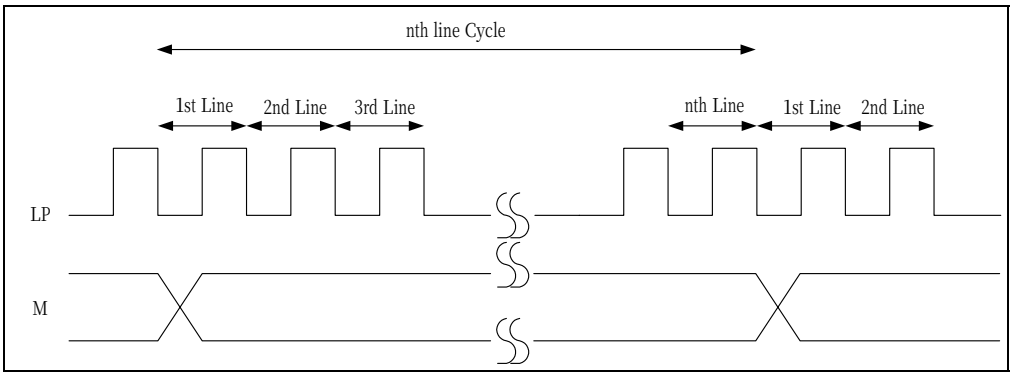
N7	N6	N5	N4	N3	N2	N1	N0	Line Address
0	0	0	0	0	0	0	0	Inhibit to use
0	0	0	0	0	0	0	1	2
…								…
0	1	0	0	0	0	1	0	67

Alternate Timing

NLIN=”0” (in case of 1/64 DUTY Display)



NLIN=”1”



8.2.4 Display Control (1) Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SHIFT	65K	ALL ON	ON/ OFF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {SHIFT, 65K, ALLON, ON/OFF}=4H, read address: 8H)

ALLON

Regardless of the data for display, all is on.

This control has priority over display normal/reverse commands.

ALLON = “0”: Normal display

ALLON = “1”: All display lighted

65K

Select 65K gradation display

65K=”0”: 4096 or 256 gradation display, decided by C256 control bit.

65K=”1”: 65K gradation display mode.

SHIFT

The shift direction of display scanning data in the common driver output is selected.

SHIFT = “0”: COM0 → COM67 shift-scan

SHIFT = “1”: COM67 → COM0 shift-scan

ON/OFF

This register controls whether to turning on the LCD panel or not.

ON/OFF =”0”: Display OFF

ON/OFF =”1”: Display ON

8.2.5 Display Control (2) Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	REV	NLIN	SWAP	REF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {REV, NLIN, SWAP, REF}=0H, read address: 9H)

REV

Corresponding to the data of display RAM, the lighting or not-lighting of the display is set up.

REV =”0”: When RAM data at “H”, LCD at ON voltage (normal)

REV =”1”: When RAM data at “L”, LCD at ON voltage (reverse)

NLIN

The NLIN control n-line alternated drive.

NLIN = “0”: n-line alternated drive OFF. In each frame, the alternated signals (M) are reversed.

NLIN =”1”: n-line alternated drive ON. According to data set up in n-line alternated register, the alternation is made.

REF, SWAP

The REF control the reverse of display or not

REF=”0” : Normal mode.

REF=’”1”: Reverse of display, Exchange display data of R and B

The SWAP control the display data of R and B exchange or not.

SWAP = “0”: Normal mode. SWAP = “1”: Exchange display data of R and B.

REF	SWAP	Effect on the Panel
0	0	Normal display
0	1	Exchange display data of R and B.
1	0	Reverse display, Exchange display data of R and B
1	1	Reverse display

8.2.6 Increment Control Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	WIN	AIM	AYI	AXI

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {WIN, AIM, AYI, AXI}=0H, read address: AH)

This register controls the increment mode and window function when accessing to display RAM. The increment operation of AX and AY register can control by AIM, AYI and AXI registers setting and every write access or every read access to display RAM. The AY register directly connects to display RAM as Y address. The AX register connect to address converter, and that output to display RAM as X address in the auto increment mode, AX and AY register are increment, not directly increment X and Y address.

In setting to this control register, the increment operation of address can be made without setting successive addresses for writing data or for reading data to display RAM from MPU.

The WIN register used for window function control.

WIN=”0”: Normal RAM access

WIN=”1”: Window function access

In case of using window function access, should be set following register before access to RAM.

WIN=”1”, AXI=”1”, AYI=”1”

X Address, Y Address, Window X End Address, Window Y End Address

Moreover, should be keep following address condition.

Window end X address $\geqq$ Window start X address

Window end Y address $\geqq$ Window start Y address

The increment control of X and Y addresses by AIM, AYI and AXI registers are as follows.

AIM	Address Increment Timing
0	When writing to Display RAM or reading from Display RAM This is effective when access to successive address area
1	Only when writing to Display RAM This is effective the case of “Read Modify Write

AYI	AXI	Select Address Increment Operation	Remark
0	0	Address is not increment	(1)
0	1	X-Address is increment	(2)
1	0	Y-Address is increment	(3)
1	1	X and Y both are increment	(4)

(1) Regardless of AIM, no increment for AX and AY register.

(2) According to the setting-up of AIM, automatically change X address.

Transition of AX Register	Transition of X Address
00H→ 01H→.....→ max	Same as AX register

NOTE
maxH: The internal maximum X-address in each access mode.

(3) According to the setting-up of AIM, automatically change Y address.

Transition of AY Register	Transition of Y Address
00H→01H →.....→ max	Same as AY register

(4) According to the setting-up of AIM, cooperative change X and Y address. When the X address exceed maxH, Y address increment occurs.

Transition of AX and AY Register	Transition of X and Y Address
AX: 00H → 00H → – – → max AY: When each AX exceed maxH, increment AY 00H → 00H → – – → max	Same as AX and AY register

NOTE
maxH: The internal maximum X-address in each access mode.

Following shows address increment in window function access.

Transition of AX and AY Register	Transition of X and Y Address
AX: START Address → START Address+1 → – – → END Address AY: When each AX exceed AE, increment AY START Address → START Address+1 → – – → END Address	Same as AX and AY register

NOTE

maxH: The internal maximum X-address in each access mode.

In each operation mode, the following increment operation is performed:

When gradation display mode and 8-bit access are selected

Address is incremented as described above.

When gradation display mode and 16-bit access are selected:

Accessing the RAM once accesses two bytes.

The X-addresses increment in the order of 00H,01H,…5FH,60H and 61H.

8.2.7 Power Control Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	AMPON	HALT	DCON	ACL

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {AMPON, HALT, DCON, ACL}=0H, read address: BH)

ACL

The internal circuit can be initialized.

ACL = “0”: Normal operation

ACL = “1”: Initialization ON

When the reset operation begins internally after ACL register sets to “1”, the ACL register is automatically cleared to “0”. The internal reset signal has been generated with a clock (built-in oscillation circuit or CK input) for the display. Therefore, install the WAIT period for the display clock two cycles at least. After WAIT period, next operation can handle.

DCON

The internal booster circuit is set ON/OFF

DCON = “0”: Booster circuit OFF

DCON=”1”: Booster circuit ON

HALT

The conditions of power saving are set ON/OFF by this command.

HALT = “0”: Normal operation

HALT=”1”: Power-saving operation

When setting in the power-saving state, the consumed current can be reduced to a value near to the standby current.

The internal condition at power saving are as follows.

The oscillating circuit and power supply circuit are stopped.

The LCD drive is stopped, and output of the segment driver and common driver are VSS level.

The clock input from CK pin is inhibited.

The contents of Display RAM data are maintained.

The operational mode maintains the state of command execution before executing power saving command.

AMPON

The internal OP-AMP circuit block (voltage regulator, electronic volume, and voltage conversion circuit) is set ON/OFF by this command.

AMPON = “0”: The internal OP-AMP circuit OFF

AMPON = ”1”: The internal OP-AMP circuit ON

8.2.8 LCD Duty (DS)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	DS3	DS2	DS1	DS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {DS3, DS2, DS1, DS0}=CH, read address: CH)

※ mark means “Don’t care”

The DS register set to LCD display duty.

DS3	DS2	DS1	DS0	Display width and Duty
0	0	0	0	1/8 duty
0	0	0	1	1/16 duty
0	0	1	0	1/24 duty
0	0	1	1	1/32 duty
0	1	0	0	1/48 duty
0	1	0	1	1/64 duty
0	1	1	0	1/72 duty
1	1	0	0	Reserved

Partial display can be made possible by setting an arbitrary duty ratio.

8.2.9 Booster Setup (VU)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	SHP	VU2	VU1	VU0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {SHP, VU2, VU1, VU0}=5H, read address: DH)

※ mark means “Don’t care”

The booster steps set to VU register

.VU2	VU1	VU0	Booster Operation
0	0	0	Booster disable (No operation)
0	0	1	2 times voltage output
0	1	0	3 times voltage output
0	1	1	4 times voltage output
1	0	0	5 times voltage output
1	0	1	Reserved

8.2.10 Bias Setting Register (B)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	B3	B2	B1	B0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {B3, B2, B1, B0}=8H, read address: EH)

※ mark means “Don’t care”

This register is used to set a bias ratio. A bias ratio can be selected from 1/5 to 1/9 by setting B3, B2, B1, and B0.

B3	B2	B1	B0	Bias
0	0	0	0	1/5 Bias
0	0	0	1	1/6 Bias
0	0	1	0	1/7 Bias
0	0	1	1	1/8 Bias
0	1	0	0	1/9 Bias
1	0	0	0	Reserved

8.2.11 Register Access Control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	TST0	RE2	RE1	RE0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

(At the time of reset: {TST0, RE2, RE1, RE0}=0H, read address: FH)

※ mark means “Don’t care”

The RE register set to number of register bank. Access to each control register, set RE register at first.

The TST0 register use for test of LSI, Therefore this register must be set to “0”

8.2.12 Graphic Start X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	GSX3	GSX2	GSX1	GSX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GSX3, GSX2, GSX1, GSX0} = 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	GSX6	GSX5	GSX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GSX6, GSX5, GSX4} = 0H, read address: 1H)

※ mark means “Don’t care”

Set X start address of the rectangle. 0 <= X <= 97 ; Graphic start X address <= Graphic end X address

8.2.13 Graphic End X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	GEX3	GEX2	GEX1	GEX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GEX3, GEX2, GEX1, GEX0} = 0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	GEX6	GEX5	GEX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GEX6, GEX5, GEX4} = 0H, read address: 3H)

※ mark means “Don’t care”

Set X end address of the rectangle. 0 <= X <= 97 ; Graphic start X address <= Graphic end X address

8.2.14 Graphic Start Y Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	GSY3	GSY2	GSY1	GSY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GSY3, GSY2, GSY1, GSY0} = 0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	GSY7	GSY6	GSY5	GSY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GSY7, GSY6, GSY5, GSY4} = 0H, read address: 5H)

※ mark means “Don’t care”

Set Y start address of rectangle. 0 <= Y <= 67 ; Graphic start Y address <= Graphic end Y address

8.2.15 Graphic End Y Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	GEY3	GEY2	GEY1	GEY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GEY3, GEY2, GEY1, GEY0} = 0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	GEY7	GEY6	GEY5	GEY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {GEY7, GEY6, GEY5, GEY4} = 0H, read address: 7H)

※ ,ark means “Don’t care”

Set Y end address of rectangle. 0 <= Y <= 67 ; Graphic start Y address <= Graphic end Y address

8.2.16 Draw Rectangle Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	*	FILL	RECT

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {FILL, RECT} = 0H, read address: 8H)

※ mark means “Don’t care”

The FILL bit control filling color in the interior of rectangle enable or disable.

FILL=”0”, fill function disable.

FILL=”1”, fill function enable.

The RECT bit control drawing rectangle enable or disable.

RECT=”0”, draw rectangle disable.

RECT=”1”, draw rectangle enable.

FILL	RECT	Condition
0	0	Initial value
0	1	Draw rectangle but not fill color
1	0	Inhibited for use
1	1	Draw rectangle and fill color

NOTE

When RECT=1, hardware starts the drawing operation, and when finished Drawing operation, RECT will be cleared to ‘0’ automatically by hardware.

8.2.17 Line Color R

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	LR3	LR2	LR1	LR0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {LR3, LR2, LR1, LR0} = 0H, read address: 9H)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	LR4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {LR4} = 0H, read address: AH)

※ mark means “Don’t care”

Set line color R of rectangle.

NOTE

When in 256 color mode, LR3 don’t care ; when 4k or 256 color mode, LR4 don’t care

8.2.18 Line Color G

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	LG3	LG2	LG1	LG0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {LG3, LG2, LG1, LG0} = 0H, read address: BH)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	*	*	LG5	LG4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {LG5,LG4} = 0H, read address: CH)

※ mark means “Don’t care”

Set line color G of the rectangle.

NOTE

When 256 color mode, LG3 don’t care ; when 4k or 256 color mode, LG5 and LG4 don’t care

8.2.19 Line Color B

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	LB3	LB2	LB1	LB0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {LB3, LB2, LB1, LB0} = 0H, read address: DH)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	*	*	*	LB4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {LB4} = 0H, read address: EH)

※ mark means “Don’t care”

Set line color B of rectangle.

NOTE

When in 256 color mode, LB3 and LB2 don't care ; when 4k or 256 color mode, LB4 don't care

8.2.20 Fill Color R

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FR3	FR2	FR1	FR0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {FR3, FR2, FR1, FR0} = 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	*	FR4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {FR4} = 0H, read address: 1H)

※ mark means "Don't care"

Set fill color R of rectangle.

NOTE

When in 256 color mode, FR3 don't care ; when 4k or 256 color mode, FR4 don't care

8.2.21 Fill Color G

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	FG3	FG2	FG1	FG0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {FG3, FG2, FG1, FG0} = 0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	FG5	FG4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {FG5, FG4} = 0H, read address: 3H)

※ mark means "Don't care"

Set fill color G of rectangle.

NOTE

When in 256 color mode, FG3 don't care ; when 4k or 256 color mode, FG4 and FG5 don't care

8.2.22 Fill Color B

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	FB3	FB2	FB1	FB0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {FB3, FB2, FB1, FB0} = 0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	FB4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {FB4} = 0H, read address: 5H)

※ mark means “Don’t care”

Set fill color B of rectangle.

NOTE

When in 256 color mode, FB2 and FB3 don’t care ; when 4k or 256 color mode, FB4 don’t care

8.2.23 Dim, Copy & Clear Functions Control

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	CLR	COPY	DBW	DIM

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {CLR, COPY, DBW, DIM} = 0H, read address: 6H)

※ mark means “Don’t care”

Clear function will clear the RAM data to ‘0’ enclosed by rectangle area. The CLR bit control clear function enable or disable.

CLR=”0”, clear function disable.

CLR=”1”, clear function enable.

Copy function will copy the specified rectangle to another destination. The COPY bit control copy function enable or disable.

COPY=”0”, copy function disable.

COPY=”1”, copy function enable.

Dim function will dim the rectangle area to 50% black or 50% white. The DIM bit controls the dim function enable or disable. The DBW bit select dimming to 50% black or 50% white.

DIM=”0”, dim function disable.

DIM=”1”, dim function enable.

DBW=”0”, dim to 50% black.

DBW=”1”, dim to 50% white.

8.2.24 Copy Destination X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	CDX3	CDX2	CDX1	CDX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {CDX3, CDX2, CDX1, CDX0} = 0H, read address: 7H)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	CDX6	CDX5	CDX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {CDX6, CDX5, CDX4} = 0H, read address: 8H)

※ mark means “Don’t care”

Set destination X address of copying rectangle. 0<= X <= 97

8.2.25 Copy Destination Y Address

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	CDY3	CDY2	CDY1	CDY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {CDY3, CDY2, CDY1, CDY0} = 0H, read address: 9H)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	CDY7	CDY6	CDY5	CDY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {CDY7, CDY6, CDY5, CDY4} = 0H, read address: AH)

※ mark means “Don’t care”

Set destination Y address of copying rectangle. 0<= Y <= 67

8.2.26 Scroll Top Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	STA3	STA2	STA1	STA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {STA3, STA2, STA1, STA0} = 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	STA7	STA6	STA5	STA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {STA7, STA6, STA5, STA4} = 0H, read address: 1H)

※ mark means “Don’t care”

Set top address of scroll data area in RAM. 0 <= Scroll top address <= 67 ; Scroll top address must < Scroll bottom address

8.2.27 Scroll Bottom Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	SBA3	SBA2	SBA1	SBA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {SBA3, SBA2, SBA1, SBA0} = FH, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	SBA7	SBA6	SBA5	SBA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {SBA7, SBA6, SBA5, SBA4} = 9H, read address: 3H)

※ mark means “Don’t care”

Set bottom address of scroll data area in RAM. 0 <= Scroll bottom address <= 67 ; Scroll top address must < Scroll bottom address

8.2.28 Scroll Specified Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	SSA3	SSA2	SSA1	SSA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {SSA3, SSA2, SSA1, SSA0} = FH, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	SSA7	SSA6	SSA5	SSA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {SSA7, SSA6, SSA5, SSA4} = 9H, read address: 5H)

※ mark means “Don’t care”

According to the display panel size or the duty ratio selection, set the specified address in RAM where to jump to the scroll bottom address and then show the fixed data area. Scroll specified address = scroll top address + panel scroll area – 1

8.2.29 Scroll Start Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	SAY3	SAY2	SAY1	SAY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {SAY3, SAY2, SAY1, SAY0} = 0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	SAY7	SAY6	SAY5	SAY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {SAY7, SAY6, SAY5, SAY4} = 0H, read address: 7H)

※ mark means “Don’t care”

Set the starting address of the area scrolling and then executes the area scroll operation. The scroll start address must be in the scrolling area.

Scroll top address <= Scroll start address <= Scroll bottom address

Note: The setting sequence of Scroll start address registers must be setting SAY[7:4] (Bank 3[7H]) first, then setting SAY[3:0] (Bank 3[6H]), to prevent error.

8.2.30 Scroll Mode Select

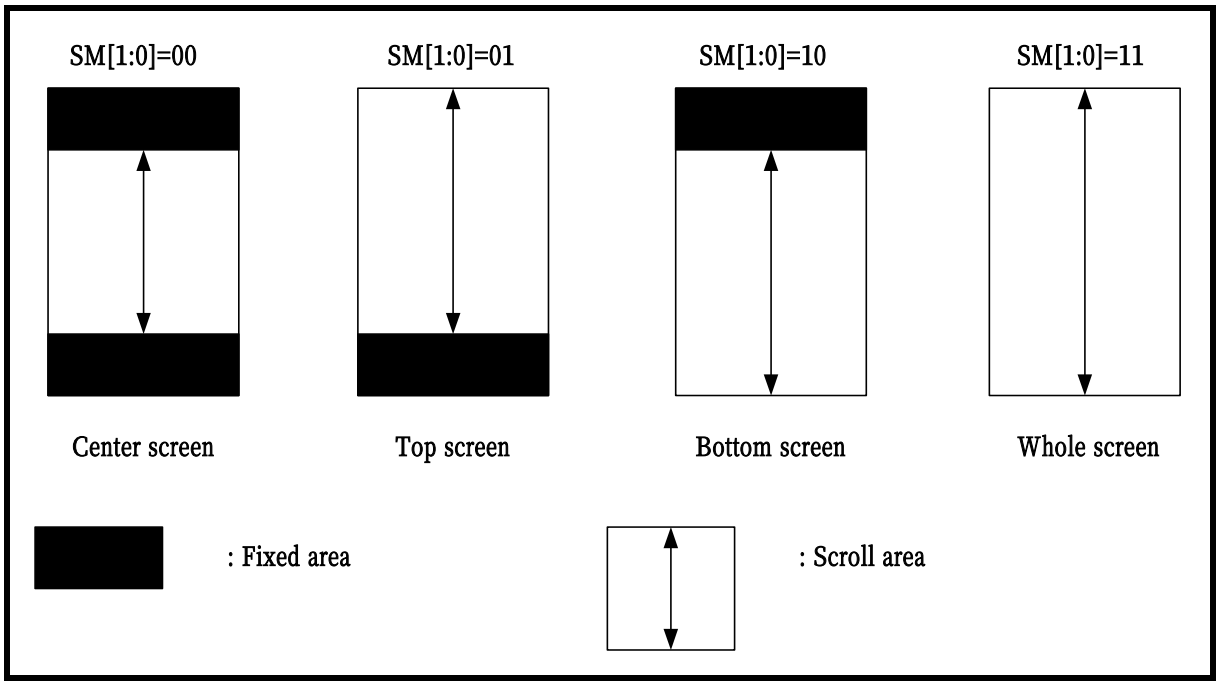
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	*	SM1	SM0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(At the time of reset: {SM1, SM0} = 3H, read address: 8H)

※ mark means “Don’t care”

SM1	SM0	Type of Area Scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll



8.2.31 RAM Data Writing Select Control

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	WBS	RDWS2	RDWS1	RDWS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {WBS, RDWS2, RDWS1, RDWS0} = 0H, read address: 3H)

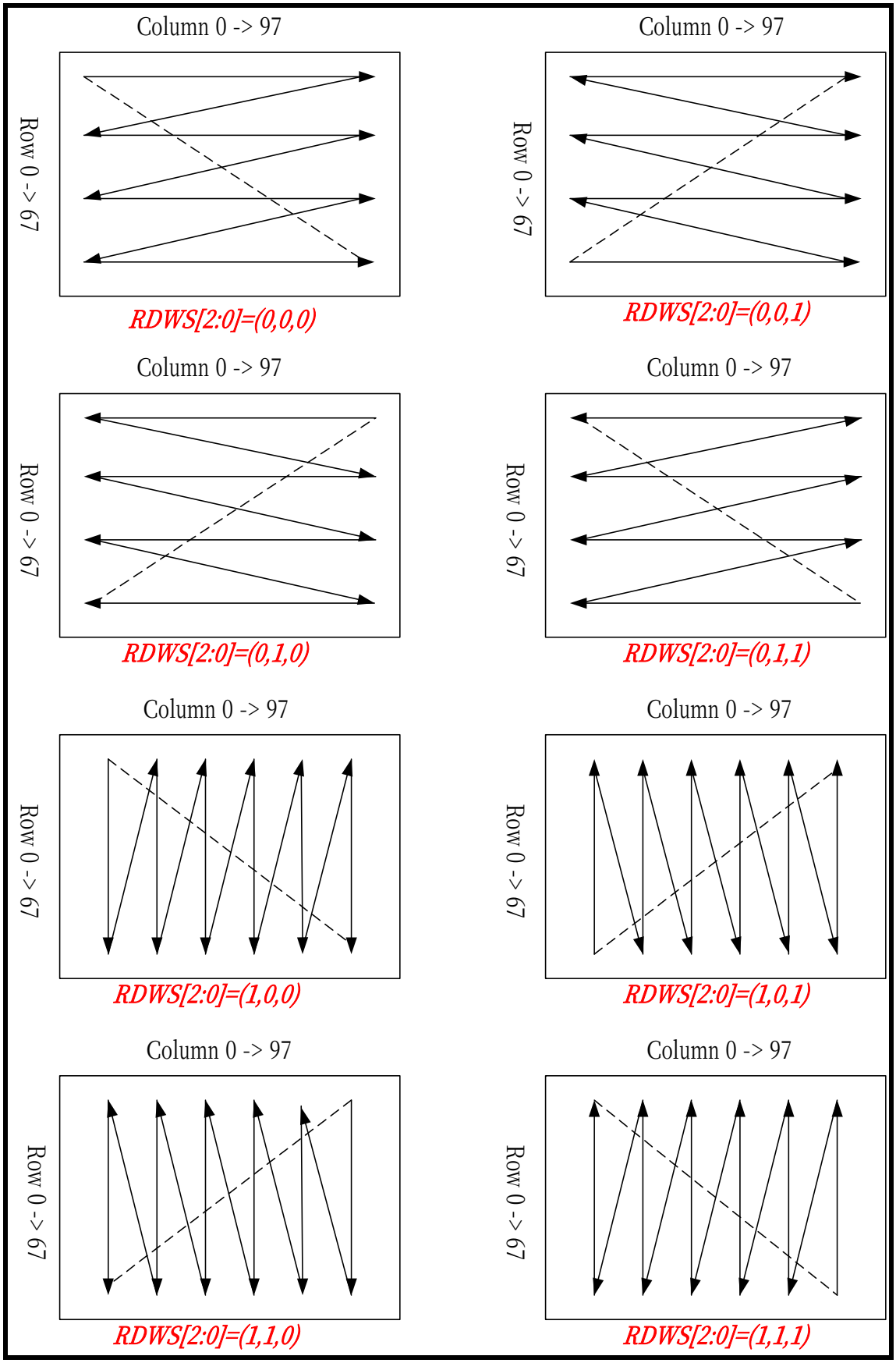
※mark means “Don’t care”

The WBS bit select byte writing sequence while display data writing.

WBS=0, low byte writing first

WBS=1, high byte writing first

The RDWS[2:0] select RAM data writing mode shown as follow:


Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(0,0,0)
Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(0,0,1)
Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(0,1,0)
Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(0,1,1)
Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(1,0,0)
Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(1,0,1)
Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(1,1,0)
Column 0 -> 97
Row 0 -> 67
RDWS[2:0]=(1,1,1)

8.2.32 Display Start Common

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	SC3	SC2	SC1	SC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address=6H)

(At the time of reset:{SC3,SC2,SC1,SC0}=0H)

※ mark means “Don’t care”

The SC register set up the scanning start output of the common driver.

SC3	SC2	SC1	SC0	Display Starting Common when SHIFT=0	Display Starting Common when SHIFT=1
0	0	0	0	COM0~	
0	0	0	1	COM10~	
0	0	1	0	COM20~	
0	0	1	1	COM30~	
0	1	0	0	COM40~	
0	1	0	1	COM50~	
0	1	1	0	COM60~	
1	0	0	1		COM67~
1	0	1	0		COM59~
1	0	1	1		COM49~
1	1	0	0		COM39~
1	1	0	1		COM29~
1	1	1	0		COM19~
1	1	1	1		COM9~

SHIFT=”0”: COM0 to COM67 shift-scan

SHIFT=”1”: COM67 down to COM0 shift-scan

8.2.33 Temperature Compensation Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	TCS1	TCS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset:{ TCS1,TCS0 }=0H, read address: 7H)

※ mark means “Don’t care”

TCS1	TCS0	Temperature Compensation Slope
0	0	-0.05% per °C
0	1	-0.1% per °C
1	0	-0.15% per °C
1	1	-0.2% per °C

K (T) (Temperature compensation output voltage) is control by TCS1, TCS0 and formerly environment temperature T.

$$K_{REF}(T) = K[(1 + TCS(T - 25^{0}C)]$$

✸TCS is selected by TCS1 and TCS0

✸K = 4.005*10^(-3) at 25°C

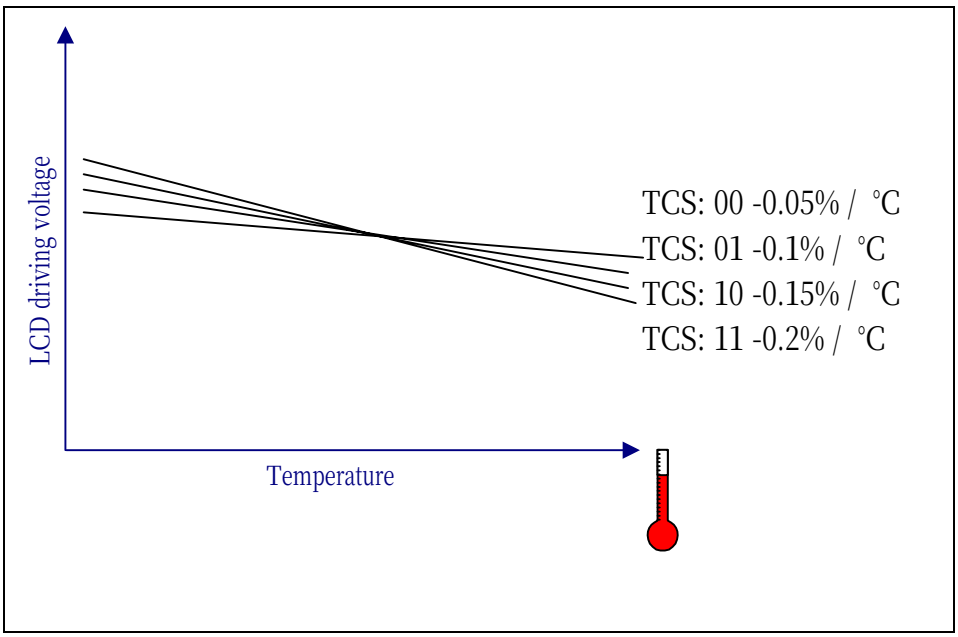


Figure 8-1 Temperature Compensation Slope

8.2.34 Display Select Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	GLSB	*	*

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {GLSB} = 0H, read address: 8H)

※ mark means “Don’t care”

GLSB

In 256 color mode, for the segment driver of 4-gradation display, select 4 gradations from 8 gradations using the 2 bits written to the corresponding RAM area and the 1 bit supplemented by the gradation LSB circuit. Supplement the 1 bit of data by setting the gradation LSB register (GLSB).

Gradation LSB = “0”: Selects 0 as the LSB information on the RAM for 4-gradation segment driver.

Gradation LSB = “1”: Selects 1 as the LSB information on the RAM for 4-gradation segment driver.

8.2.35 RAM Data Length Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	C256	HSW	ABS	WLS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {C256, HSW, ABS, WLS} = 0H, read address: 9H)

※ mark means “Don’t care”

The WLS register select data bus size for access from MPU

WLS = “0”: The data bus size is 8-bits width

WLS = “1”: The data bus size is 16-bits width

When MPU access to control register using 16-bits bus size , high byte data is ignored.

ABS

ABS= “0”: normal mode

ABS= “1”: change corresponding bit from input data bus

HSW

HSW=“0”: High speed writing mode off

HSW=“1”: High speed writing mode on accessing the 8-bit data RAM

*HSW is only used for horizontal direction (X-direction) of multi-RAM data write mode.

C256

C256= “0”: 4096-color mode

C256= “1”: 256-color mode

*IF 65K=1, C256 is prohibited control bit.

8.2.36 Electronic Volume Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	DV3	DV2	DV1	DV0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: AH)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	※	DV6	DV5	DV4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(Read address: BH)

(At the time of reset: {DV6~DV0} = 00H)

※ mark means “Don’t care”

The DV register can control VEV voltage.

The DV register has 7 bits, so can select 128 level voltage.

DV6	DV5	DV4	DV3	DV2	DV1	DV0	Output Voltage
0	0	0	0	0	0	0	Smaller
0	0	0	0	0	0	1	:
			: :				: :
1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	Larger

The output voltage at VEV is specified by equation (1).

VEV = K * (373+(DV+CV))----------(1)

(K: 4.005 * 10^{-3} temperature compensation coefficient, CV: Vop offset setting value of OTP)

VEV range form 1.5V to 2V at 25 °C

The LCD drive voltage V0 is determined by VEV level and RM register value equation
V0 = VEV * N ----------(2)

(N = RM register value)

In order to prevent transient voltage from generating when an electronic volume code is set, the circuit design is such that the set value is not reflected as a level immediately after only the upper bits (DV6-DV4) of the electronic code have been set. The set value becomes valid when the lower bits (DV3-DV0) of the electronic control volume code have also been set.

NOTE

When writing code to set the electronic volume register, set DV6~DV4 first, then set DV3~DV0.

8.2.37 Internal Register Read Address

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	RA3	RA2	RA1	RA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {RA3, RA2, RA1, RA0} = CH)

The RA register set to specify the address for register read operation. The EM65570S has many registers and a register bank. Hence, a maximum of 4-steps are necessary to read a specific register.

(1) Write 04H to RE register for access to RA register.

(2) Writes specific register address to RA register.

(3) Write specific register bank to RE register.

(4) Read specific contents.

8.2.38 RC Oscillator Resistance Ratio

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	RF3	RF2	RF1	RF0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {RF3, RF2, RF1, RF0} = 0H, read address: DH)

※ mark shows “Don’t care”

The RF registers can control the resistance ratio of RC oscillator. Hence, the frame frequency can change the RF registers setting.

When change RF registers value, should be need to check LCD display quality.

RF3	RF2	RF1	RF0	Operation
0	0	0	0	Initial Resistance Ratio
0	0	0	1	0.72 times of initial Resistance Ratio
0	0	1	0	0.86 times of initial Resistance Ratio
0	0	1	1	1.14 times of initial Resistance Ratio
0	1	0	0	1.28 times of initial Resistance Ratio
0	1	0	1	0.65 times of initial Resistance Ratio
0	1	1	0	0.79 times of initial Resistance Ratio
0	1	1	1	0.93 times of initial Resistance Ratio
1	0	0	0	1.07 times of initial Resistance Ratio
1	0	0	1	1.21 times of initial Resistance Ratio
1	0	1	0	1.35 times of initial Resistance Ratio
1	0	1	1	1.42 times of initial Resistance Ratio
1	1	0	0	1.49 times of initial Resistance Ratio
1	1	0	1	1.56 times of initial Resistance Ratio
1	1	1	0	1.63 times of initial Resistance Ratio
1	1	1	1	1.7 times of initial Resistance Ratio

8.2.39 Booster Frequency Control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	BF1	BF0	HPM	DIS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {BF1, BF0, HPM, DIS}=4H;read address: EH)

The DIS register can control capacitors discharged that connected between the power supply V0-V4 for LCD drive voltage and VSS.

When using this register, refer to 7-21 (Discharge circuit).

DIS = “0”: Discharge OFF

DIS = “1”: Discharge start

The HPM register is the power control for the power supply circuit for liquid crystal drive.

HPM= “H”: High power mode

HPM= “L”: Normal mode

BF1~BF0: The operating frequency in the booster is selected. When the boosting frequency is high, the driving ability of booster become high, but the current consumption is increased. Adjust the boosting frequency considering the external capacitors and the current consumption.

BF1	BF0	Booster Operating Clock Frequency
0	0	3kHz * 4
0	1	3kHz * 2
1	0	3kHz
1	1	3kHz * 8

8.2.40 Windows End X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	EX3	EX2	EX1	EX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {EX3, EX2, EX1, EX0} = 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	EX7	EX6	EX5	EX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {EX7, EX6, EX5, EX4} = 0H, read address: 1H)

※Mark shows “Don’t care”

The EX registers set to X direction end address for window function.

8.2.41 Windows End Y Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	EY3	EY2	EY1	EY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {EY3, EY2, EY1, EY0} = 0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	EY7	EY6	EY5	EY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {EY7, EY6, EY5, EY4} = 0H, read address: 3H)

※ mark means “Don’t care”

The EY registers set to Y direction end address for window function.

8.2.42 Line Reverse Start Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LS3	LS2	LS1	LS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {LS3, LS2, LS1, LS0} = 0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	LS7	LS6	LS5	LS4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {LS7, LS6, LS5, LS4} = 0H, read address: 5H)

※ mark means “Don’t care”

The LS registers set to line reverse start address. Moreover, must keep following two conditions.

(1) 00H ≦ LS ≦ 43H

(2) LS ≦ LE LE: Line reverse end address

8.2.43 Line Reverse End Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	LE3	LE2	LE1	LE0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {LE3, LE2, LE1, LE0} = 0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	LE7	LE6	LE5	LE4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {LE7, LE6, LE5, LE4} = 0H, read address: 7H)

※ mark means “Don’t care”

The LE registers set to line reverse end address. Moreover, must keep following two conditions.

(1) 00H ≦ LS ≦ 43H

(2) LS ≦ LE LS: Line reverse start address

8.2.44 Line Reverse Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	EOR	BST	BT	LREV

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {EOR, BST, BT, LREV} = 0H, read address: 8H)

※ mark means “Don’t care”

The EOR control n-line alternated drive.

EOR=0 M always reverses on the nth raster row regardless of whether the end of a frame is reached.

EOR=1 M reverses at the nth raster row and restarts the raster row count at the start of every frame.

The BST register controls the Fast Burst RAM write function

BST = “0”: Burst RAM write function OFF

BST = “1”: Burst RAM write function ON

The LREV registers control line reverse display function.

LREV = “0”: Normal display (Not reverse).

LREV = “1”: Line reverse display enable.

The area specified by Line Reverse Start/End Register reverse display.

The reverse type is selectable by BT register.

When using Line Reverse Display function, LS and LE registers must be kept in following relation.

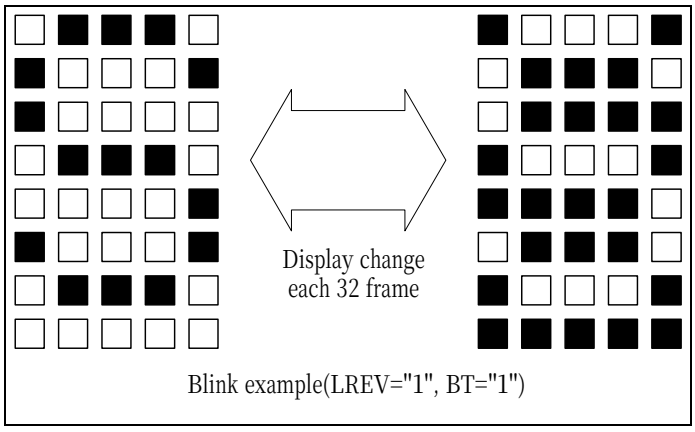
LS ≦ LE

The BT register controls the line reverse type. This is an option of line reverse display function.

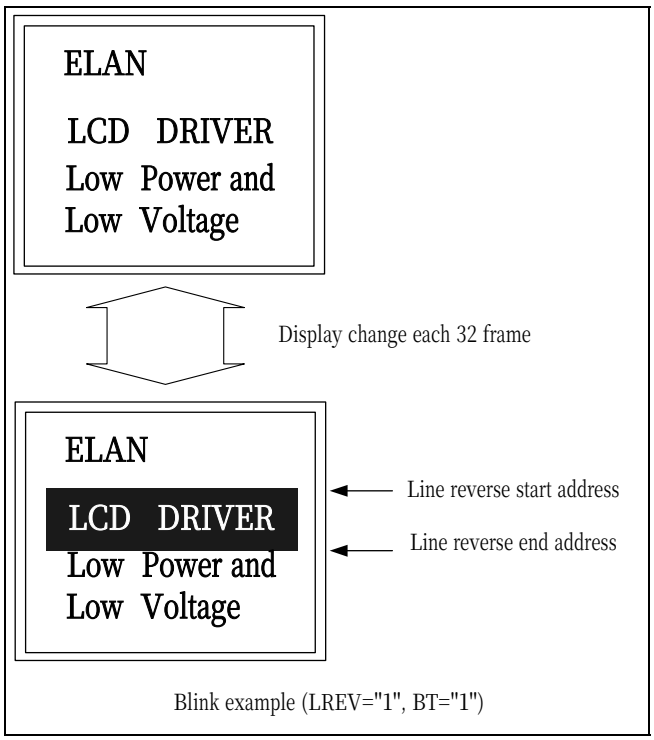
This BTs setting is only available in case of LREV=”1”

BT = “0”: Reverse display

BT = “1”: Reverse display for every 32 frames.



Blink example(LREV="1", BT="1")



8.2.45 Regulator Multiple Ratio Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	RM3	RM2	RM1	RM0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {RM3, RM2, RM1, RM0} = 5H, read address: 9H)

※ mark means “Don’t care”

The booster steps set to RM register

RM3	RM2	RM1	RM0	Regulator Multiple Ratio Control
0	0	0	0	3.0 times voltage output
0	0	0	1	4.5 times voltage output
0	0	1	0	6.0 times voltage output
0	0	1	1	7.5 times voltage output
0	1	0	0	8.0 times voltage output
0	1	0	1	8.5 times voltage output
1	0	0	0	4.0 times voltage output

8.2.46 OTP Mode Select Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	M1	M0	VPP_EXT	*

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {M1, M0, VPP_EXT, *} = CH, read address: AH)

The (M1, M0) register control OTP mode

(M1, M0)	OTP Operating Mode	Delay Time
00	Read	-
01	Program	-
10	Reserve	-
11	Standby	-

NOTE

1. When using OTP Program function, RM must be 1000 (4 times)

2. In program mode, the delay time necessary is more than 1ms

8.2.47 Vop Calibration Offset Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	CV3	CV2	CV1	CV0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(read address: BH)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	*	*	CV5	CV4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(read address: EH)

The CV5~CV0 register control Vop calibration offset voltage selection

VEV = K*(373+(DV+CV)) K=4.005*10^{-3}

CV5~CV0	Calibration Offset
011111	+31
011110	+30
…	…
000001	+1
000000	0
100000	-32
100001	-31
…	…
111111	-1

NOTE

1. if CV5~CV0 has not been programmed (OTP programming) , then CV5~CV0 will be equal to 3FH (-1) at the time of reset.

2. if CV5~CV0 have been programmed (OTP programming), then CV5~CV0 will be equal to the programming-value at the time of reset.

9 Absolute Maximum Rating

9.1 Absolute Maximum Ratings

Item	Symbol	Condition	Pin Used	Rating	Unit
Supply voltage (1)	VDD	Ta=25°C	VDD	-0.3 ~ + 4.0	V
Supply voltage (2)	VEE		VEE	-0.3 ~ + 4.0	V
Supply voltage (3)	VOUT		VOUT	--0.3 ~ + 19	V
Supply voltage (4)	VEV		VEV	1.5 ~ + 2.0	V
Supply voltage (5)	V0		V0	-0.3 ~ + 18.5	V
Supply voltage (6)	V1,V2,V3,V4		V1,V2,V3,V4	-0.3 ~ V0+ 0.3	V
Input voltage	VI		*1	-0.3 ~ VDD+ 0.3	V
Storage temperature	Tstg			-45 ~ +125	°C

9.2 Recommended Operating Conditions

Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Note
Supply voltage	VDD1	VDD	2.2		3.3	V	*1
	VDD2 VDD3	VDD	2.4		3.3	V	*2
	VEE	VEE	2.4		3.3	V	*3
Operating voltage	V0	V0	4.5		18.5	V	*4
	VOUT	VOUT			19	V	*5
	VEV	VEV		1.5	2.0	V	
Operating temperature	Topr		-30		85	°C	

NOTE

1. Power supply for logic circuit

2. Power supply for analog circuit.

3. Power supply for internal boosting circuit. If applied voltage same as VDD, connect to VDD.

4. Voltage V0>V1>V2>V3>V4>VSS must always satisfied.

5. Voltage VOUT > V0 must always satisfy.

10 DC electrical Characteristics

VSS=0V, VDD = 2.2 ~3.3V, Ta = -30 ~85°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Pin Used
High level input voltage	VIH	-		0.8VDD	0.9VDD	VDD	V	※1
Low level input voltage	VIL	-		0	0.1VDD	0.2VDD	V	※1
High level output current	IOH1	VOH = VDD-0.4V		-2.7	-3.2	-3.5	mA	※2
Low level output current	IOL1	VOL= 0.4V		2.7	3.2	3.5	mA	※2
High level output current	IOH2	VOH = VDD-0.4V		-0.8	-1.0	-1.2	mA	※3
Low level output current	IOL2	VOL= 0.4V		0.8	1.0	1.2	mA	※3
Input leakage current	ILI1	VI = VSS or VDD		-2	0	2	µA	※4
Output leakage current	ILO	VI = VSS or VDD		-2	0	2	µA	※5
LCD driver output resistance	RON	Δ |Von| = 0.5V	V0=10V	1.0	1.3	1.6	KΩ	※6
			V0=6V	1.2	1.7	2.2		
Standby current through VDD pin	ISTB	CK=0, CSB=VDD, Ta=25°C, VDD=3V			5	15	µA	※7
Oscillator frequency (48 gradation mode)	$Fosc_1$	VDD=3V, Ta=25°C, Rf setting = (Rf2,Rf1,Rf0)=(000)		731	754	776	kHz	※8
Oscillator frequency (16 gradation mode)	$Fosc_2$	VDD=3V, Ta=25°C, Rf setting = (Rf2,Rf1,Rf0)=(000)		365	377	388	kHz	※9
Oscillator frequency (8 gradation mode)	$Fosc_3$	VDD=3V , Ta=25°C, Rf setting = (Rf2,Rf1,Rf0)=(000)		182	188	193	kHz	※10
Booster output voltage on VOUT pin	VOUT1	Five times boosting RL = 500KΩ (VOUT-VSS)		5*VEE *0.95	5*VEE *0.98	5*VEE *0.99	V	※11
	VOUT2	Four times boosting RL = 500KΩ (VOUT-VSS)		4*VEE *0.95	4*VEE *0.98	4*VEE *0.99	V	※12
	VOUT3	Three times boosting RL = 500KΩ (VOUT-VSS)		3*VEE *0.95	3*VEE *0.98	3*VEE *0.99	V	※13

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
	VOUT4	Two times boosting RL = 500KΩ (VOUT-VSS)	2*VEE *0.95	2*VEE *0.98	2*VEE *0.99	V	※14
Current Consumption	IDD1	VDD = 3.0V, 5 times booster, All ON pattern	-	350		μA	※15
	IDD2	VDD = 3.0V, 5 times booster, Checker pattern	-	400		μA	※16
VEV output voltage	VEV	VDD =2.4V~3.3V	1.5		2.0	V	※17
V0 output voltage	V0	VDD = 2.4 ~ 3.3V	0.99*V0	V0	1.01*V0	V	

Relationship between oscillating frequency (fosc) and external clock frequency (fCK) to LCD frame frequency (fFLM) is each display mode

Original Oscillating Clock	Display Mode	Display Duty Cycle Ratio (1/D)			
		1/72 to 1/48	1/32 to 1/24	1/16	1/8
When use built-in oscillating circuit (fosc)	Simple gradation (65K color)	fosc/(4*31*D)	fosc/(8*31*D)	fosc/(16*31*D)	fosc/(32*31*D)
	Simple gradation (4096 color)	fosc/(4*15*D)	fosc/(8*15*D)	fosc/(16*15*D)	fosc/(32*15*D)
	Simple gradation (256 color)	fosc/(4*7*D)	fosc/(8*7*D)	fosc/(16*7*D)	fosc/(32*7*D)
When use external clock from CK pin. (fCK)	Simple gradation (65K color)	fCK/(4*31*D)	fCK/(8*31*D)	fCK/(16*31*D)	fCK/(32*31*D)
	Simple gradation (4096 color)	fCK/(4*15*D)	fCK/(8*15*D)	fCK/(16*15*D)	fCK/(32*15*D)
	Simple gradation (256 color)	fCK/(4*7*D)	fCK/(8*7*D)	fCK/(16*7*D)	fCK/(32*7*D)

Pin used:

1 D0-D15, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins.

2 D0~D15 pins

3 CLK pins

4 CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins

5 Applied when D0~D15 are in the state of high impedance.

6 SEGA0~SEGA97, SEGB0~SEGB97, SEGC0~SEGC97, COM0~COM67 pins Resistance when being applied 0.5V between each output pin and each power supply (V0, V1, V2, V3, V4) and when being applied 1/14 bias.

7 VDD pin, VDD pin current without load at the stoppage of original oscillating clock and at non-select (CSB=VDD)

8 Oscillating frequency, when using the built-in oscillating circuit (48 gradation display mode)

9 Oscillating frequency, when using the built-in oscillating circuit (16 gradation display mode)

10 Oscillating frequency, when using the built-in oscillating circuit (8 gradation display mode)

11 VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 5 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/4~1/9, 1/72 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”

12 VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 4 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/4~1/9, 1/72 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”

13 VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 3 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/4~1/9, 1/72 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”

14 VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 2 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/4~1/9, 1/72 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1”, BF=”11”

15 VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 5 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display ALL ON pattern {Rf2, Rf1, Rf0 = (“0 0 0 ”) } and LCD driver pin with no load. Measuring conditions: VDD=VEE , C1=C2=1.0μF, C3=0.1μF, DV=7FH, RM=02H, DCON=AMPON=”1” , NLIN=”0”, (BF1,BF0)=(1,1),1/72 duty , 1/7 bias , BF=”11”

16 VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 5 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display a checkered pattern, {Rf2, Rf1, Rf0 = (“0 0 0 ”) } and LCD driver pin with no load. Measuring conditions: VDD=VEE, C1=C2=1.0μF, C3=0.1μF, DV=7FH, RM=02H, DCON=AMPON=”1” , NLIN=”0” ,(BF1,BF0)=(1,1) ,1/72 duty , 1/7 bias, BF=”11”

17 VEV pin. Measuring conditions: N times boosting (N=2~8), electronic control = “1 1 1 1 1 1” , Display a checkered pattern , DCON=AMPON=”1” , NLIN=”0” ,1/72 duty , VDD=VEE , C1=C2=1.0μF, C3=0.1μF , no load

NOTE

The capacitor C1 is use for booster related pin.

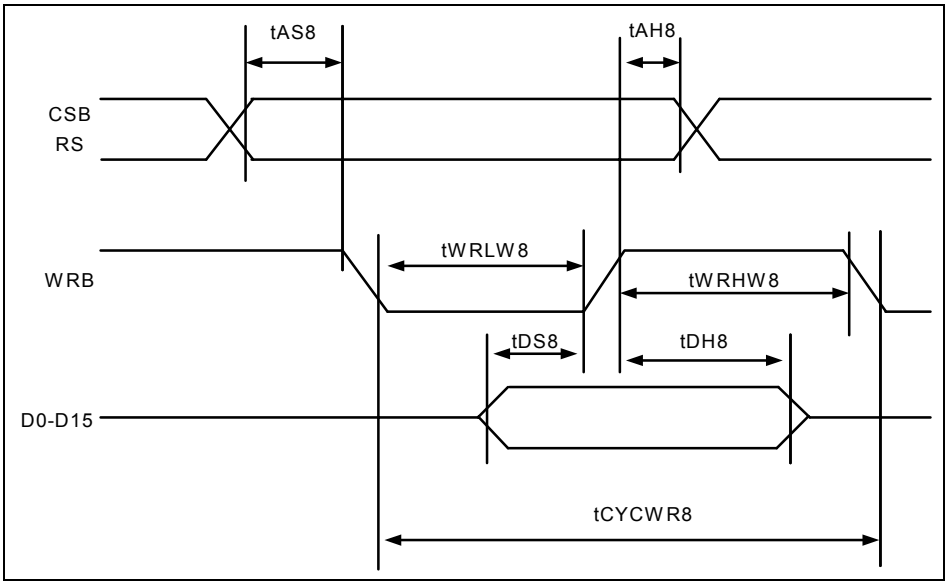
CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3- , CAP4+ , CAP2- and VOUT, VSS

The capacitor C2 is use for bias related pin.

V0, V1, V2, V3, V4

11 Ac Electrical Characteristics

11.1 80-family MCU write timing



VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		20			ns	CSB RS
Address setup time	tAS8		20			ns	
System cycle time in write	tCYCWR8		330			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		50			ns	
Write pulse “H” width	tWRHW8		250			ns	
Data setup time	tDS8		20			ns	D0~D15
Data hold time	tDH8		20			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8	-	40	-	-	ns	CSB RS
Address setup time	tAS8	-	40	-	-	ns	
System cycle time in write	tCYCWR8	-	400	-	-	ns	WRB (R/WB)
Write pulse “L” width	tWRLW8	-	70	-	-	ns	
Write pulse “H” width	tWRHW8	-	300	-	-	ns	
Data setup time	tDS8	-	40	-	-	ns	D0~D15
Data hold time	tDH8	-	40	-	-	ns	

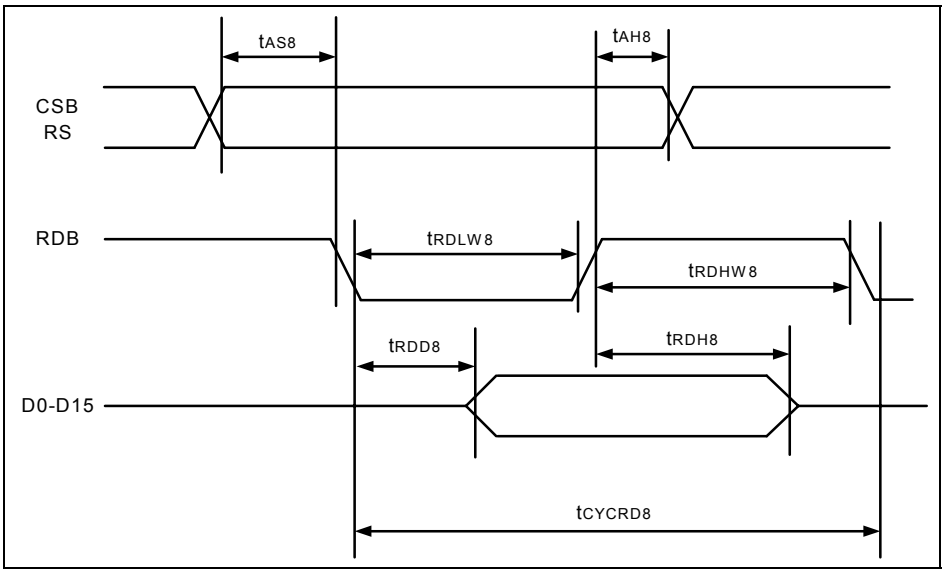
VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		40			ns	CSB RS
Address setup time	tAS8		40			ns	
System cycle time in write	tCYCWR8		500			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		100			ns	
Write pulse “H” width	tWRHW8		350			ns	
Data setup time	tDS8		40			ns	D0~D15
Data hold time	tDH8		40			ns	

NOTE

All the timings must be specified relative to 20% and 80% of VDD voltage.

11.2 80-family MCU Read Timing



VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		20			ns	CSB RS
Address setup time	tAS8		20			ns	
System cycle time in read	tCYCRD8		530			ns	RDB(E)
Read pulse “L” width	tRDLW8		220			ns	
Read pulse “H” width	tRDHW8		280			ns	
Data setup time	tRDD8	CL = 80 pF			230	ns	D0~D15
Data hold time	tRDH8		20			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		40			ns	CSB RS
Address setup time	tAS8		40			ns	
System cycle time in read	tCYCRD8		620			ns	RDB(E)
Read pulse “L” width	tRDLW8		260			ns	
Read pulse “H” width	tRDHW8		330			ns	
Data setup time	tRDD8	CL = 80 pF			270	ns	D0~D15
Data hold time	tRDH8		40			ns	

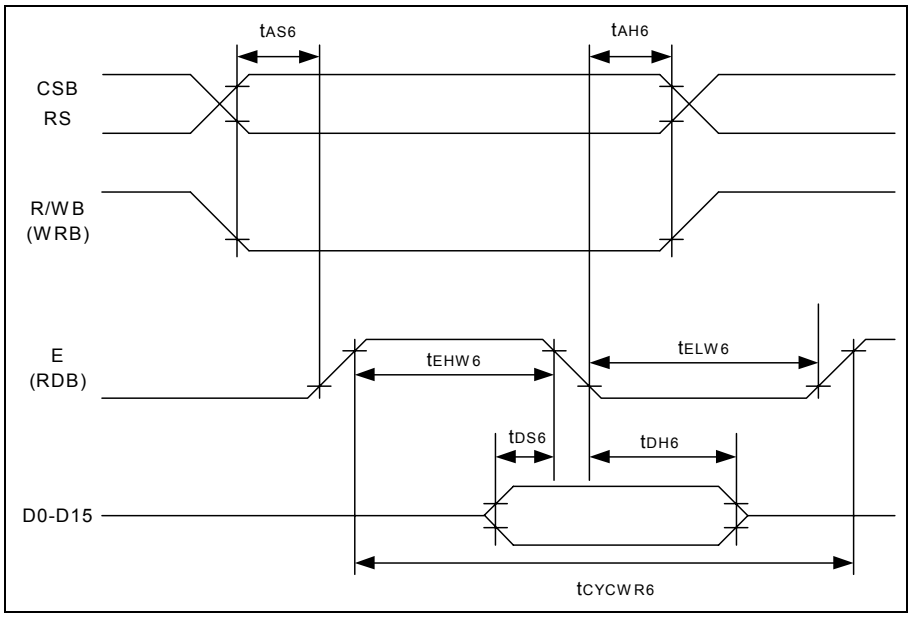
VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH8		40			ns	CSB RS
Address setup time	tAS8		40			ns	
System cycle time in read	tCYCRD8		720			ns	RDB(E)
Read pulse “L” width	tRDLW8		290			ns	
Read pulse “H” width	tRDHW8		390			ns	
Data setup time	tRDD8	CL = 80 pF			300	ns	D0~D15
Data hold time	tRDH8		40			ns	

NOTE

All the timings must be specified relative to 20% and 80% of VDD voltage.

11.3 68-family MCU Write Timing



VSS=0V, VDD = 2.7 ~3.3V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		20			ns	CSB RS
Address setup time	tAS6		20			ns	
System cycle time in write	tCYCWR6		330			ns	RDB(E)
Write pulse “L” width	tELW6		250			ns	
Write pulse “H” width	tEHW6		50			ns	
Data setup time	tDS6		20			ns	D0~D15
Data hold time	tDH6		20			ns	

VSS=0V, VDD = 2.4 ~2.7V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		40			ns	CSB RS
Address setup time	tAS6		40			ns	
System cycle time in write	tCYCWR6		400			ns	RDB(E)
Write pulse “L” width	tELW6		300			ns	
Write pulse “H” width	tEHW6		70			ns	
Data setup time	tDS6		40			ns	D0~D15
Data hold time	tDH6		40			ns	

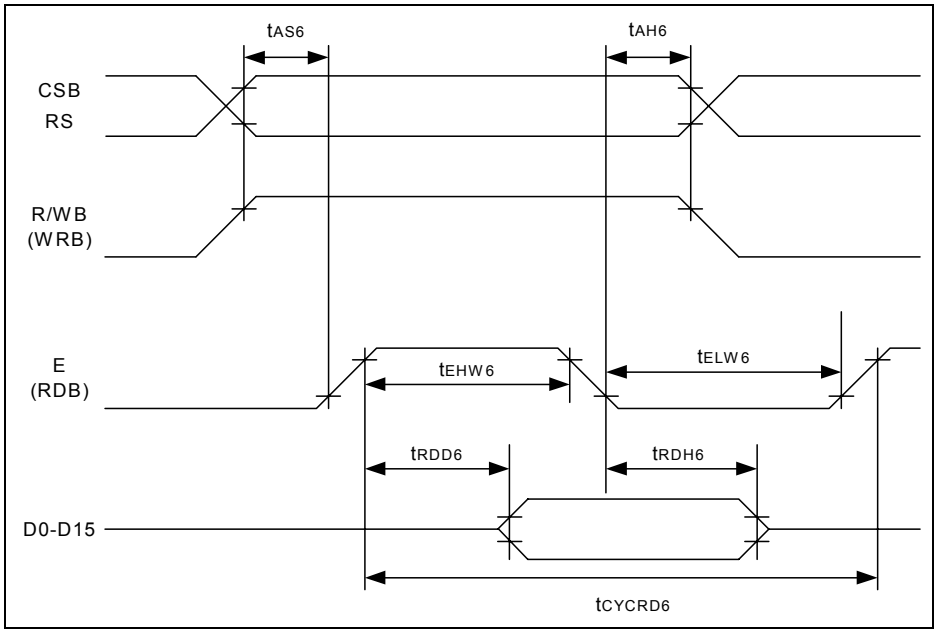
VSS=0V, VDD = 2.2 ~2.4V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		40			ns	CSB RS
Address setup time	tAS6		40			ns	
System cycle time in write	tCYCWR6		500			ns	RDB(E)
Write pulse “L” width	tELW6		350			ns	
Write pulse “H” width	tEHW6		100			ns	
Data setup time	tDS6		40			ns	D0~D15
Data hold time	tDH6		40			ns	

NOTE

All the timings must be specified relative to 20% and 80% of VDD voltage.

11.4 68-family MCU Read Timing



VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		20			ns	CSB RS
Address setup time	tAS6		20			ns	
System cycle time in read	tCYCRD6		530			ns	RDB(E)
Write pulse “L” width	tELW6		220			ns	
Write pulse “H” width	tEHW6		280			ns	
Data setup time	tRDD6	CL=50pF			230	ns	D0~D15
Data hold time	tRDH6		20			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6	-	40			ns	CSB RS
Address setup time	tAS6	-	40			ns	
System cycle time in read	tCYCRD6	-	620			ns	RDB(E)
Write pulse “L” width	tELW6	-	260			ns	
Write pulse “H” width	tEHW6	-	330			ns	
Data setup time	tRDD6	CL=50pF			270	ns	D0~D15
Data hold time	tRDH6		40			ns	

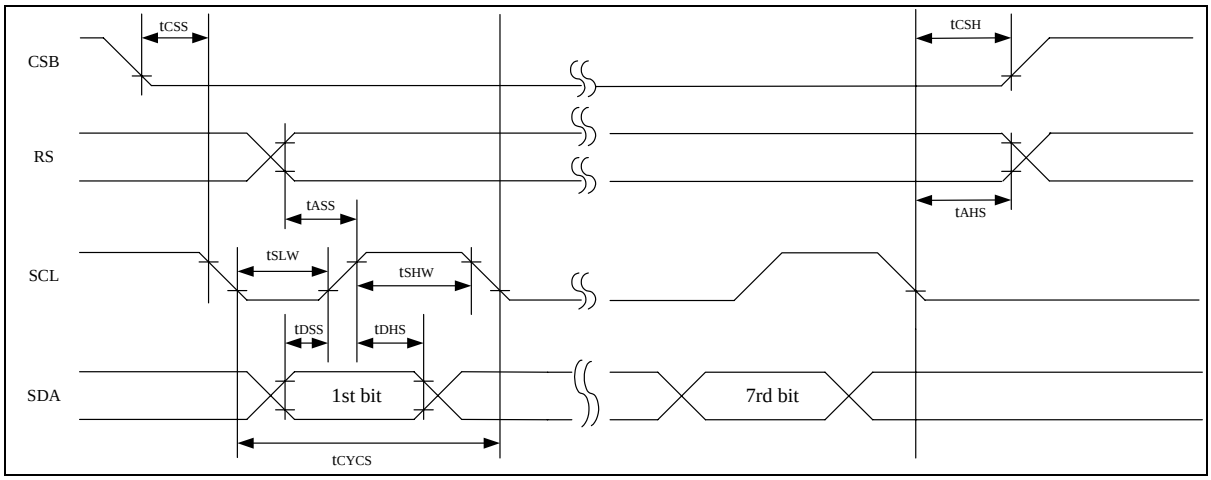
VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address hold time	tAH6		40			ns	CSB RS
Address setup time	tAS6		40			ns	
System cycle time in read	tCYCRD6		720			ns	RDB(E)
Write pulse “L” width	tELW6		290			ns	
Write pulse “H” width	tEHW6		390			ns	
Data setup time	tRDD6	CL=50pF			300	ns	D0~D15
Data hold time	tRDH6		40			ns	

NOTE

All the timings must be specified relative to 20% and 80% of VDD voltage.

11.5 Serial Interface Timing Diagram



VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Serial clock period	tCYCS		100			ns	SCL
SCL pulse “H” width	tSHW		40			ns	
SCL pulse “L” width	tSLW		40			ns	
Address setup time	tASS		20			ns	RS
Address hold time	tAHS		20			ns	
Data setup time	tDSS		40			ns	SDA
Data hold time	tDHS		40			ns	
CSB-SCL time	tCSS		20			ns	CSB
CSB hold time	tCSH		20			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Serial clock period	tCYCS		150			ns	SCL
SCL pulse “H” width	tSHW		60			ns	
SCL pulse “L” width	tSLW		60			ns	
Address setup time	tASS		40			ns	RS
Address hold time	tAHS		40			ns	
Data setup time	tDSS		60			ns	SDA
Data hold time	tDHS		60			ns	
CSB-SCL time	tCSS		40			ns	CSB
CSB hold time	tCSH		40			ns	

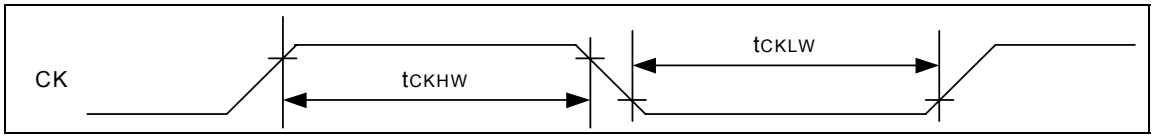
VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		40			ns	RS
Address hold time	tAHS		40			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		40			ns	CSB
CSB hold time	tCSH		40			ns	

NOTE

All the timings must be specified relative to 20% and 80% of VDD voltage.

11.6 Clock Input Timing

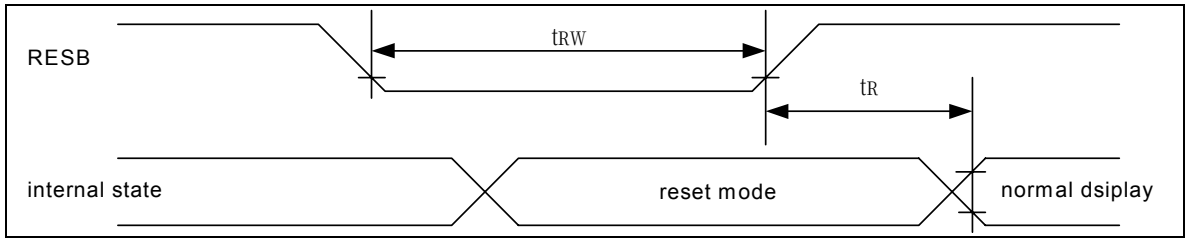


VSS=0V, VDD = 2.2~3.3V, Ta = -30~+85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
CK pulse “H” width	tTCKHW2		5.4		6.5	μs	CK
CK pulse “L” width	tCKLW2		5.4		6.5	μs	※ 1

※1 Applied when the gradation display mode 65K=”1”

11.7 Reset Timing



VSS=0V, VDD = 2.2~3.3V, Ta = -30~+85°C

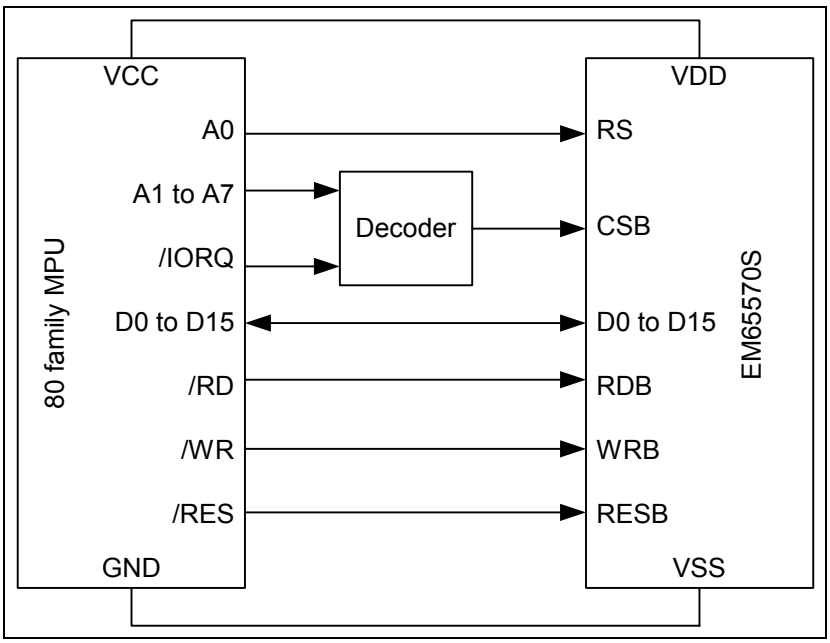
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Reset time	tR				1	μs	
Reset pulse “L” width	tRW		150			μs	RESB

NOTE

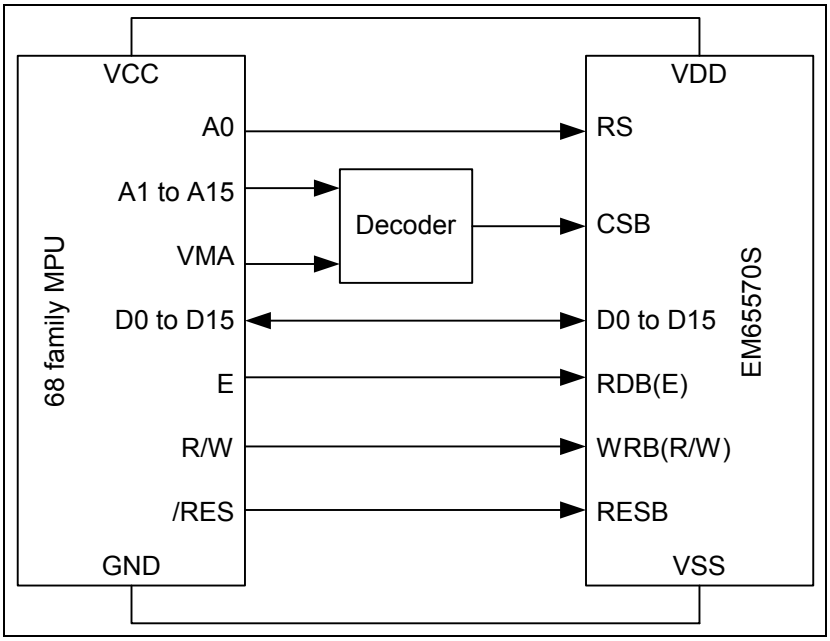
All the timings must be specified relative to 20% and 80% of VDD voltage.

12 Application Circuit

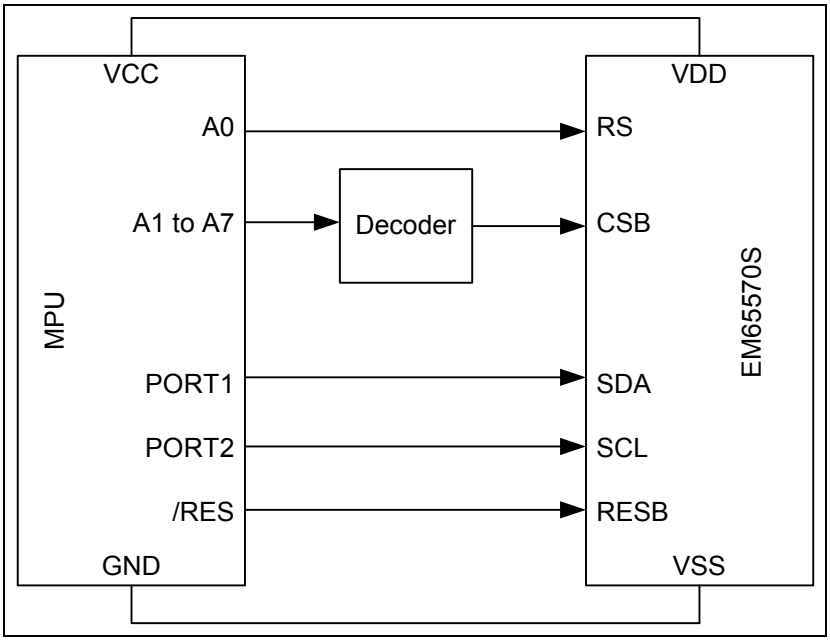
12.1 Connection to 80-family MCU



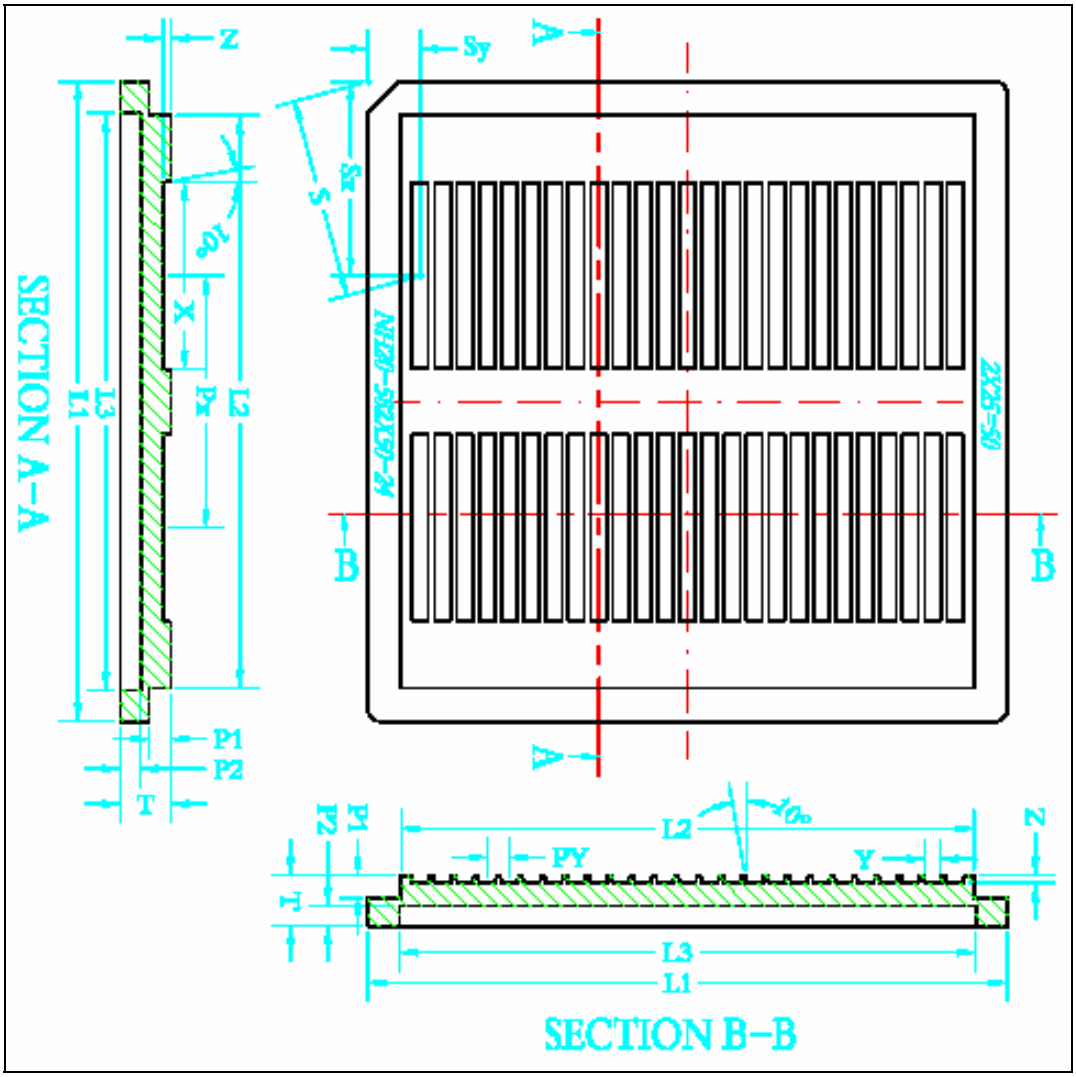
12.2 Connection to 68-family MCU



12.3 Connection to the MCU with Serial Interface



13 Tray Information



13.1 Tray Outline Dimensions

Symbol	Dimensions in mm	Symbol	Dimensions in mm
L1	50.75	Z	0.61 ± 0.05
L2	45.50	Px	20.00
L3	45.70	Py	1.77
T	4.00	Nx	2
Sx	15.40	Ny	25
Sy	4.16	N	50
S	15.95	P1	1.76
X	14.78 ± 0.05	P2	1.60
Y	1.27 ± 0.05		

Unit : mm