DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT583
4-bit full adder with fast carry

Product specification
Supersedes data of December 1990
File under Integrated Circuits, IC06

1998 Mar 31

Philips
Semiconductors

PHILIPS

4-bit full adder with fast carry 74HC/HCT583

FEATURES

- Adds two decimal numbers
- Full internal look-ahead
- Fast ripple carry for economical expansion
- Output capability: standard driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT583 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JECEC standard no. 7A.

The 74HC/HCT583 are high-speed 4-bit BCD full adders with internal carry look-ahead. They accept two 4-bit decimal numbers (A_0 to A_3 and B_0 to B_3) and a carry input (C_{IN}).

The "583" generates the decimal sum outputs (Σ_0 to Σ_3) and a carry output (C_{n+4}) if the sum is greater than 9.

If an addition of two BCD numbers produce a number greater than 9, a valid BCD number and a carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading "583s".

See the "283" for the binary version.

QUICK REFERENCE DATA

GND = 0 V; T_{amb}= 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	C_{IN} to C_{n+4}		20	23	ns
	A_n, B_n to C_{n+4}		23	27	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	116	120	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC583	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC583	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT583	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HCT583	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5	C_{IN}	carry input
6	C_{n+4}	carry output
8	GND	ground (0 V)
11, 10, 7, 9	Σ_0 to Σ_3	sum outputs
12, 1, 2, 3	B_0 to B_3	B operand inputs
13, 14, 15, 4	A_0 to A_3	A operand inputs
16	V_{CC}	positive supply voltage

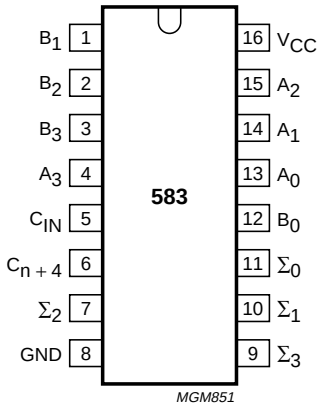


Fig.1 Pin configuration.

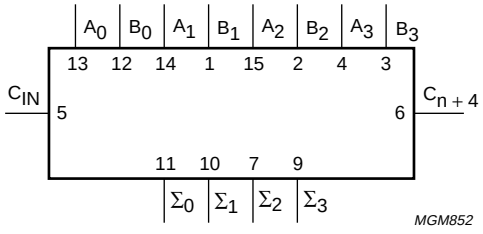


Fig.2 Logic symbol.

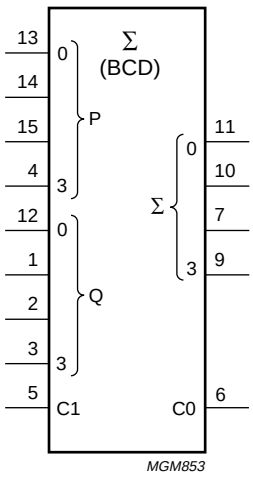


Fig.3 IEC logic symbol.

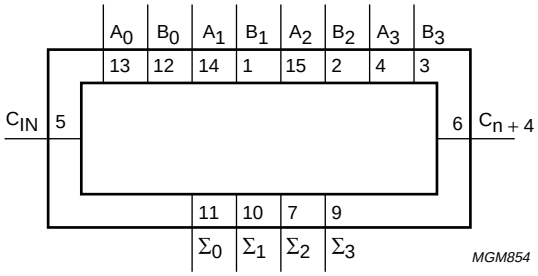


Fig.4 Functional diagram.

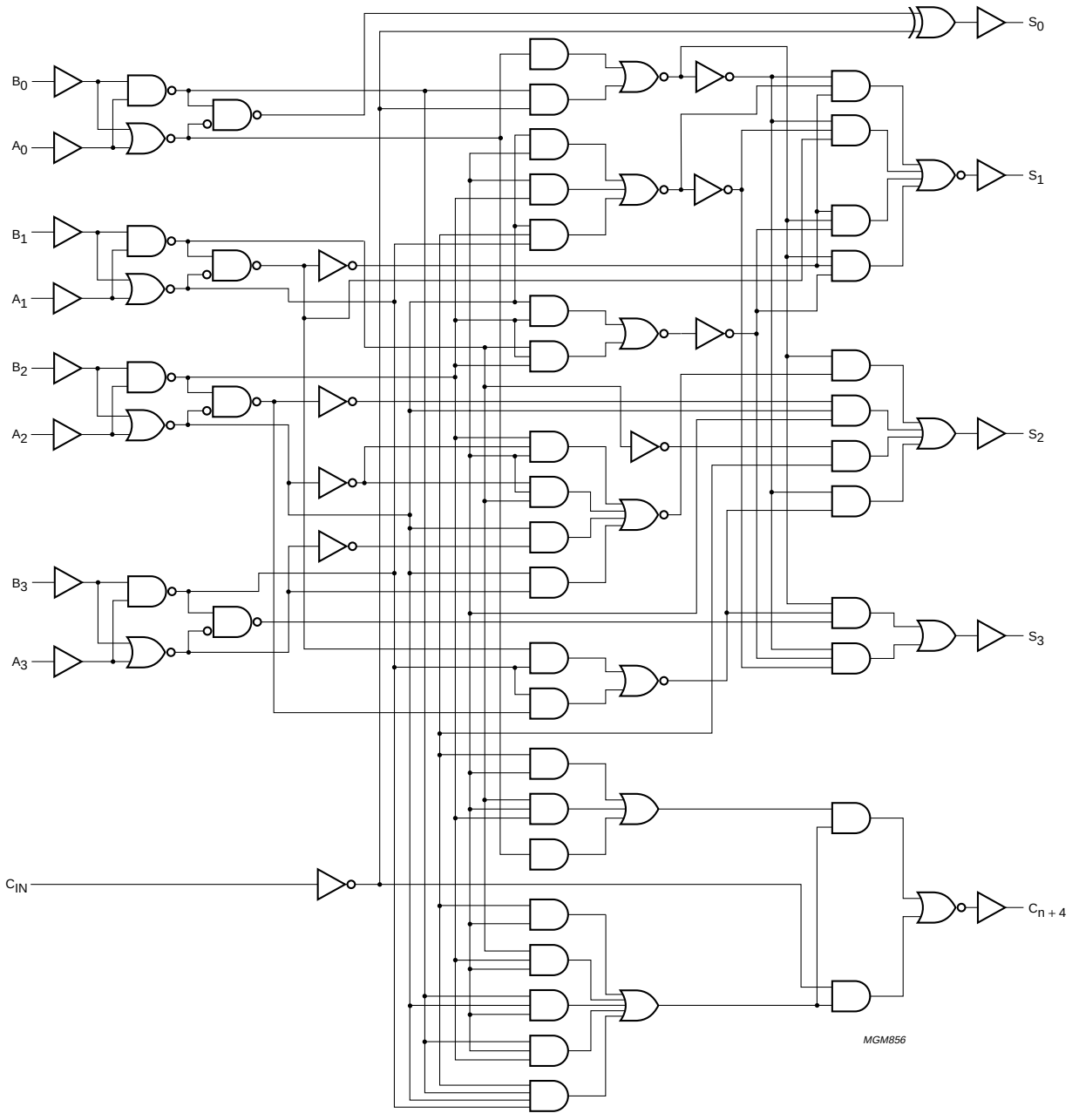


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_0		50	155		195		235	ns	2.0	Fig.6
			18	31		39		47		4.5	
			14	26		33		40		6.0	
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_1		113	350		440		525	ns	2.0	Fig.6
			41	70		88		105		4.5	
			33	60		75		90		6.0	
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_2		100	305		380		460	ns	2.0	Fig.6
			36	61		76		92		4.5	
			29	52		65		78		6.0	
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_3		110	340		425		510	ns	2.0	Fig.6
			40	68		85		102		4.5	
			32	58		72		87		6.0	
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_0		50	155		195		235	ns	2.0	Fig.6
			18	31		39		47		4.5	
			14	26		33		40		6.0	
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_1		120	365		455		550	ns	2.0	Fig.6
			43	73		91		110		4.5	
			34	62		77		94		6.0	
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_2		105	325		405		490	ns	2.0	Fig.6
			38	65		81		98		4.5	
			30	55		69		83		6.0	
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_3		116	355		445		535	ns	2.0	Fig.6
			42	71		89		107		4.5	
			34	60		76		91		6.0	
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to C_{n+4}		63	195		245		295	ns	2.0	Fig.6
			23	39		49		59		4.5	
			18	33		42		50		6.0	
t_{PHL}/ t_{PLH}	propagation delay A_n to C_{n+4}		72	220		275		330	ns	2.0	Fig.6
			26	44		55		66		4.5	
			21	37		47		56		6.0	

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay B_n to C_{n+4}		74	230		290		345	ns	2.0	Fig.6
			27	46		58		69		4.5	
			22	39		49		59		6.0	
t_{THL}/ t_{TLH}	output transition time standard outputs		19	75		95		110	ns	2.0	Fig.6
			7	15		19		22		4.5	
			6	13		16		19		6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

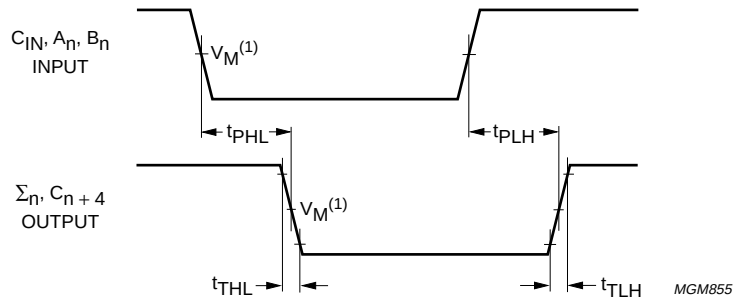
INPUT	UNIT LOAD COEFFICIENT
A_n, B_n	0.4
C_{IN}	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_0		20	34		43		51	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_1		40	68		85		102	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_2		38	65		81		98	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_3		38	65		81		98	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_0		22	37		46		56	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_1		43	73		91		110	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_2		40	68		85		102	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_3		41	70		88		105	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to C_{n+4}		27	46		58		69	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n to C_{n+4}		31	53		66		80	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay B_n to C_{n+4}		30	51		64		77	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time standard outputs		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS

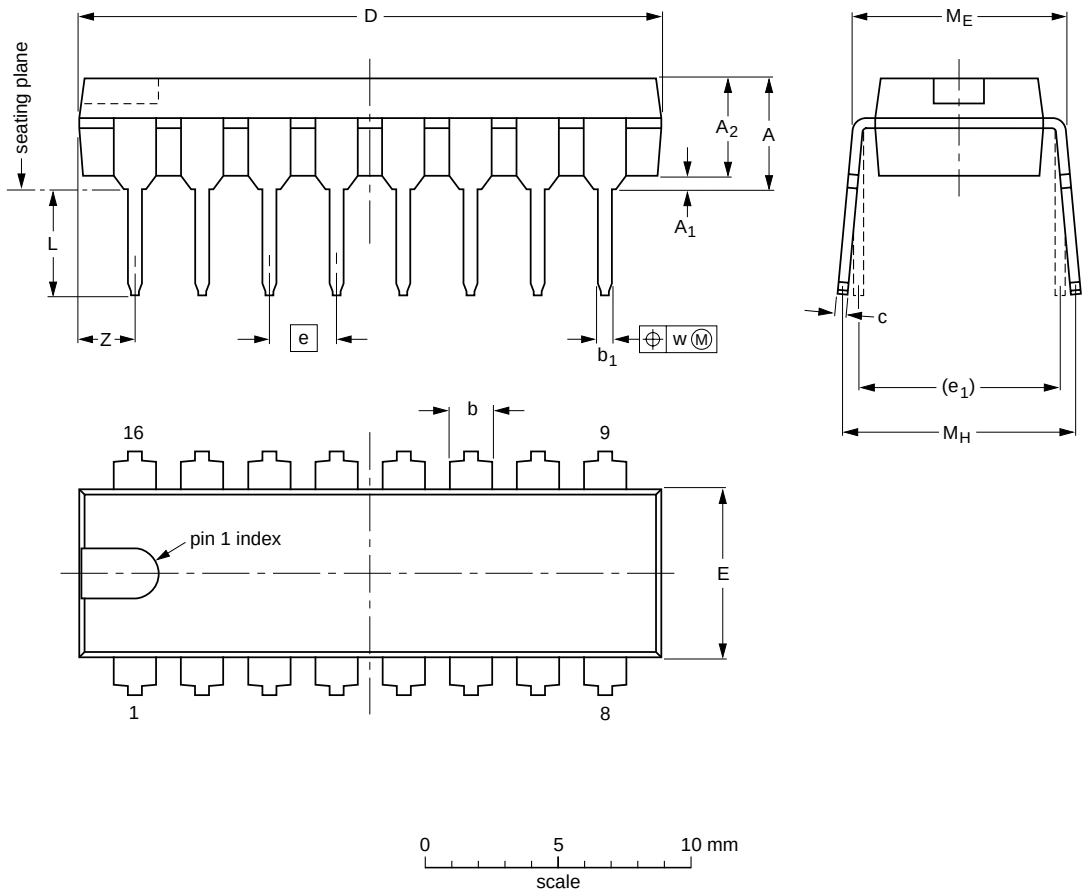


(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the inputs (C_{IN}, A_n, B_n) to the outputs (Σ_n, C_{n+4}) propagation delays and the output transition times.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

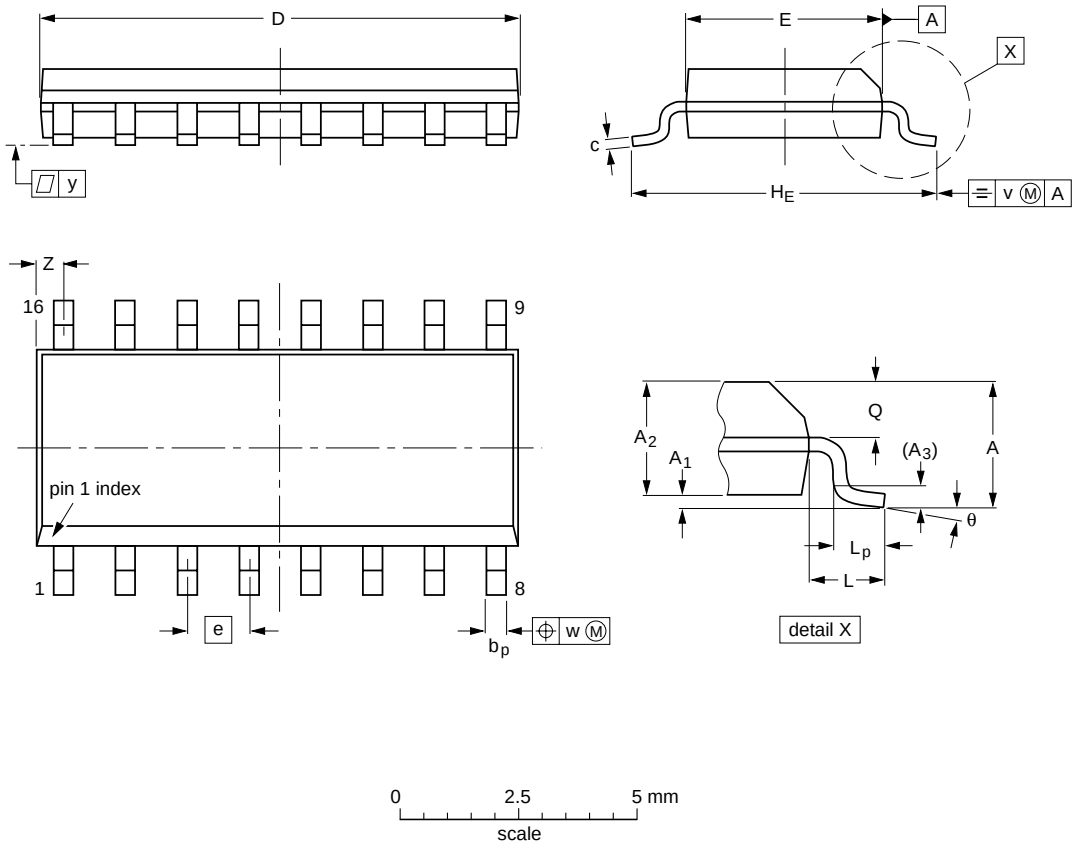
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.