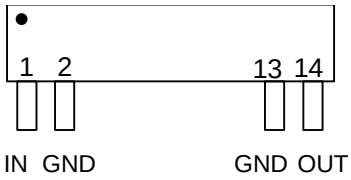
# FIXED SIP DELAY LINE
# $T_D/T_R = 10$
# (SERIES 1515)

data delay devices, inc.

## FEATURES

- Fast rise time for high freq. applications
- Very narrow device (SIP package)
- Stackable for PC board economy
- Low profile
- Epoxy encapsulated
- Meets or exceeds MIL-D-23859C

## PACKAGES




1515-xxz
xx = Delay ($T_D$)
z = Impedance Code

## FUNCTIONAL DESCRIPTION

The 1515-series device is a fixed, single-input, single-output, passive delay line. The signal input (IN) is reproduced at the output (OUT), shifted by a time ($T_D$) given by the device dash number. The characteristic impedance of the line is given by the letter code that follows the dash number (See Table). The rise time ($T_R$) of the line is 10% of $T_D$, and the 3dB bandwidth is given by 3.5 / $T_D$.

## PIN DESCRIPTIONS

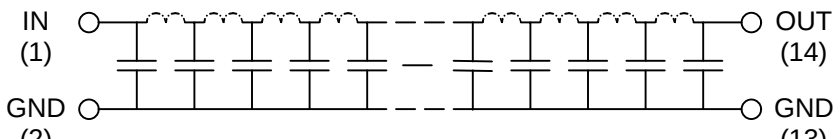
| | |
|---|---|
| IN | Signal Input |
| OUT | Signal Output |
| GND | Ground |

## SERIES SPECIFICATIONS

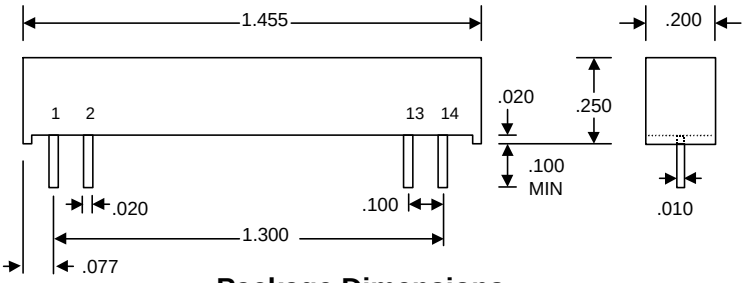
- **Dielectric breakdown:** 50 Vdc
- **Distortion @ output:** 10% max.
- **Operating temperature:** -55°C to +125°C
- **Storage temperature:** -55°C to +125°C
- **Temperature coefficient:** 100 PPM/°C

## DASH NUMBER SPECIFICATIONS

| Part Number | Delay (ns) | Impedance (Ω) | Ins. Loss (dB) | Cut-Off (MHz) |
|---|---|---|---|---|
| 1515-10A | 10 ± 1.0 | 50 | < 0.5 | 350 |
| 1515-20A | 20 ± 1.0 | 50 | < 0.5 | 175 |
| 1515-30A | 30 ± 1.5 | 50 | < 0.5 | 116 |
| 1515-40A | 40 ± 2.0 | 50 | < 0.5 | 87 |
| 1515-50A | 50 ± 2.5 | 50 | < 0.5 | 70 |
| 1515-60A | 60 ± 3.0 | 50 | < 1.0 | 58 |
| 1515-70A | 70 ± 3.5 | 50 | < 1.0 | 50 |
| 1515-80A | 80 ± 4.0 | 50 | < 1.0 | 43 |
| 1515-90A | 90 ± 4.5 | 50 | < 1.0 | 38 |
| 1515-100A | 100 ± 5.0 | 50 | < 1.0 | 35 |
| 1515-10Y | 10 ± 1.0 | 75 | < 0.5 | 350 |
| 1515-20Y | 20 ± 1.0 | 75 | < 0.5 | 175 |
| 1515-30Y | 30 ± 1.5 | 75 | < 0.5 | 116 |
| 1515-40Y | 40 ± 2.0 | 75 | < 0.5 | 87 |
| 1515-50Y | 50 ± 2.5 | 75 | < 0.5 | 70 |
| 1515-60Y | 60 ± 3.0 | 75 | < 1.0 | 58 |
| 1515-70Y | 70 ± 3.5 | 75 | < 1.0 | 50 |
| 1515-10B | 10 ± 1.0 | 100 | < 0.5 | 350 |
| 1515-20B | 20 ± 1.0 | 100 | < 0.5 | 175 |
| 1515-30B | 30 ± 1.5 | 100 | < 0.5 | 116 |
| 1515-40B | 40 ± 2.0 | 100 | < 0.5 | 87 |
| 1515-50B | 50 ± 2.5 | 100 | < 0.5 | 70 |




**Functional Diagram**




**Package Dimensions**

# PASSIVE DELAY LINE TEST SPECIFICATIONS

## TEST CONDITIONS

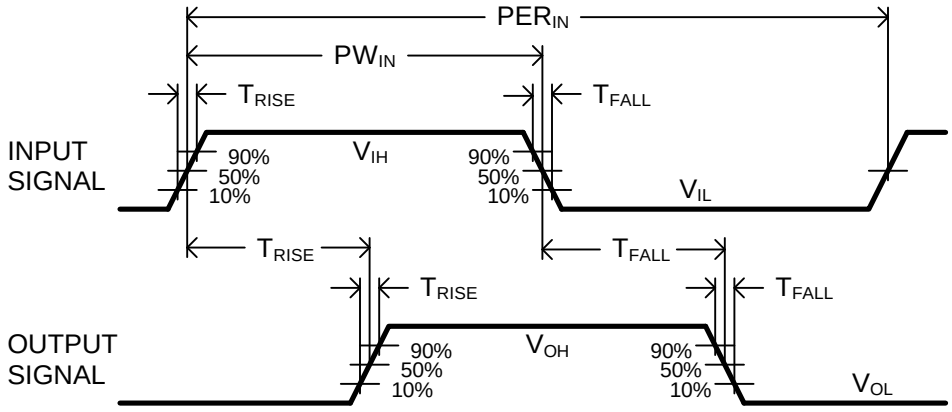
**INPUT:**

**Ambient Temperature:** 25°C ± 3°C
**Input Pulse:** High = 3.0V typical
Low = 0.0V typical
**Source Impedance:** 50Ω Max.
**Rise/Fall Time:** 3.0 ns Max. (measured at 10% and 90% levels)
**Pulse Width (TD <= 75ns):** $PW_{IN}$ = 100ns
**Period (TD <= 75ns):** $PER_{IN}$ = 1000ns
**Pulse Width (TD > 75ns):** $PW_{IN} = 2 \times T_D$
**Period (TD > 75ns):** $PER_{IN} = 10 \times T_D$

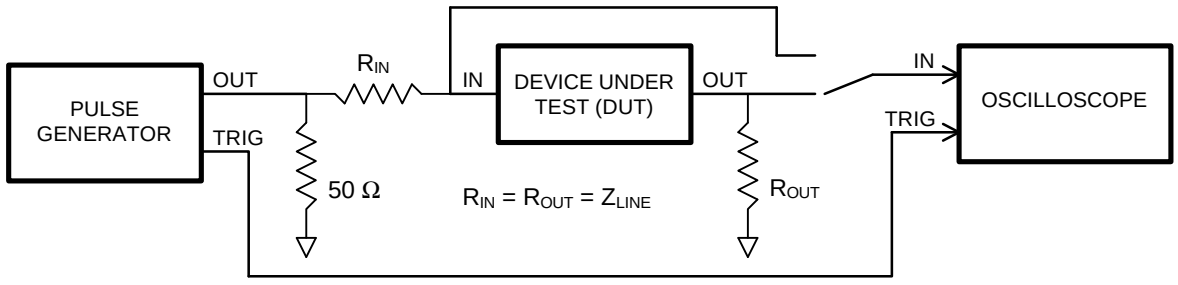
**OUTPUT:**

**$R_{load}$:** 10MΩ
**$C_{load}$:** 10pf
**Threshold:** 50% (Rising & Falling)

**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.




**Timing Diagram For Testing**




**Test Setup**