

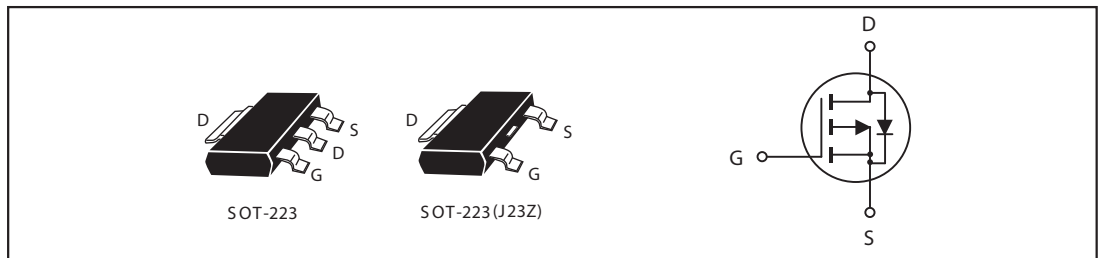


## P-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> ( mΩ ) TYP
-30V	-5.3A	52 @ V <sub>GS</sub> = -10V
		85 @ V <sub>GS</sub> = -4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- SOT-223 Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous @ T <sub>J</sub> =125 °C -Pulsed <sup>a</sup>	I <sub>D</sub>	-5.3	A
	I <sub>DM</sub>	-16	A
Drain-Source Diode Forward Current	I <sub>S</sub>	5.3	A
Maximum Power Dissipation @ T <sub>C</sub> =25 °C Derate above 25 °C	P <sub>D</sub>	3	W
		0.08	W/ °C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R θ <sub>JC</sub>	12	°C/W
Thermal Resistance, Junction-to-Ambient	R θ <sub>JA</sub>	42	°C/W

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ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250uA	-1	-1.5	-3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> =-5.3A		52	65	m ohm
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.2A		85	100	m ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -10V	-16			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -10V, I <sub>D</sub> = - 5.3A		-7		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> = 0V f=1.0MHz		860		pF
Output Capacitance	C <sub>OSS</sub>			470		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			180		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>D</sub> = -15V, I <sub>D</sub> = -1A, V <sub>GEN</sub> = - 10V, R <sub>GEN</sub> = 6 ohm		9	20	ns
Rise Time	t <sub>r</sub>			10	40	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			37	90	ns
Fall Time	t <sub>f</sub>			23	110	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> = -5.3A, V <sub>GS</sub> =-10V		15	20	nC
		V <sub>DS</sub> =-15V, I <sub>D</sub> = -5.3A, V <sub>GS</sub> =-4.5V		8.8	10.6	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> = -5.3A, V <sub>GS</sub> =-10V		3		nC
Gate-Drain Charge	Q <sub>gd</sub>			4		nC

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS <sup>b</sup>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = -5.3A$		-0.84	-1.3	V

### Notes

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

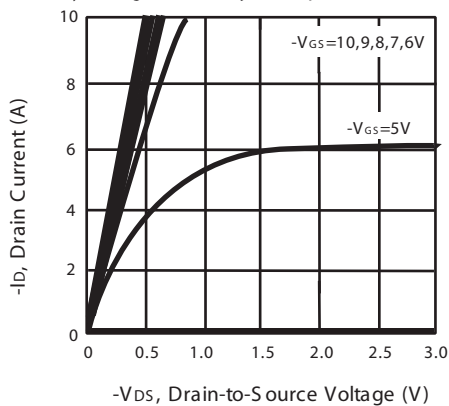


Figure 1. Output Characteristics

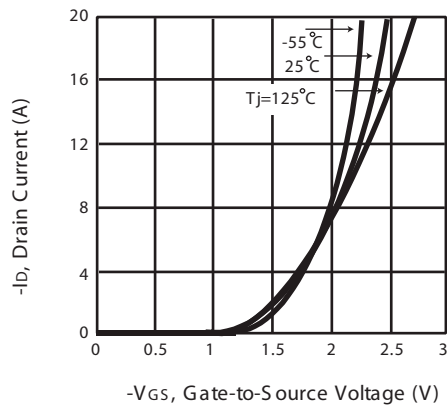


Figure 2. Transfer Characteristics

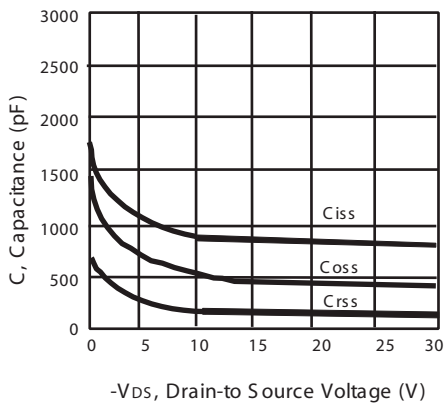


Figure 3. Capacitance

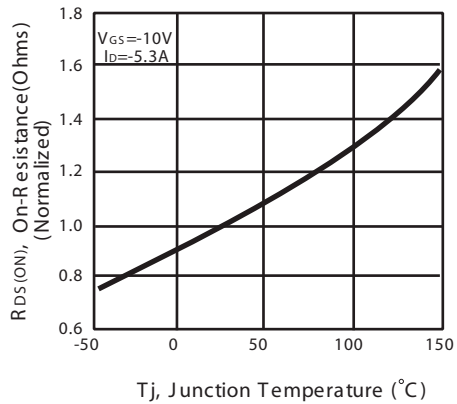


Figure 4. On-Resistance Variation with Temperature

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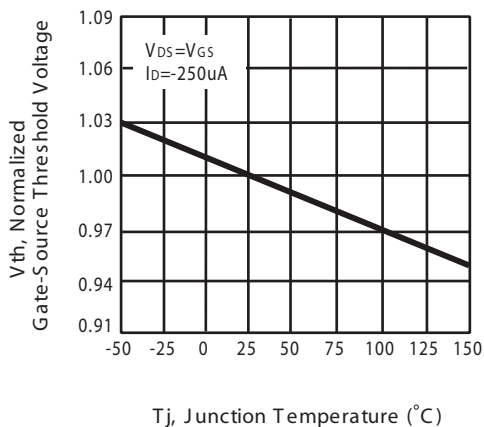


Figure 5. Gate Threshold Variation with Temperature

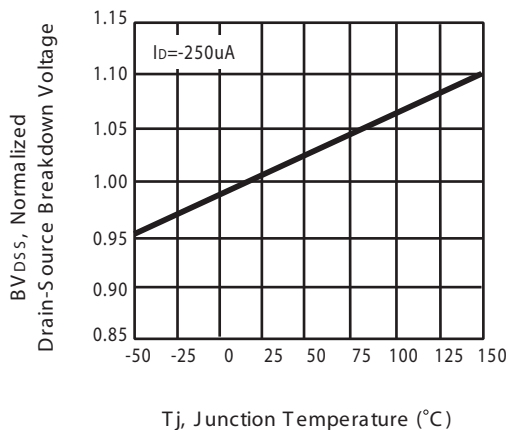


Figure 6. Breakdown Voltage Variation with Temperature

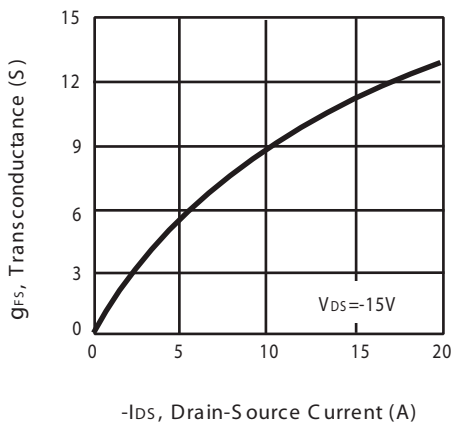


Figure 7. Transconductance Variation with Drain Current

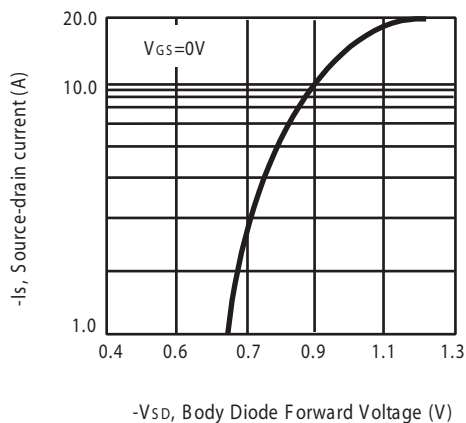


Figure 8. Body Diode Forward Voltage Variation with Source Current

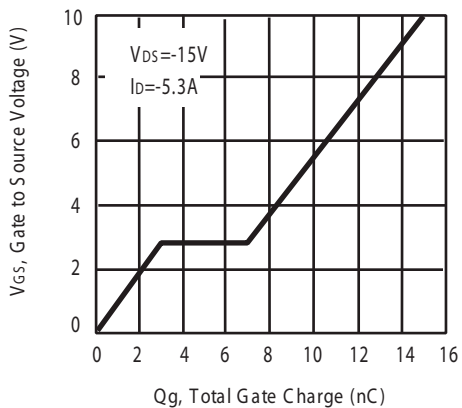


Figure 9. Gate Charge

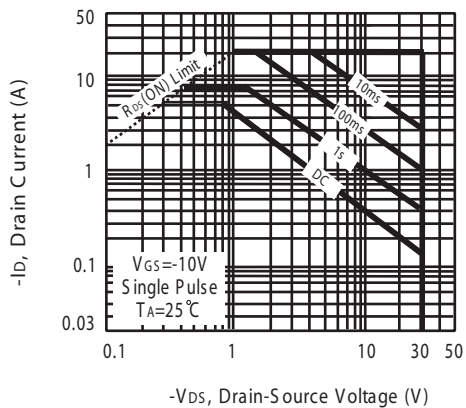


Figure 10. Maximum Safe Operating Area

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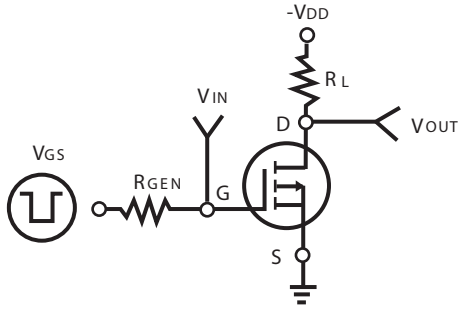


Figure 11. Switching Test Circuit

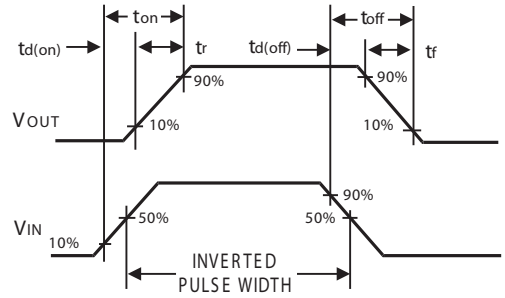


Figure 12. Switching Waveforms

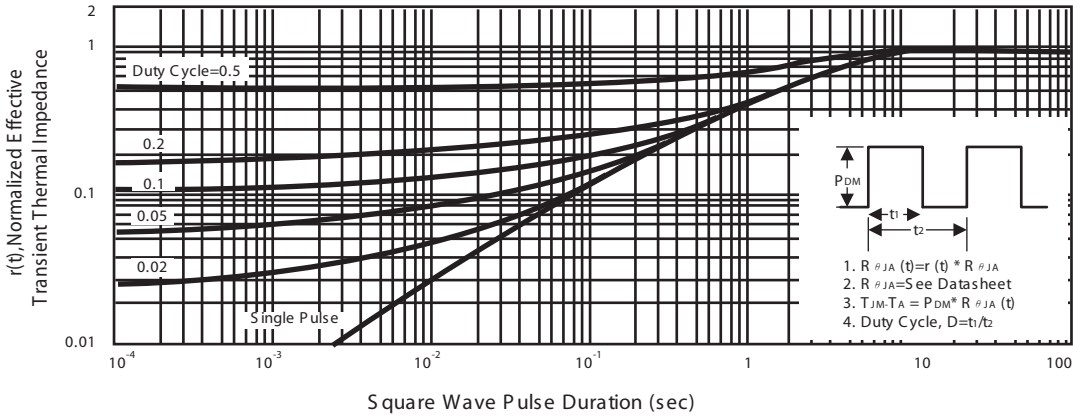


Figure 13. Normalized Thermal Transient Impedance Curve