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NTE2056
Integrated Circuit
8–Bit Multiplying Digital–to–Analog Converter

Description:

The NTE2056 is an 8–bit multiplying D–to–A converter in a 16–Lead DIP type package designed for use where the output current is a linear product of an eight–bit digital word and an analog input voltage.

Features:

- Fast Setting Time: 300ns Typ
- Non–Inverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing: +0.4V to –5.0V
- High–Speed Multipling Input: Slew Rate 4.0mA/μs
- Standard Supply Voltages: +5.0V and –5.0V to –15V

Applications:

- Tracking A–to–D Converters
- Successive Approximation A–to–D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog–Digital Multiplication
- Digital–Digital Multiplication
- Analog–Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Power Supply Voltage
- V_{CC} . . . . . +5.5V
- V_{EE} . . . . . –16.5V

Digital Input Voltage, V_5 thru V_{12} . . . . . 0 to +5.5V

Applied Output Voltage, V_O . . . . . +0.5V, –5.2V

Reference Current, I_{14} 5mA

Reference Amplifier Inputs
- V_{14} . . . . . V_{CC}
- V_{15} . . . . . V_{EE}

Operating Temperature Range, T_A . . . . . 0° to +75°C

Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Electrical Characteristics: (T_A = 0° to +75°C, V_{CC} = +5V, V_{EE} = –15V, V_{ref}/R14 = 2mA, All digital inputs at high logic level, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O)	E_r	Note 1		–	–	±0.78	%
Setting Time to within ±1/2 LSB (Includes t_{PLH})	t_S	T_A = +25°C, Note 2		–	300	–	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	T_A = +25°C		–	30	100	ns
Output Full Scale Current Drift	TCI_O			–	–20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1"	V_{IH}			2.0	–	–	V
Low Level, Logic "0"	V_{IL}			–	–	0.8	V
Digital Input Current (MSB) High Level	I_{IH}	V_{IH} = 5V		–	0	0.04	mA
Low Level	I_{IL}	V_{IL} = 0.8V		–	–0.4	–0.8	mA
Reference Input Bias Current (Pin15)	I_{15}			–	–1.0	–5.0	µA
Output Current Range	I_{OR}	V_{EE} = –5V		0	2.0	2.1	mA
		V_{EE} = –15V, T_A = +25°C		0	2.0	4.2	mA
Output Current	I_O	V_{ref} = 2.000V, R14 = 1000Ω		1.9	1.99	2.1	mA
	$I_{O\ (min)}$	All bits low		–	0	4.0	µA
Output Voltage Compliance	V_O	$E_r \leq 0.19\%$, T_A = +25°C	Pin1 Grounded	–	–	–0.55, +0.4	V
			Pin1 Open, V_{EE} below –10V	–	–	–5.0, +0.4	V
Reference Current Slew Rate	SR I_{ref}			–	4.0	–	mA/µs
Output Current Power Supply Sensitivity	PSRR(–)			–	0.5	2.7	µA/V
Power Supply Current	I_{CC}	All bits low		–	+13.5	+22.0	mA
	I_{EE}			–	–7.5	–13.0	mA
Power Supply Voltage Range	V_{CCR}	T_A = +25°C		+4.5	+5.0	+5.5	V
	V_{EER}			–4.5	–15.0	–16.5	V
Power Dissipation All bits low	P_D	V_{EE} = –5V		–	105	170	mW
		V_{EE} = –15V		–	190	305	mW
All bits high		V_{EE} = –5V		–	90	–	mW
		V_{EE} = –15V		–	160	–	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current.

Note 2. All bits switched.

Pin Connection Diagram