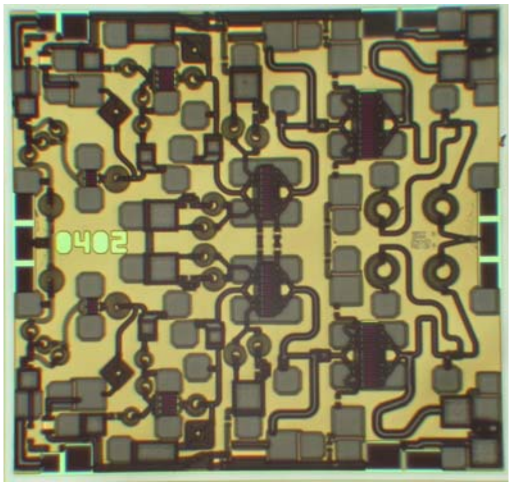
Amplifier, Power, 2W
7.1-11.7 GHz

MAAPGM0069-DIE
Rev B
Preliminary Datasheet

Features

- **2 Watt Saturated Output Power Level**
- **Variable Drain Voltage (6-10V) Operation**
- **MSAG® Process**



Description

The MAAPGM0069-DIE is a 4-stage 2 W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- **Point-to-Point Radio**
  - **7, 8 and 11 GHz Bands**

Electrical Characteristics: $T_B = 30°C^1$, $Z_0 = 50\ \Omega$, $V_{DD} = 8V$, $I_{DQ} = 760mA^2$, $P_{in} = 4$ dBm, $R_G = 100\ \Omega$

Parameter	Symbol	Typical	Units
Bandwidth	f	7.1-11.7	GHz
Output Power	P_{OUT}	33	dBm
1-dB Compression Point	P1dB	32	dBm
Power Added Efficiency	PAE	27	%
Small Signal Gain	G	34	dB
Input VSWR	VSWR	1.8:1	
Output VSWR	VSWR	2.0:1	
Gate Current	I_{GG}	2	mA
Drain Current	I_{DD}	960	mA
Output Third Order Intercept	TOI	44	dBm
Output Third Order Intermod, P_{out} = 25 dBm (DCL)	IM3	45	dBc

1. **T_B = MMIC Base Temperature**
2. **Adjust V_{GG} between –2.6 and –1.2V to achieve specified Idq.**

Maximum Ratings[3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	13.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	1.22	A
Quiescent DC Power Dissipated (No RF)	P_{DISS}	8.1	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[4]

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	6.0	8.0	10.0	V
Gate Voltage	V_{GG}	-2.6	-2.0	-1.2	V
Input Power	P_{IN}		8.0	10.0	dBm
Thermal Resistance	Θ_{JC}		11.7		°C/W
MMIC Base Temperature	T_B			Note 5	°C

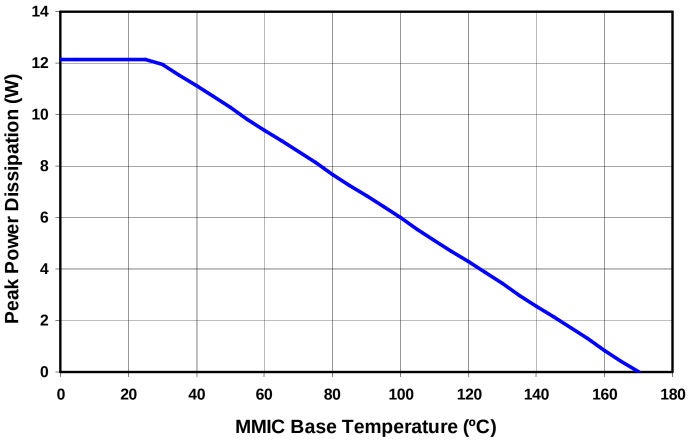
4. Operation outside of these ranges may reduce product reliability.
5. MMIC Base Temperature = 170°C — Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2.7 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8.0 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –2.0 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.

Power Derating Curve, Quiescent (No RF)



All Data is at 30ºC MMIC base temperature, CW stimulus, unless otherwise noted.

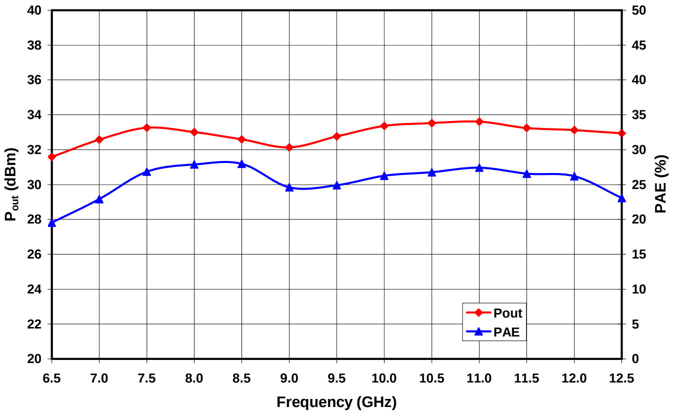


Figure 1. Output Power and Power Added Efficiency at V_D = 8V, P_{in} = 4dBm, and 25% IDSS

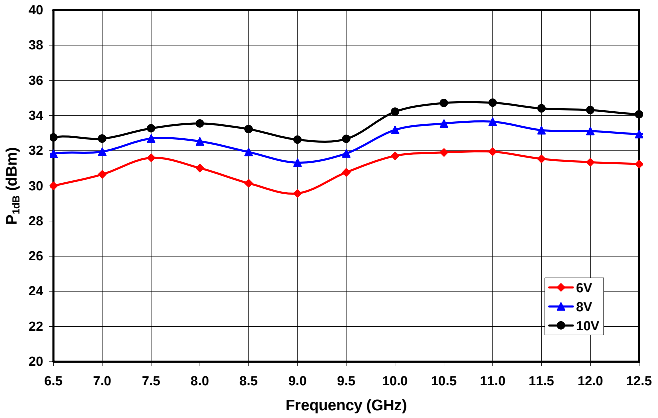


Figure 2. 1dB Compression Point and Drain Voltage at 25% IDSS

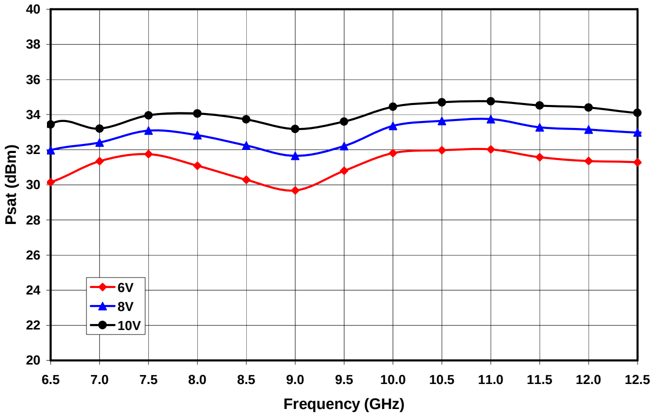


Figure 3. Saturated Output Power and Drain Voltage at 25% IDSS

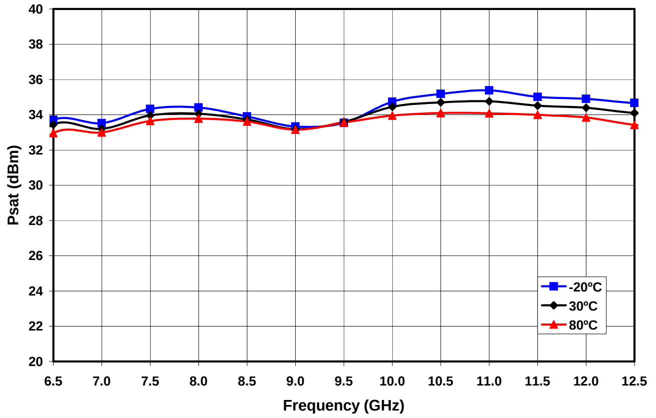


Figure 4. Saturated Output Power and Temperature at 8V and 25% IDSS

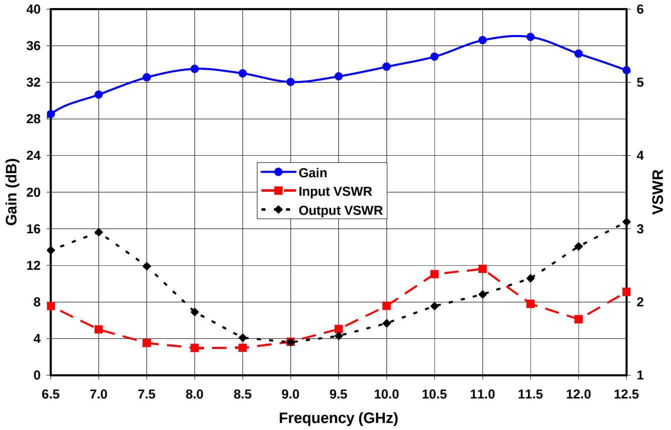


Figure 5. Small Signal Gain and Input and Output VSWR at 25% IDSS, V_D = 8V

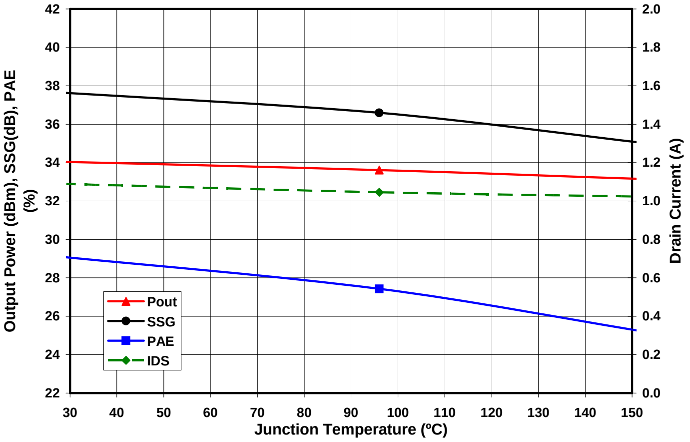


Figure 6. Output Power, Small Signal Gain, Power Added Efficiency, and Drain Current vs. Junction Temperature at 8V, 11 GHz, and 25% IDSS

All Data is at 40ºC MMIC base temperature, CW stimulus, unless otherwise noted.

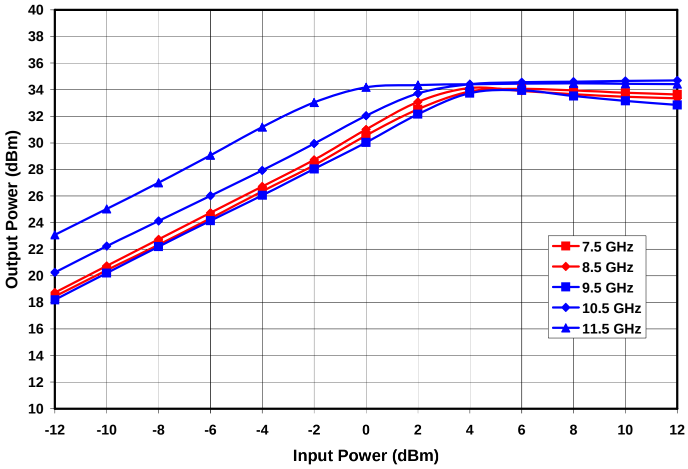


Figure 7. Output Power vs. Input Power and Frequency at 10V and 25% IDSS

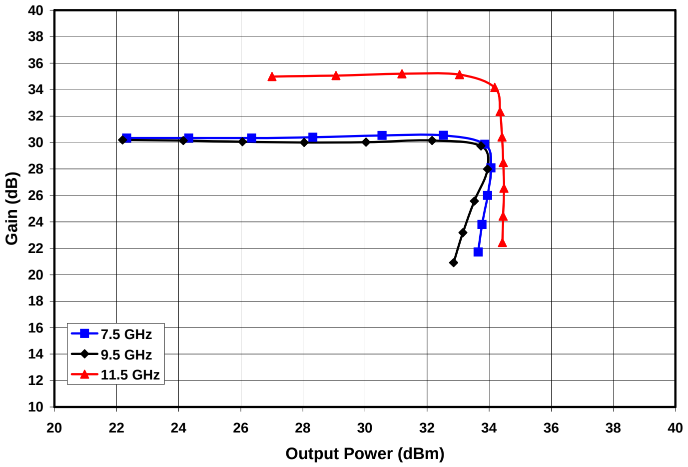


Figure 8. Gain vs. Output Power and Frequency at 10V and 25% IDSS

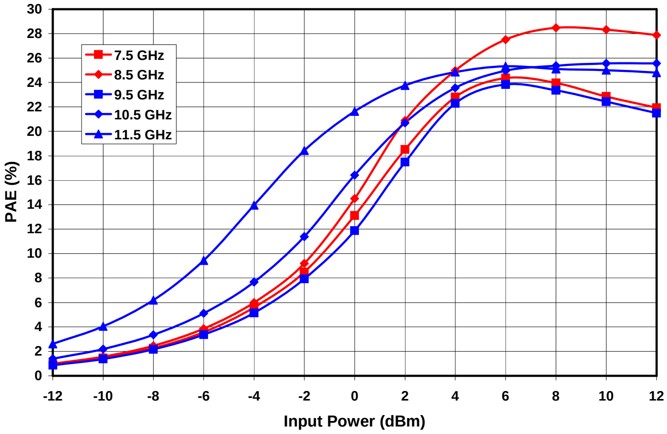


Figure 9. Power Added Efficiency vs. Input Power and Frequency at 10V and 25% IDSS

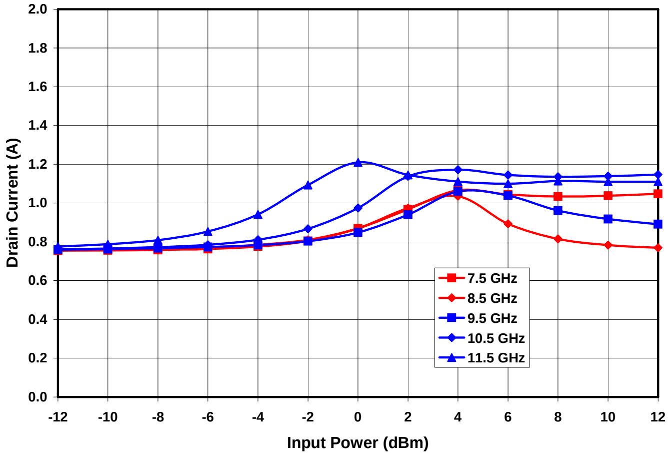


Figure 10. Drain Current vs. Input Power and Frequency at 10V and 25% IDSS

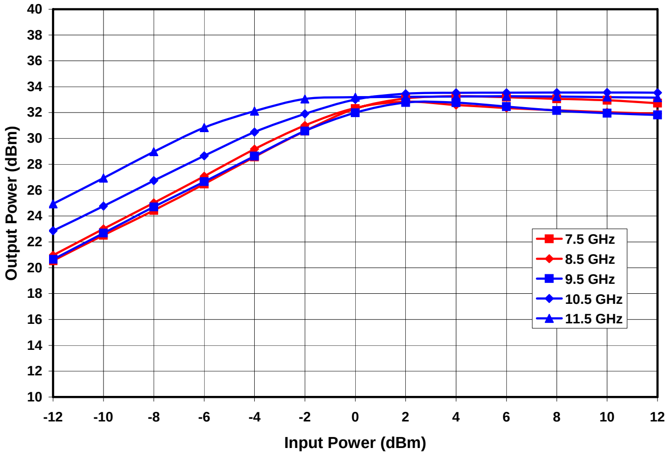


Figure 11. Output Power vs. Input Power and Frequency at 8V and 25% IDSS

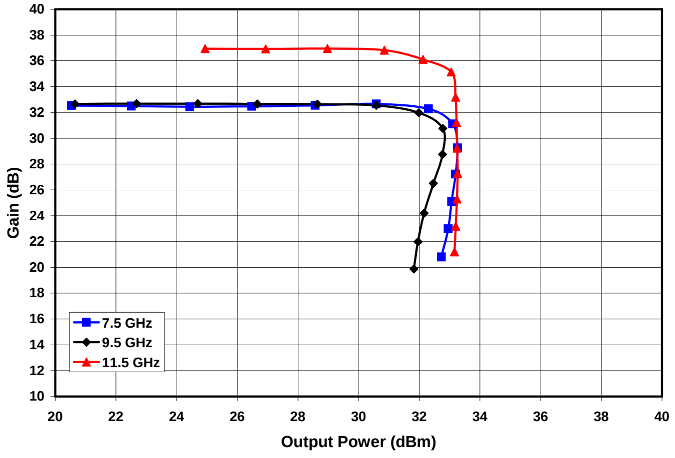


Figure 12. Gain vs. Output Power and Frequency at 8V and 25% IDSS

All Data is at 30ºC MMIC base temperature, CW stimulus, unless otherwise noted.

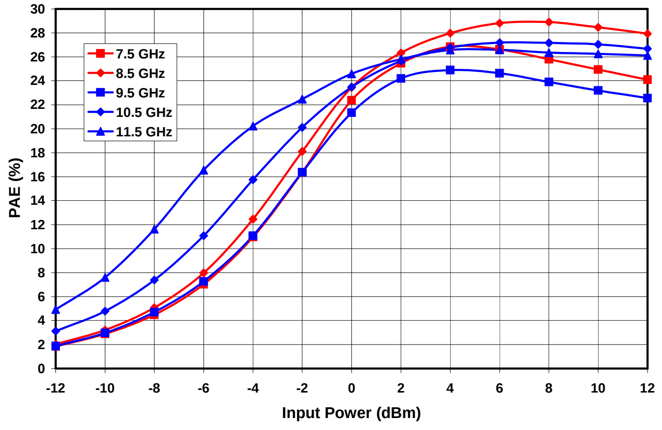


Figure 13. Power Added Efficiency vs. Input Power and Frequency at 8V and 25% IDSS

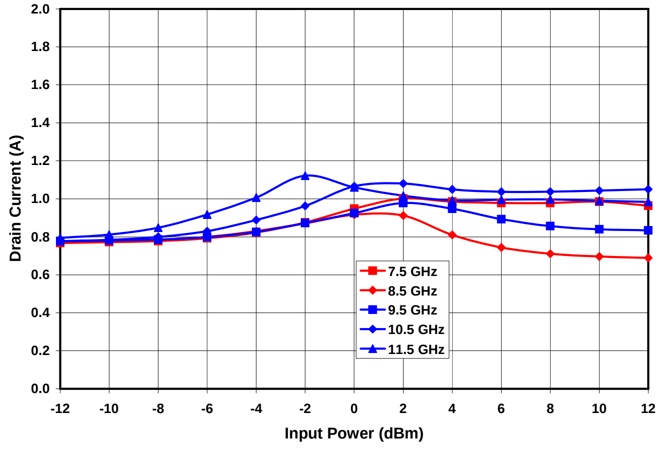


Figure 14. Drain Current vs. Input Power and Frequency at 8V and 25% IDSS

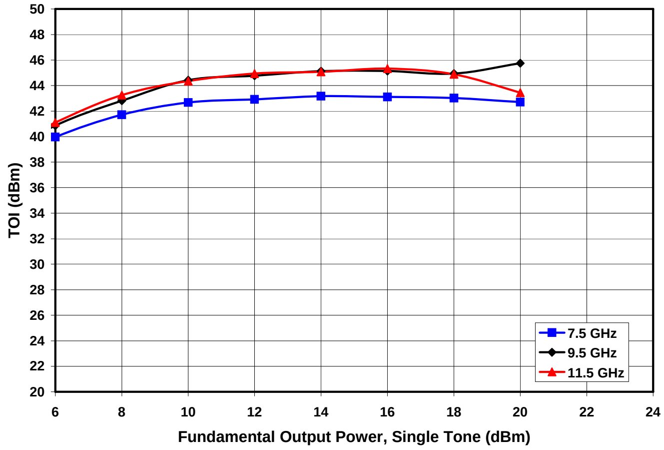


Figure 15. Third Order Intercept vs. Output Power and Frequency at 6V.

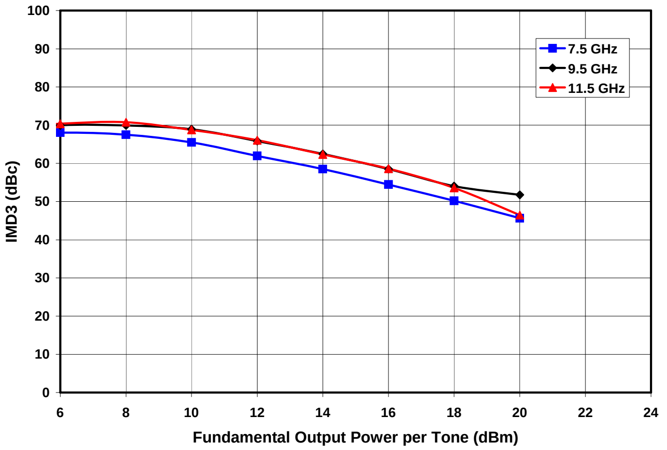


Figure 16. Third Order Intermod vs. Output Power and Frequency at 6V.

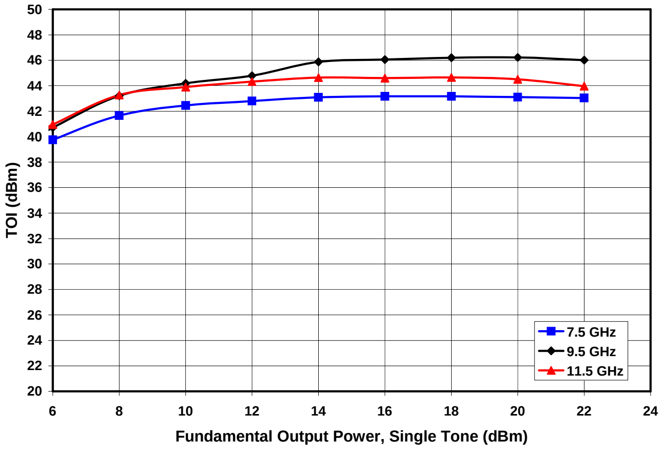


Figure 17. Third Order Intercept vs. Output Power and Frequency at 8V.

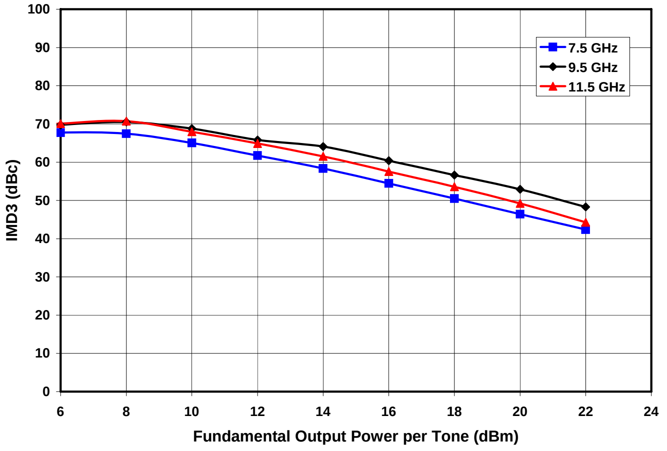


Figure 18. Third Order Intermod vs. Output Power and Frequency at 8V.

All Data is at 30ºC MMIC base temperature, CW stimulus, unless otherwise noted.

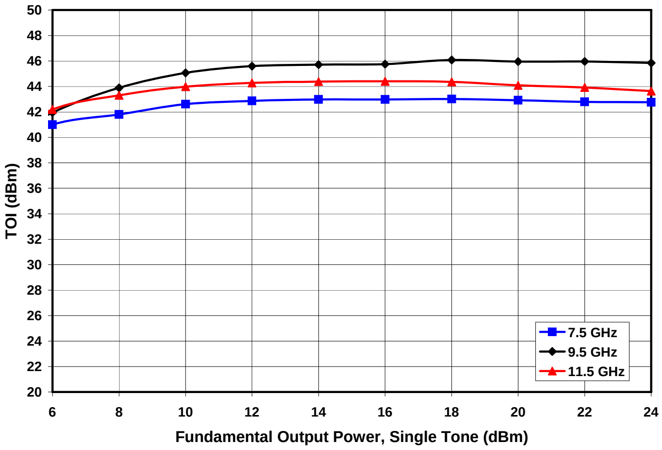


Figure 19. Third Order Intercept vs. Output Power and Frequency at 10V.

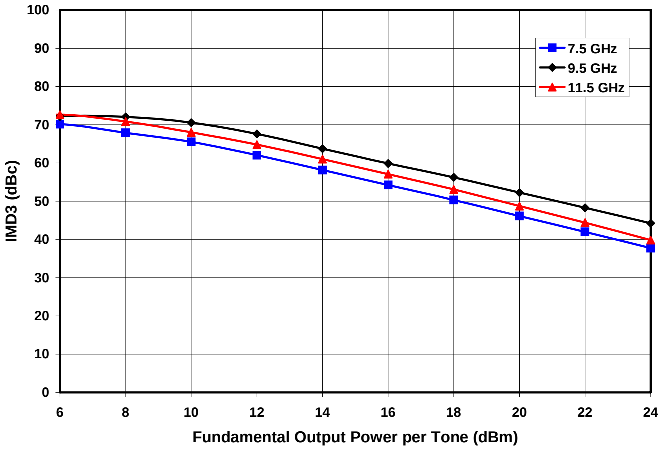


Figure 20. Third Order Intermod vs. Output Power and Frequency at 10V.

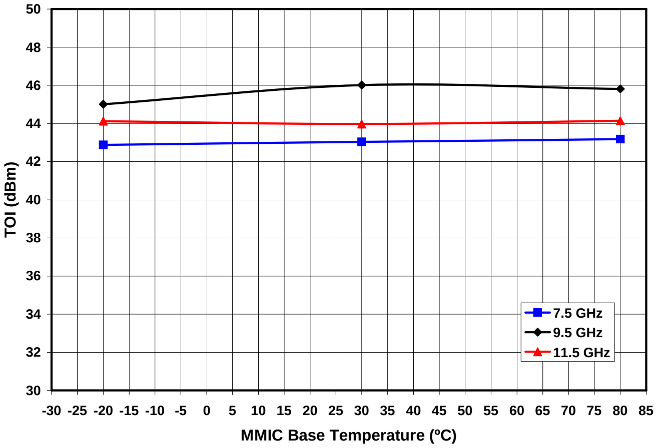


Figure 21. Third Order Intercept vs. Temperature and Frequency at 8V and P_{out} = 25 dBm DCL.

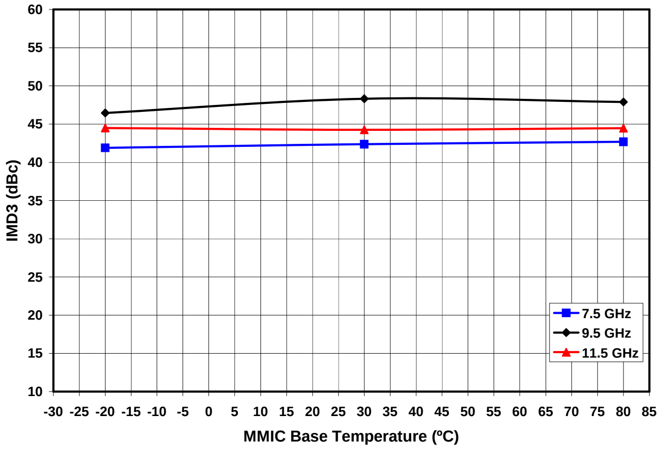


Figure 22. Third Order Intermod vs. Temperature and Frequency at 8V and P_{out} = 25 dBm DCL.

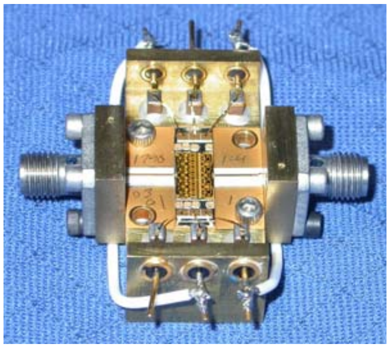
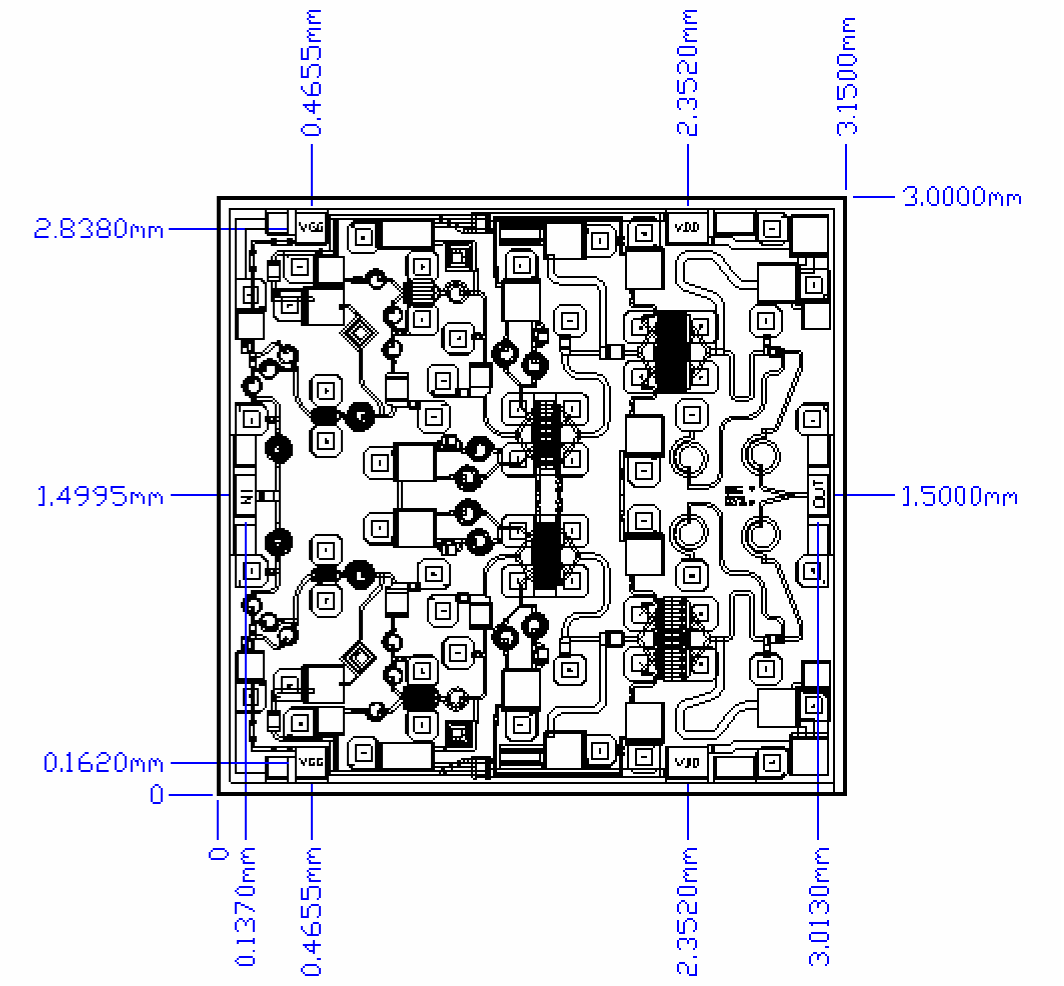


Figure 21. Fixture used to characterize MAAPGM0069-DIE under CW stimulus.

Mechanical Information

Chip Size: 3.000 x 3.150 x 0.075 mm (118 x 124 x 3 mils)



Chip edge to bond pad dimensions are shown to the center of the bond pad.

Figure 22. Die Layout

Bond Pad Dimensions

Pad	Size (μm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VDD	200 x 150	8 x 6
DC Gate Supply Voltage VGG	150 x 150	6 x 6

Assembly and Bonding Diagram

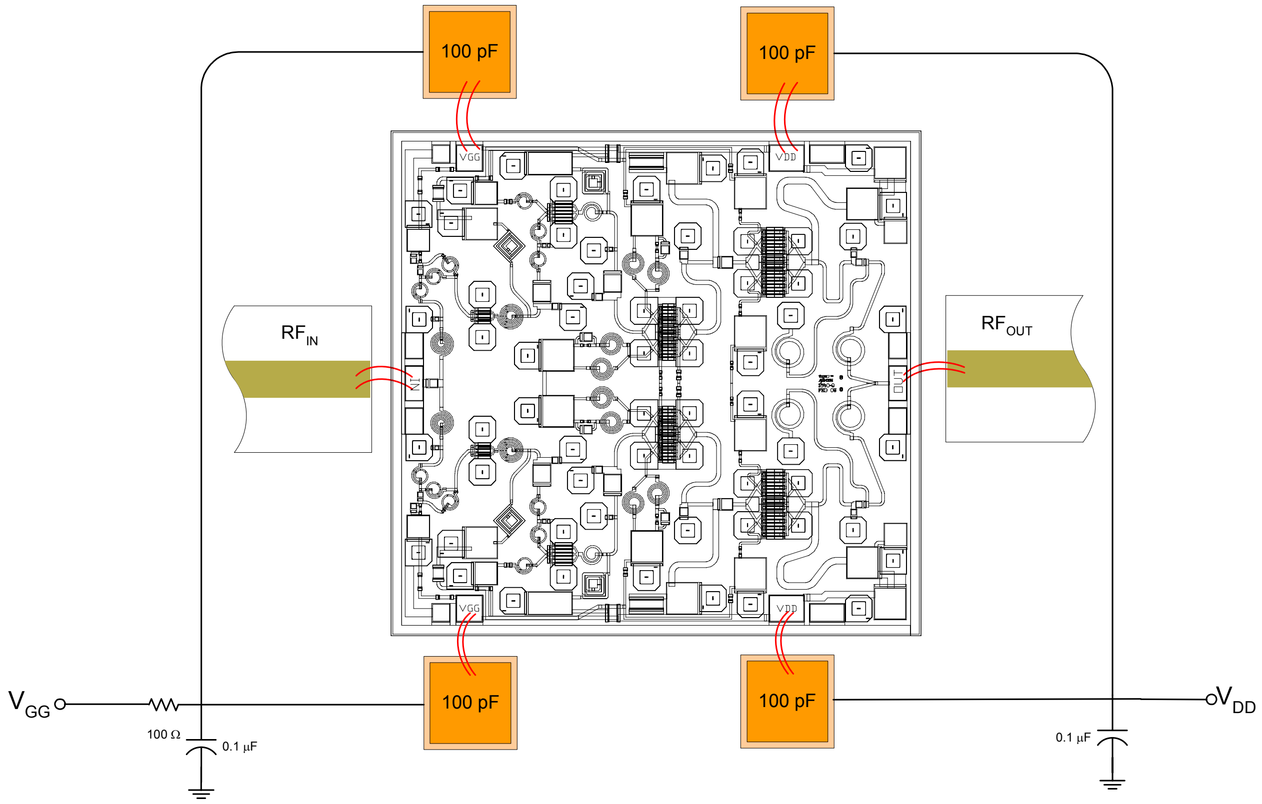


Figure 23. Recommended operational configuration. Wire bond as shown.

Die Handling:

Refer to Application Note AN3016.

Assembly Instructions:

Die Attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 310 °C to less than 7 minutes. Refer to Application Note AN3017 for more detailed information.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

ATTENTION
Static-Sensitive Devices
Handling Precautions Required

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.