Integrated Circuit Systems, Inc.

ICS93776

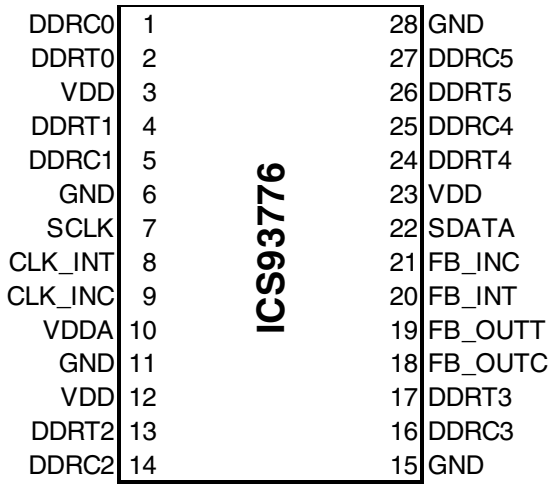
Low Cost DDR Phase Lock Loop Zero Delay Buffer

Recommended Application:
DDR Zero Delay Clock Buffer

Product Description/Features:
- Low skew, low jitter PLL clock driver
- Max frequency supported = 266MHz (DDR 533)
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- 3.3V tolerant CLK_INT/C input

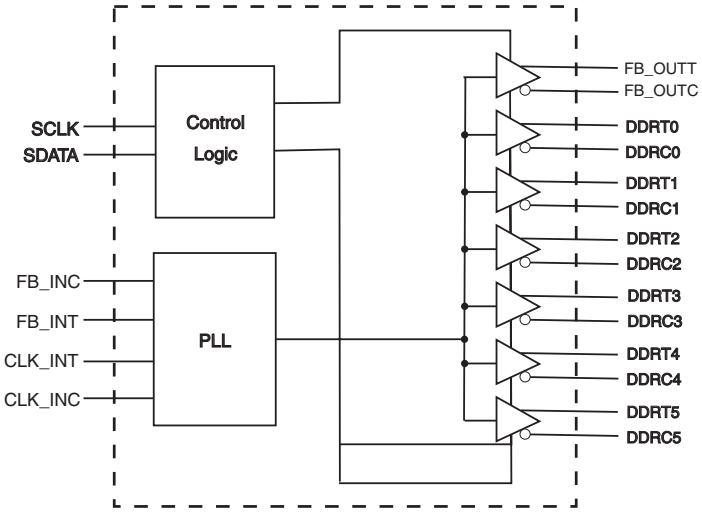
Switching Characteristics:
- CYCLE - CYCLE jitter: <100ps
- OUTPUT - OUTPUT skew: <100ps
- DUTY CYCLE: 48% - 52%

Pin Configuration



28-Pin 209mil SSOP

Block Diagram



Functionality

INPUTS		OUTPUTS			PLL State
AVDD	CLK_INT	CLKT	CLKC	FB_OUTT	
2.5V (nom)	L	L	H	L	on
2.5V (nom)	H	H	L	H	on

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	DDRC0	OUT	"Complementary" Clock of differential pair output.
2	DDRT0	OUT	"True" Clock of differential pair output.
3	VDD	PWR	Power supply, nominal 2.5V
4	DDRT1	OUT	"True" Clock of differential pair output.
5	DDRC1	OUT	"Complementary" Clock of differential pair output.
6	GND	PWR	Ground pin.
7	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
8	CLK_INT	IN	"True" reference clock input.
9	CLK_INC	IN	"Complementary" reference clock input.
10	VDDA	PWR	2.5V power for the PLL core.
11	GND	PWR	Ground pin.
12	VDD	PWR	Power supply, nominal 2.5V
13	DDRT2	OUT	"True" Clock of differential pair output.
14	DDRC2	OUT	"Complementary" Clock of differential pair output.
15	GND	PWR	Ground pin.
16	DDRC3	OUT	"Complementary" Clock of differential pair output.
17	DDRT3	OUT	"True" Clock of differential pair output.
18	FB_OUTC	OUT	Complement single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs, This output must be connect to FB_INC.
19	FB_OUTT	OUT	True single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs, This output must be connect to FB_INT.
20	FB_INT	IN	True single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INT to eliminate phase error.
21	FB_INC	IN	Complement single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INT to eliminate phase error.
22	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
23	VDD	PWR	Power supply, nominal 2.5V
24	DDRT4	OUT	"True" Clock of differential pair output.
25	DDRC4	OUT	"Complementary" Clock of differential pair output.
26	DDRT5	OUT	"True" Clock of differential pair output.
27	DDRC5	OUT	"Complementary" Clock of differential pair output.
28	GND	PWR	Ground pin.

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input / Supply / Common Output parameters

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5}$	R_T = 120W, C_L = 12 pF at 100MHz			300	mA
		R_T = 120W, C_L = 12 pF at 133MHz			300	
	I_{DDPD}	CL=0 pF			100	mA
Output High Current	I_{OH}	V_{DD} = 2.5V, V_{OUT} = 1V	-48		-29	mA
Output Low Current	I_{OL}	V_{DD} = 2.5V, V_{OUT} = 1.2V	29		37	mA
High Impedance Ouptut Current	I_{OZ}	V_{DD} = 2.7V, V_{OUT} = V_{DD} or GND			10	mA
High-level Output Voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1mA	2			V
		V_{DD} = 2.3V, I_{OH} = -12mA				
Low-level Output Voltage	V_{OL}	V_{DD} = min to max, I_{OH} = 1mA			0.1	V
		V_{DD} = 2.3V, I_{OH} = 12mA			0.4	
Output Capacitance[1]	C_{OUT}	V_I = V_{DD} or GND				pF

1. Guaranteed by design, not 100% tested in production.

Recommended Operation Conditions

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog / Core Supply Voltage	AV_{DD}		2.3		2.7	V
Input Voltage Level	V_{IN}		2		3	V

Timing Requirements

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Clock Frequency[1]	$freq_{op}$	Input Voltage level: 0-2.50V	22		340	MHz
Input Clock Duty Cycle[1]	d_{tin}		40	50	60	%
Clock Stabilization[1]	t_{STAB}	from VDD = 2.5V to 1% target frequency			100	µs

1. Guaranteed by design, not 100% tested in production.

Switching Characteristics

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.50V ± 0.20V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle to cycle Jitter[1,2]	t_{c-c}	66 MHz to 266 MHz			100	ps
Phase Error[1]	t_{pe}		-150		150	ps
Output to output Skew[1]	T_{skew}				100	ps
Duty Cycle (Sign Ended)[1,3]	DC	66 MHz to 267 MHz	48		52	%
Rise Time, Fall Time[4]	t_R , t_f	Load=120Ω/14pF			950	ps
Output Differential Pair Crossing Voltage	V_{OC}	V_{DD}=2.50V	1.23		1.32	V

1. Guaranteed by design, not 100% tested in production.
2. Refers to transistion on non-inverting period.
3. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formular: duty_cycle=t_{wH}/t_C, where the cycle time (t_C)decreases as the frequency increases.

General SMBus serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D5 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D4(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D4(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D5(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

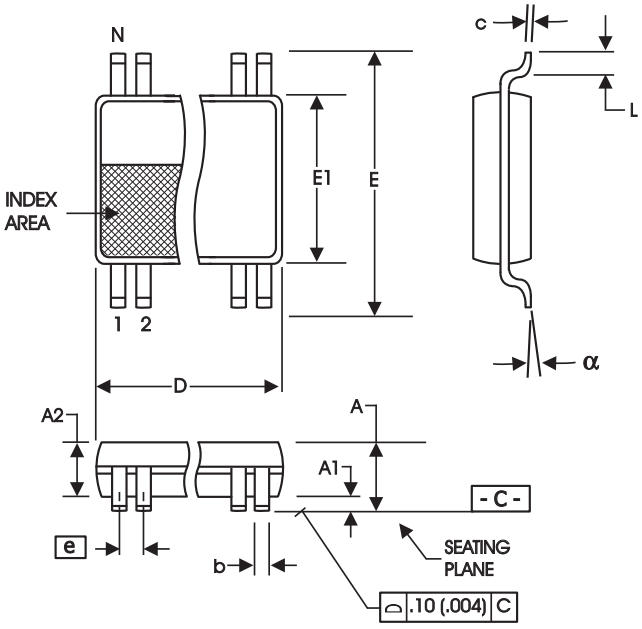
Bytes 2 to 6 are reseved power up default = 1. This allows operation with main clock.

BYTE 0	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	2, 1	DDR0(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 6	4, 5	DDR1(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 5	-	-	Reserved	X	-	-	1
Bit 4	-	-	Reserved	X	-	-	1
Bit 3	13, 14	DDR2(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 2	26, 27	DDR5(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 1	-	-	Reserved	X	-	-	1
Bit 0	24, 25	DDR4(T&C)	Output Control	RW	DISABLE	ENABLE	1

Note: PWD = Power Up Default

BYTE 1	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	Reserved	X	-	-	1
Bit 6	16,17	DDR3(T&C)	Output Control	RW	DISABLE	ENABLE	1
Bit 5	-	-	Reserved	X	-	-	0
Bit 4	-	-	Reserved	X	-	-	0
Bit 3	-	-	Reserved	RW	-	-	0
Bit 2	-	-	Reserved	X	-	-	0
Bit 1	-	-	Reserved	RW	-	-	0
Bit 0	-	-	Reserved	X	-	-	0

Note: PWD = Power Up Default



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

Ordering Information

ICS93776yFLF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0793A—03/08/05

Revision History

Rev.	Issue Date	Description	Page #
N/A	8/12/2004	Updated I2c	6
N/A	8/20/2004	Updated I2c	6