



**GENERAL DESCRIPTION**



The ICS810001-21 is a member of the HiperClockS™ family of high performance clock solutions from ICS. The ICS810001-21 is a PLL based synchronous clock generator that is optimized for digital video clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation, and to support the complex PLL multiplication ratios needed for video rate conversion. The second stage is a FemtoClock frequency multiplier that provides the low jitter, high frequency video output clock.

Preset multiplication ratios are selected from internal lookup tables using device input selection pins. The multiplication ratios are optimized to support most common video rates used in professional video system applications. The VCXO requires the use of an external, inexpensive pullable crystal. Two crystal connections are provided (pin selectable) so that both 60 and 59.94 base frame rates can be supported. The VCXO requires external passive loop filter components which are used to set the PLL loop bandwidth and damping characteristics.

**FEATURES**

- Accepts various HD and SD references including hsync, transport and pixel clock rates
- Outputs HD and SD pixel rates
- One LVCMOS/LVTTL PLL clock output
- Two selectable LVCMOS/LVTTL input clocks
- LVCMOS input select lines
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking
- FemtoClock frequency multiplier provides low jitter, high frequency output
- FemtoClock range: 560MHz - 700MHz
- RMS phase jitter @ 148.3516484MHz, using a 26.973027MHz crystal (12kHz - 20MHz): 0.81ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature

**OUTPUT RATES SUPPORTED:**

Frequency (MHz)	Application
27MHz	MPEG Transport, ITU-R601, CCIR 656
26.973027MHz	27MHz x 1000/1001
74.25MHz	SMPTE 292M/60
74.17582418MHz	SMPTE 292M/59.94
148.5MHz	SMPTE 292M/60, 1080P
148.3516484MHz	SMPTE 292M/59.94, 1080P
36MHz	SMPTE 259M Level "D"

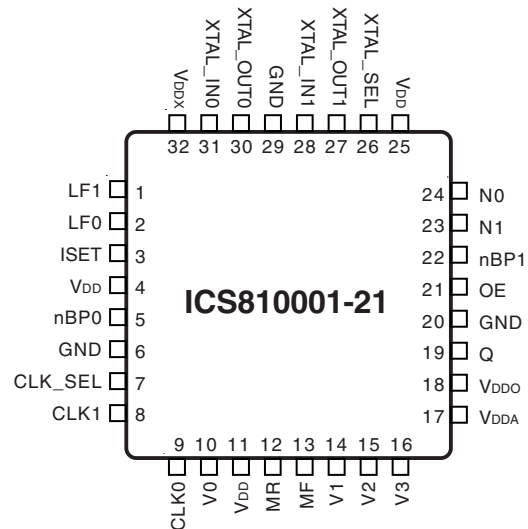
**EXAMPLE FREQUENCY CONVERSIONS:**

All nine combinations from / to:

- 27MHz
- 74.175MHz
- 74.25MHz

NTSC or PAL hsync to 27MHz  
NTSC or PAL hsync to 4xFsc

**PIN ASSIGNMENT**

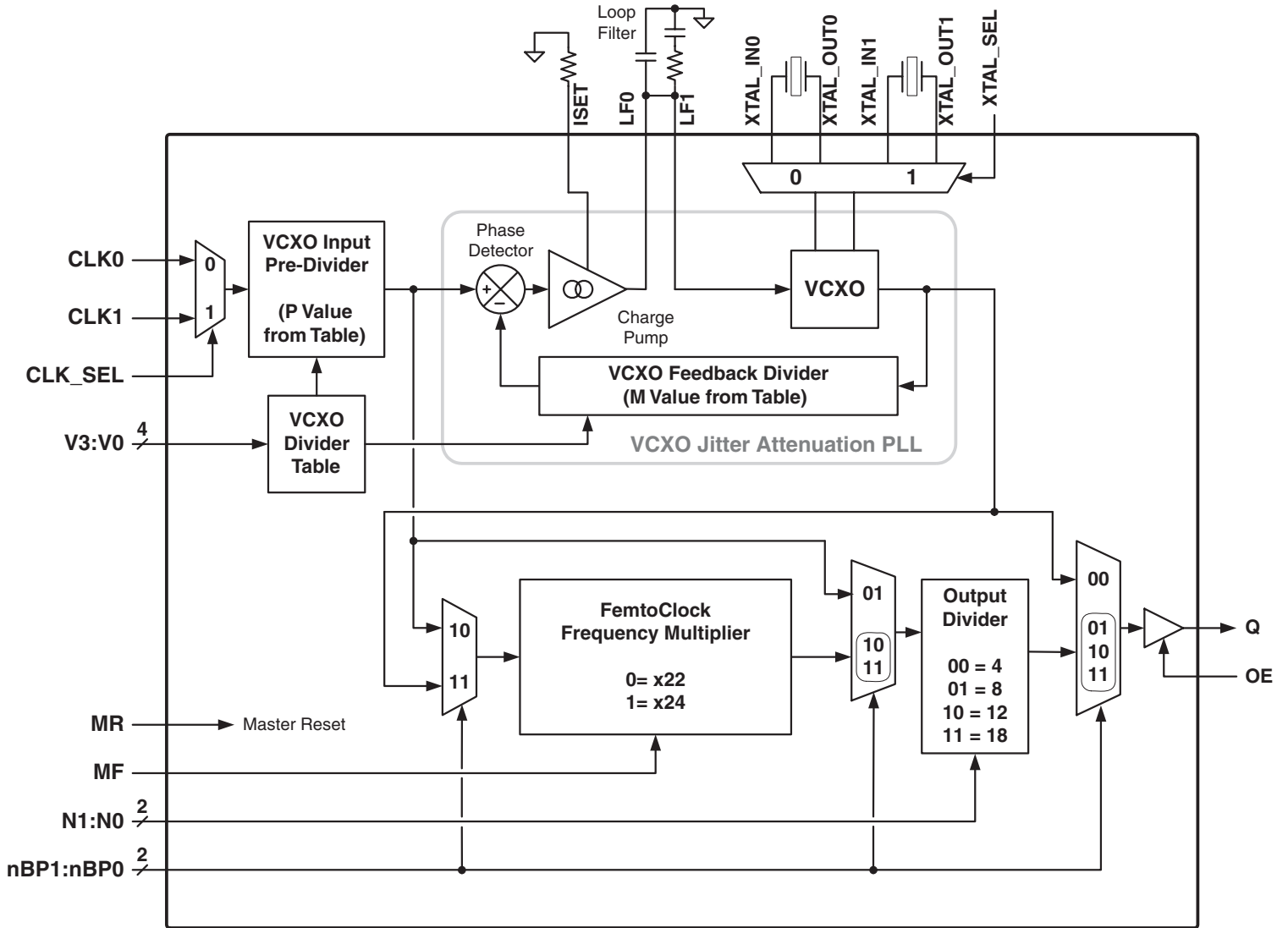


**32-Lead VFQFN**  
5mm x 5mm x 0.95 package body  
**K Package**  
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



**BLOCK DIAGRAM**





**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 11, 25	V <sub>DD</sub>	Power		Core power supply pins.
5, 22	nBP0, nBP1	Input	Pullup	PLL Bypass control pins. See block diagram.
6, 20, 29	GND	Power		Power supply ground.
7	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1. When LOW, selects CLK0. LVCMOS/LVTTL interface levels.
8, 9	CLK1, CLK0	Input	Pulldown	Clock inputs. LVCMOS/LVTTL interface levels.
10, 14, 15, 16	V0, V1, V2, V3	Input	Pulldown	VCXO PLL divider selection pins. LVCMOS/LVTTL interface levels.
12	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the output to go low. When logic LOW, the internal dividers and the output is enabled. LVCMOS / LVTTL interface levels.
13	MF	Input	Pulldown	FemtoClock multiplication factor select pin. LVCMOS/LVTTL interface levels.
17	V <sub>DDA</sub>	Power		Analog supply pin.
18	V <sub>DDO</sub>	Power		Output power supply pin.
19	Q	Output		VCXO PLL clock output. LVCMOS/LVTTL interface levels.
21	OE	Input	Pullup	Output enable. When logic LOW, the clock output is in tristate. When logic HIGH, the output is enabled. LVCMOS/LVTTL interface levels.
23, 24	N1, N0	Input	Pulldown	FemtoClock output divide select. LVCMOS/LVTTL interface levels.
26	XTAL_SEL	Input	Pulldown	Crystal select. When HIGH, selects XTAL1. When LOW, selects XTAL0. LVCMOS/LVTTL interface levels.
27, 28	XTAL_OUT1, XTAL_IN1	Input		Crystal oscillator interface. XTAL_IN1 is the input. XTAL_OUT1 is the output.
30, 31	XTAL_OUT0, XTAL_IN0	Input		Crystal oscillator interface. XTAL_IN0 is the input. XTAL_OUT0 is the output.
32	V <sub>DDX</sub>	Power		Power supply pin for VCXO charge pump.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DD</sub> , V <sub>DDA</sub> , V <sub>DDO</sub> = 3.465V		TBD		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ



Integrated  
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Systems, Inc.

**PRELIMINARY**

**ICS810001-21**  
FEMTOCLOCKS™ DUAL VCXO VIDEO PLL

**TABLE 3A. FIRST FREQUENCY TRANSLATION STAGE: VCXO PLL**

VCXO PLL Divider Look-Up Table			Video Clock Application		Alternate Video Clock Application	
V3:V0 Pins	P Value	M Value	Input (kHz/MHz)	VCXO (MHz)	Input (kHz/MHz)	VCXO (MHz)
0000	1000	1000	27MHz	27MHz	26.973MHz	26.973MHz
0001	1001	1000	27MHz	26.973MHz		
0010	11000	4004	74.175MHz	27MHz		
0011	11011	4000	74.25MHz	26.973MHz		
0100	11000	4000	74.25MHz	27MHz		
0101	4004	4004	27MHz	27MHz	26.973MHz	26.973MHz
0110	4004	4000	27MHz	26.973MHz		
0111	1000	1001	26.973MHz	27MHz		
1000	250	91	74.175MHz	27MHz		
1001	253	92	74.25MHz	27MHz		
1010	92	92	27MHz	27MHz	26.973MHz	26.973MHz
1011	1	600	45kHz (720P/60 hsync)	27MHz	44.955kHz (720P/59.94)	26.973MHz
1100	1	800	33.75kHz (1080I/60 hsync)	27MHz	33.716kHz (1080I/59.94)	26.973MHz
1101	1	1728	15.625kHz (PAL hsync)	27MHz		
1110	1	1716	15.734kHz (NTSC hsync)	27MHz		
1111	1	960	28.125kHz (1080I/50 hsync)	27MHz		

**TABLE 3B. SECOND FREQUENCY TRANSLATION STAGE: FEMTOCLOCK MULTIPLIER**

FemtoClock Look-Up Table			Video Clock Application		Alternate Video Clock Application	
MF, N1:N0 Pins	FB Div	Out Div	VCXO (MHz)	Q (MHz)	VCXO (MHz)	Q (MHz)
0, 00	22	4	27MHz	148.5MHz	26.973MHz	148.35MHz
0, 01	22	8	27MHz	74.25MHz	26.973MHz	74.175MHz
0, 10	22	12				
0, 11	22	18				
1, 00	24	4				
1, 01	24	8				
1, 10	24	12	27MHz	54MHz		
1, 11	24	18	27MHz	36MHz		

**TABLE 3C. BYPASS FUNCTION TABLE**

Inputs		Operation
nBP1	nBP0	
0	0	Bypass Frequency Translator PLL and Output Divider
0	1	Test Mode: Bypass VCXO Jitter Attenuation PLL and Frequency Translator PLL
1	0	LC Mode: Bypass VCXO Jitter Attenuation PLL
1	1	PLL Mode: Active



TABLE 3D. EXAMPLE FREQUENCY CONFIGURATION TABLE, CONTINUED ON NEXT PAGE

Configuration Example Number	Input Reference Frequency (MHz)	Reference Clock Description	VCXO PLL			FemtoClock PLL		VCO_SEL	Output Frequency (MHz)	Output Description
			P Input Divider	M Feedback Divider	XTAL Frequency (MHz)	MF Feedback Divider	N Output Divider			
1	27	Transport	1001	1000	26.973027	22	8	1	74.17582418	SMPTE 292M/59.94
2	27	Transport	1000	1000	27	22	8	1	74.25	SMPTE 292M/60
3	27	Transport	1001	1000	26.973027	22	4	1	148.3516484	SMPTE 292M/59.94 (1080P)
4	27	Transport	1000	1000	27	22	4	1	148.5	SMPTE 292M/60 (1080P)
5	27	Transport	1001	1000	26.973027	na	na	0	26.973027	Transport x 1000/1001
6	27	Transport	1000	1000	27	na	na	0	27	Transport
10	74.175824	292M/59.94	11000	4004	27	22	8	1	74.25	SMPTE 292M/60
11	74.25	292M/60	11011	4000	26.973027	22	8	1	74.17582418	SMPTE 292M/59.94
12	74.175824	292M/59.94	11000	4000	26.973027	22	8	1	74.17582418	SMPTE 292M/59.94
13	74.25	292M/60	11000	4000	27	22	8	1	74.25	SMPTE 292M/60
14	74.175824	292M/59.94	11000	4004	27	na	na	0	27	Transport
15	74.25	292M/60	11000	4000	27	na	na	0	27	Transport
16	27	Transport	4004	4004	27	na	na	0	27	Transport
17	27	Transport	4004	4000	26.973027	22	8	1	74.17582418	SMPTE 292M/59.94
18	27	Transport	4004	4004	27	22	8	1	74.25	HD B
20	74.175824	292M/59.94	250	91	27	22	8	1	74.25	SMPTE 292M/60
21	74.25	292M/60	253	92	27	22	8	1	74.25	SMPTE 292M/60 (1080P)
22	74.175824	292M/59.94	253	92	26.973027	22	8	1	74.17582418	SMPTE 292M/59.94
23	27	Transport	92	92	27	22	8	1	74.25	SMPTE 292M/60
30	74.175824	292M/59.94	250	91	27	na	na	0	27	Transport
31	74.25	292M/60	253	92	27	na	na	0	27	Transport
32	74.25	292M/60	11011	4000	26.973027	na	na	0	26.973027	Transport x 1000/1001
33	74.175824	292M/59.94	253	92	26.973027	na	na	0	26.973027	Transport x 1000/1001
40	27	Transport	92	92	27	24	12	1	54	ITU-R601/656 Oversample
41	27	Transport	92	92	27	24	18	1	36	259M Level "D" Oversample
42	27	Transport	4004	4004	27	24	18	1	36	259M Level "D" Oversample



**TABLE 3D. EXAMPLE FREQUENCY CONFIGURATION TABLE**

Configuration Example Number	Input Reference Frequency (MHz)	Reference Clock Description	VCXO PLL			FemtoClock PLL		VCO_SEL	Output Frequency (MHz)	Output Clock Description
			P Input Divider	M Feedback Divider	XTAL Frequency (MHz)	FC Feedback Divider	N Output Divider			
50	F1		92	92	F1	na	na	0	F1	F1 = 15 to 30MHz
60	0.015625	PAL Hsync	1	1135	17.735	na	na	0	17.735	4x PAL subcarrier (4xFsc)
61	0.015734	NTSC Hsync	1	910	14.31818	na	na	0	14.31818	4x NTSC subcarrier (4xFsc)
62	0.015625	PAL Hsync	1	1728	27	na	na	0	27	Transport
63	0.015734	NTSC Hsync	1	1716	27	na	na	0	27	Transport
64	0.015625	PAL Hsync	1	1728	27	24	24	1	54	ITU-R601/656 Oversample
65	0.015734	NTSC Hsync	1	1716	27	24	24	1	54	ITU-R601/656 Oversample



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_i$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_o$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	34.8°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$V_{DDX}$	Charge Pump Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current			210		mA
$I_{DDA}$	Analog Supply Current			10		mA
$I_{DDO}$	Output Supply Current			5		mA
$I_{DDX}$	Charge Pump Supply Current			TBD		mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		3.0		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK0, CLK1, MR, MF, P1:P0, V3:0, N1:0, CLK_SEL, XTAL_SEL	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		OE, nBP0, nBP1	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1, MR, MF, P1:P0, V3:0, N1:0, CLK_SEL, XTAL_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		OE, nBP0, nBP1	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{OH}$	Output High Voltage; NOTE 1		2.6			V
$V_{OL}$	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to  $V_{DDO}/2$ .



**TABLE 5. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14		35	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
VCXO $K_{VCO}$ ( $K_{VCXO}$ ); NOTE 1			7000		Hz/V
Frequency Pull Range ( $F_p$ ); NOTE 1			100		ppm
Drive Level				1	mW

NOTE 1: These parameters are only guaranteed when using an ICS recommended quartz crystal device. Contact ICS regarding quartz crystal device recommendations.

**TABLE 6. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$F_{OUT}$	Output Frequency	nBP0, nBP1 = 00	14		35	MHz
		nBP1 = 1	31		175	MHz
$f_{jit}(\theta)$	RMS Phase Jitter, (Random), Configuration 3 of Table 3D; NOTE 1	148.3516484MHz, (Integration Range: 12kHz - 20MHz)		0.81		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

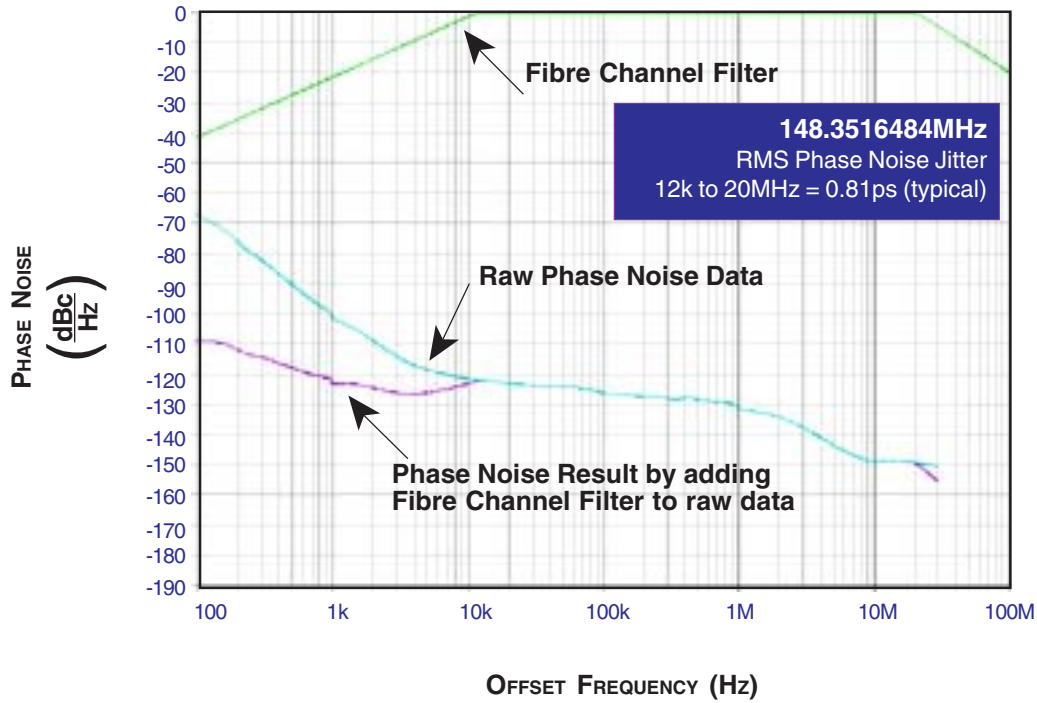
See Parameter Measurement Information section.

NOTE 1: Please refer to the Phase Noise Plot.



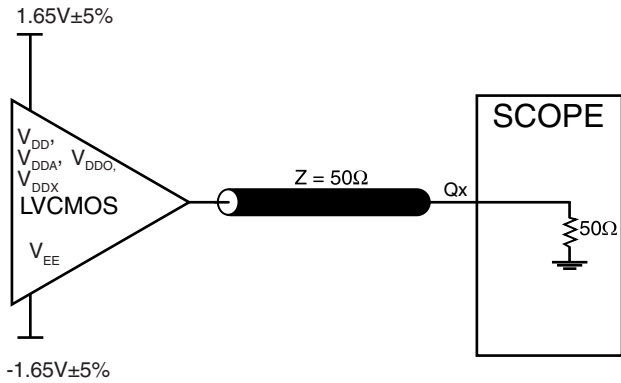


**TYPICAL PHASE NOISE AT 148.3516484MHz**

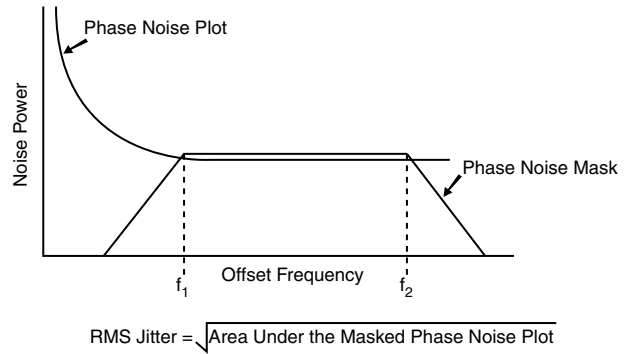




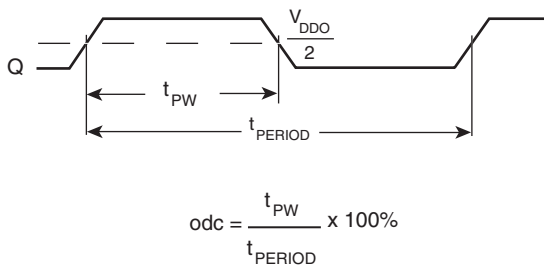
**PARAMETER MEASUREMENT INFORMATION**



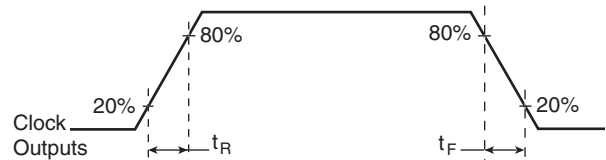
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



**PHASE JITTER**



**OUTPUT DUTY CYCLE/PULSE WIDTH/tPERIOD**



**OUTPUT RISE/FALL TIME**



**APPLICATION INFORMATION**

**EXAMPLE LOOP FILTER COMPONENT VALUES FOR VARIOUS VCXO DIVIDER SELECTIONS**

VCXO PLL Divider Selection	Loop Filter Component Selection					VCXO PLL Performance		Loop Filter Example Number	
	FB Divider (MValue)	Rset (kΩ)	Iset (μA)	Rs (kΩ)	Cs (μF)	Cp (pF)	VCXO PLL Loop BW (Hz/-3dB)		Damping Factor
1000, 1001		2.2	500	261	0.033	1500	200	1.4	1
		4.4	250	261	0.068	3300	100	1.4	2
		4.4	250	53.6	1.5	68000	20	1.4	3
4000, 4001		2.2	500	499	0.033	1500	100	1.3	4
		2.2	500	261	0.15	6800	50	1.5	5
		2.2	500	105	1	33000	20	1.6	6
91, 92		4.4	250	23.2	1	33000	100	1.6	7
600	4.4	250	261	0.068	2200	170	1.8	8	
800						125	1.6		
960						105	1.5		
1000, 1000						100	1.4		
1726, 1728						58	1		
4000, 4004						27	0.7		
1726, 1728						2.2	500		1000





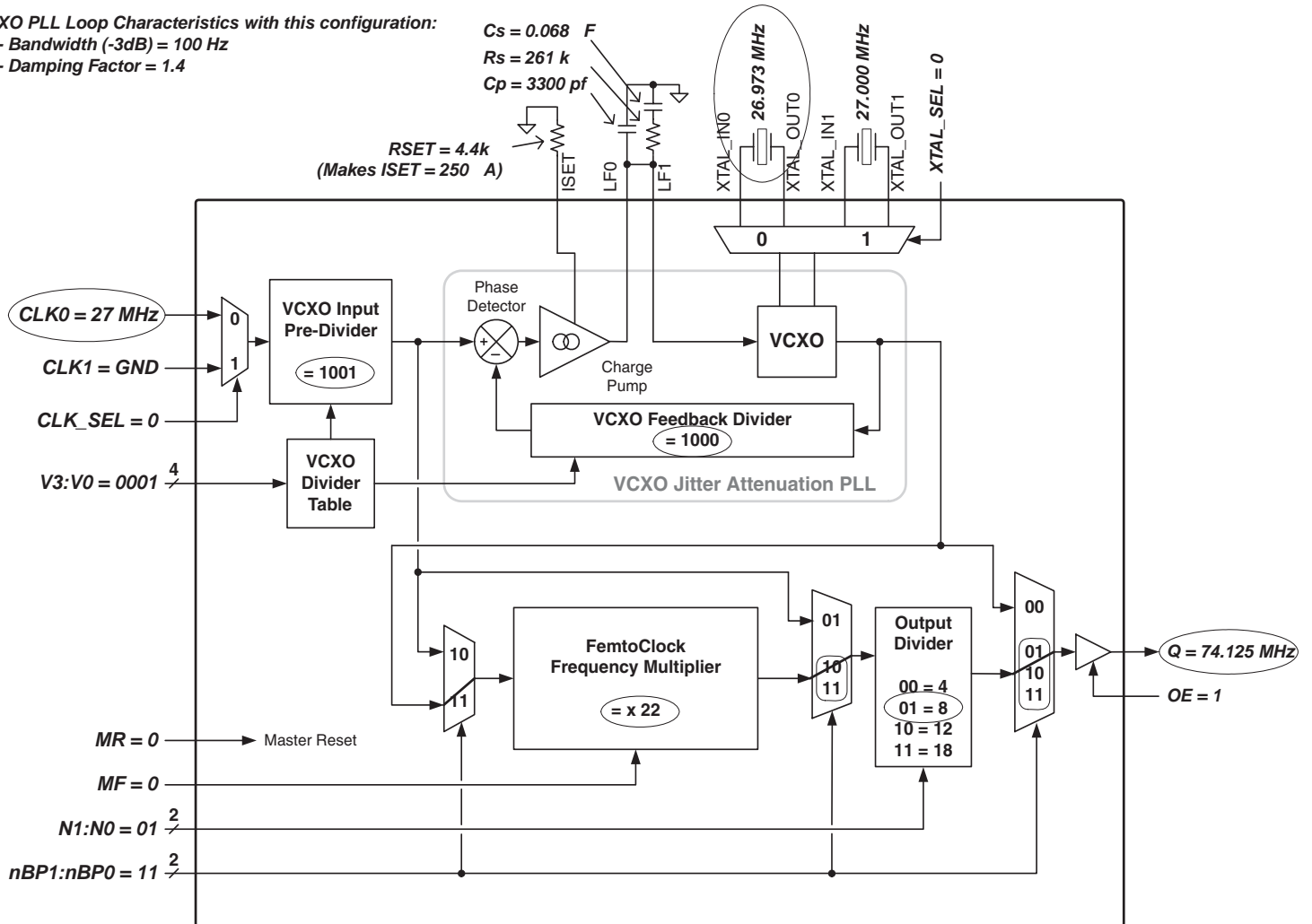
**APPLICATION EXAMPLE 2: 27MHz TO 74.175MHz**

VCXO PLL Loop Characteristics with this configuration:

- Bandwidth (-3dB) = 100 Hz
- Damping Factor = 1.4

$C_s = 0.068 \text{ F}$   
 $R_s = 261 \text{ k}$   
 $C_p = 3300 \text{ pf}$

$R_{SET} = 4.4\text{k}$   
(Makes  $I_{SET} = 250 \text{ A}$ )





**DESCRIPTION OF THE PLL STAGES**

The ICS843002-21 is a two stage device, a VCXO PLL followed by a low phase noise FemtoClock frequency multiplier. The VCXO uses an external pullable crystal which can be pulled ±100ppm by the VCXO PLL circuitry to phase lock it to the input reference frequency. There are two VCXO crystal ports in order to provide VCXO frequency versatility. For HDTV applications, this allows the use of a 26.973027MHz crystal for the generation of 74.175MHz, or a 27.00MHz crystal for the generation of 74.25MHz, for example.

The VCXO output frequency can be output directly from the device, or it can be passed to the FemtoClock frequency multiplier which will multiply it up to a higher frequency.

**VCXO PLL LOOP RESPONSE CONSIDERATIONS**

Loop response characteristics of the VCXO PLL is affected by the VCXO feedback divider value (bandwidth and damping factor), and by the external loop filter components (bandwidth, damping factor, and 2<sup>nd</sup> frequency response). A practical range of VCXO PLL bandwidth is from about 1Hz to about 1kHz. The setting of VCXO PLL bandwidth and damping factor is covered later in this document. A PC based PLL bandwidth calculator is also under development. For assistance with loop bandwidth suggestions or value calculation, please contact ICS applications.

Table 3A shows frequency translation configuration examples. Note that in the first two V3:V0 selections the VCXO PLL feedback divider is the same value of 1000. This means the VCXO PLL loop response (bandwidth and damping factor) will be the same for all of these settings.

The same is true for V3:V0 = 0010 through 0110. This means the device can be configured to translate between 74.175MHz, 74.25MHz, and 27MHz (from any one to another, all nine combinations) and it will maintain the same loop response characteristics. This is also true for V3:V0 = 1000 through 1010.

For high VCXO PLL feedback divider values, the phase detector rate, and therefore loop filter charge pulse rate, is greatly reduced. To prevent output clock wander, low leakage capacitors should be used. In addition, when loop bandwidth is low (say below 20Hz), capacitors with low microphonic sensitivity should be used. PPS film type capacitors are one type that perform well in this environment. Below 5Hz, shielding should be considered to prevent excessive phase wander (low frequency phase jitter or clock phase deviation).

**SETTING THE VCXO PLL LOOP RESPONSE**

The VCXO PLL loop response is determined both by fixed device characteristics and by other characterizes set by the user. This includes the values of R<sub>s</sub>, C<sub>s</sub>, C<sub>p</sub> and R<sub>SET</sub> as shown in the External VCXO PLL Components figure on this page.

The VCXO PLL loop bandwidth is approximated by:

$$NBW (VCXO PLL) = \frac{R_s \times I_{CP} \times K_O}{2\pi \times \text{Feedback Divider}}$$

**WHERE:**

R<sub>s</sub> = Value of resistor R<sub>s</sub> in loop filter in Ohms

I<sub>CP</sub> = Charge pump current in amps (see table on page 12)

K<sub>O</sub> = VCXO Gain in Hz/V

Feedback Divider = 1 to 11011 (as determined by inputs V3:V0)

The above equation calculates the “normalized” loop bandwidth (denoted as “NBW”) which is approximately equal to the -3dB bandwidth. NBW does not take into account the effects of damping factor or the second pole imposed by C<sub>p</sub>. It does, however, provide a useful approximation of filter performance.

To prevent jitter on the clock output due to modulation of the VCXO PLL by the phase detector frequency, the following general rule should be observed:

$$NBW (VCXO PLL) \leq \frac{f (\text{Phase Detector})}{20}$$

f(Phase Detector) = Input Frequency ÷ Pre-Divider)

The PLL loop damping factor is determined by:

$$DF = x \frac{R_s}{2} \sqrt{\frac{I_{CP} \times C_s \times K_O}{\text{Feedback Divider}}}$$

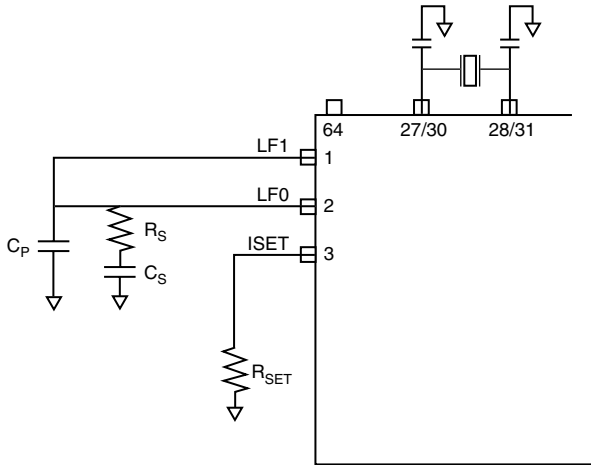
**WHERE:**

C<sub>s</sub> = Value of capacitor C<sub>s</sub> in loop filter in Farads



**EXTERNAL VCXO PLL COMPONENTS**

In general, the loop damping factor should be 0.7 or greater to ensure output stability. A higher damping factor will create less peaking in the passband. A higher damping factor may also increase lock time and output clock jitter when there is excess digital noise in the system application, due to the reduced ability of the PLL to respond to and therefore compensate for phase noise ingress.



The external crystal devices and loop filter components should be kept close to the device. Loop filter and crystal PCB connection traces should be kept short and well separated from each other and from other signal traces. Other signal traces should not run underneath the device, the loop filter or crystal components.

**NOTES ON SETTING THE VALUE OF Cp**

As another general rule, the following relationship should be maintained between components Cs and Cp in the loop filter:

$$C_p = \frac{C_s}{20}$$

Cp establishes a second pole in the VCXO PLL loop filter. For higher damping factors (> 1), calculate the value of Cp based on a Cs value that would be used for a damping factor of 1. This will minimize baseband peaking and loop instability that can lead to output jitter.

Cp also dampens VCXO PLL input voltage modulation by the charge pump correction pulses. A Cp value that is too low will result in increased output phase noise at the phase detector frequency due to this. In extreme cases where input jitter is high, charge pump current is high, and Cp is too small, the VCXO PLL input voltage can hit the supply or ground rail resulting in non-linear loop response.

The best way to set the value of Cp is to use the filter response software available from ICS (please refer to the following section). Cp should be increased in value until it just starts affecting the passband peak.

**NOTES ON EXTERNAL CRYSTAL LOAD CAPACITORS**

In the loop filter schematic diagram, capacitors are shown between pins 27/30 to ground and between pins 38/31 to ground. These are optional crystal load capacitors which can be used to center tune the external pullable crystal (the crystal frequency can only be lowered by adding capacitance, it cannot be raised). Note that the addition of external load capacitors will decrease the crystal pull range and the Kvco value.

**LOOP FILTER RESPONSE SOFTWARE**

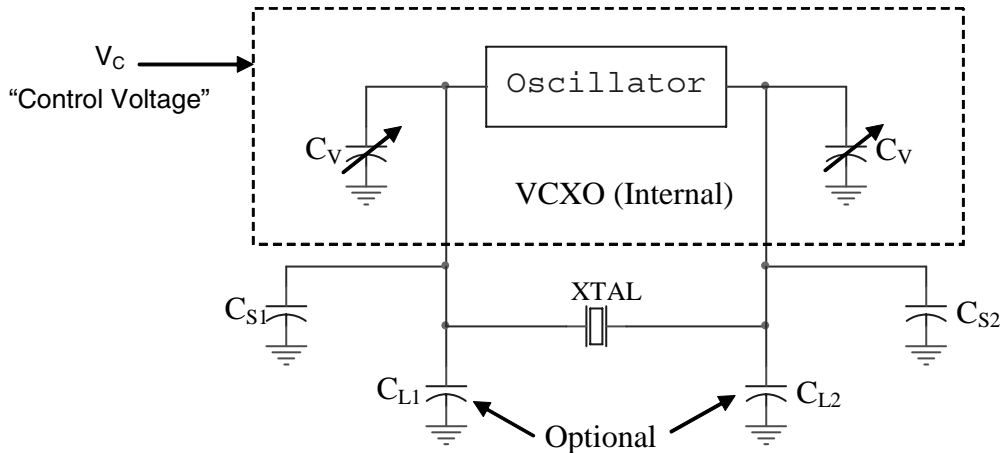
Online tools to calculate loop filter response can be found at [www.icst.com](http://www.icst.com). Contact your local sales representative if a tool cannot be found for this product.



**VCXO CRYSTAL SELECTION**

Choosing a crystal with the correct characteristics is one of the most critical steps in using a Voltage Controlled Crystal Oscillator (VCXO). The crystal parameters affect the tuning range and

accuracy of a VCXO. Below are the key variables and an example of using the crystal parameters to calculate the tuning range of the VCXO.



**FIGURE 1: VCXO OSCILLATOR CIRCUIT EXAMPLE**

$V_c$  Control voltage used to tune frequency

$C_v$  Varactor capacitance, varies due to the change in control voltage

$C_{L1}, C_{L2}$  Load tuning capacitance used for fine tuning or centering nominal frequency

$C_{S1}, C_{S2}$  Stray Capacitance caused by pads, vias, and other board parasitics

**CRYSTAL PARAMETER EXAMPLES**

Symbol	Parameter	Minimum	Typical	Maximum	Units
$f_N$	Nominal Frequency		19.44		MHz
$f_T$	Frequency Tolerance			±20	ppm
$f_S$	Frequency Stability			±20	ppm
	Operating Temperature Range	0		70	°C
$C_L$	Load Capacitance		12		pF
$C_O$	Shunt Capacitance		4		pF
$C_0/C_1$	Pullability Ratio		220	240	
ESR	Equivalent Series Resistance			20	
	Drive Level			1	mW
	Aging @ 25°C	±3 per year			ppm
	Mode of Operation	Fundamental			

**VARACTOR PARAMETERS**

Symbol	Parameter	Test Condition	Typical	Unit
$C_{V\text{ LOW}}$	Low Varactor Capacitance	$V_c = 0V$	15.4	pF
$C_{V\text{ HIGH}}$	High Varactor Capacitance	$V_c = 3.3V$	29.6	pF





**FORMULAS**

$$C_{LOW} = \frac{(C_{L1} + C_{S1} + C_{V\_LOW}) \cdot (C_{L2} + C_{S2} + C_{V\_LOW})}{(C_{L1} + C_{S1} + C_{V\_LOW}) + (C_{L2} + C_{S2} + C_{V\_LOW})}$$

$C_{LOW}$  is the effective capacitance due to the low varactor capacitance, load capacitance and stray capacitance.  $C_{LOW}$  determines the high frequency component on the TPR (Total Pull Range).

$$C_{HIGH} = \frac{(C_{L1} + C_{S1} + C_{V\_HIGH}) \cdot (C_{L2} + C_{S2} + C_{V\_HIGH})}{(C_{L1} + C_{S1} + C_{V\_HIGH}) + (C_{L2} + C_{S2} + C_{V\_HIGH})}$$

$C_{HIGH}$  is the effective capacitance due to the high varactor capacitance, load capacitance and stray capacitance.  $C_{HIGH}$  determines the low frequency component on the TPR (Total Pull Range).

$$TPR = \left( \frac{1}{2 \cdot C_0/C_1 \cdot (1+C_{LOW}/C_0)} - \frac{1}{2 \cdot C_0/C_1 \cdot (1+C_{HIGH}/C_0)} \right) \cdot 10^6$$

AbsolutePullRange (APR) = TotalPullRange – (FrequencyTolerance + FrequencyStability + Aging)

**EXAMPLE CALCULATIONS**

Using the tables and figures above, we can now calculate the TPR and APR of the VCXO using the example crystal parameters. For the numerical example below there were some assumptions made. First, the stray capacitance ( $C_{S1}$ ,  $C_{S2}$ ), which is all the excess capacitance due to board parasitic, is 4pF. Second, the expected lifetime of the project is 5 years; hence

the inaccuracy due to aging is ±15ppm. Third, though many boards will not require load tuning capacitors ( $C_{L1}$ ,  $C_{L2}$ ), it is recommended for long-term consistent performance of the system that two tuning capacitor pads be placed into every design. Typical values for the load tuning capacitors will range from 0 to 4pF.

$$C_{LOW} = \frac{(0 + 4pF + 15.4pF) \cdot (0 + 4pF + 15.4pF)}{(0 + 4pF + 15.4pF) + (0 + 4pF + 15.4pF)} = 9.7pF$$

$$C_{HIGH} = \frac{(0 + 4pF + 29.6pF) \cdot (0 + 4pF + 29.6pF)}{(0 + 4pF + 29.6pF) + (0 + 4pF + 29.6pF)} = 16.8pF$$

$$TPR = \left( \frac{1}{2 \cdot 220 \cdot (1+9.7pF/4pF)} - \frac{1}{2 \cdot 220 \cdot (1+16.8pF/4pF)} \right) \cdot 10^6 = 226.5ppm$$

TPR = ±113.25ppm

APR = 113.25ppm – (20ppm + 20ppm + 15ppm) = ±58.25ppm

The example above will ensure a total pull range of ±113.25 ppm with an APR of ±58.25ppm. Many times, board designers may select their own crystal based on their application. If the application requires a tighter APR, a crystal with better pullability

(C0/C1 ratio) can be used. Also, with the equations above, one can vary the frequency tolerance, temperature stability, and aging or shunt capacitance to achieve the required pullability.



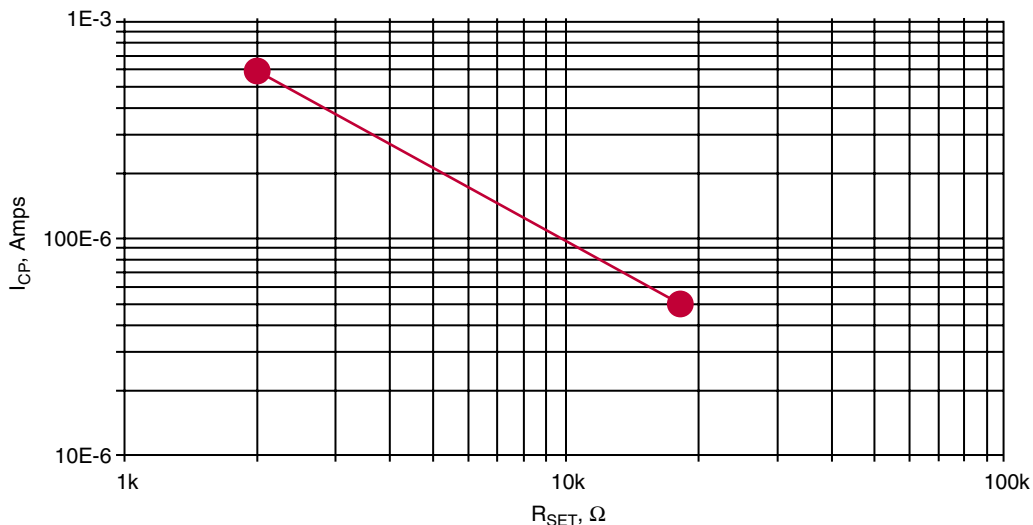
**NOTES ON SETTING CHARGE PUMP CURRENT**

The recommended range for the charge pump current is 50µA to 300µA. Below 50µA, loop filter charge leakage, due to PCB or capacitor leakage, can become a problem. This loop filter leakage can cause locking problems, output clock cycle slips, or low frequency phase noise.

As can be seen in the loop bandwidth and damping factor equations or by using the filter response software available from ICS, increasing charge pump current ( $I_{CP}$ ) increases both bandwidth and damping factor.

**CHARGE PUMP CURRENT, EXAMPLE SETTINGS**

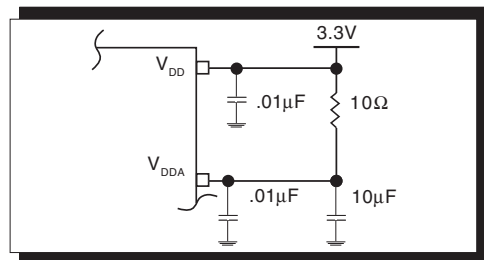
$R_{SET}$	Charge Pump Current ( $I_{CP}$ )
17.6k	62.5µA
8.8k	125µA
4.4k	250µA
2.2k	500µA



**FIGURE 2. CHARGE PUMP CURRENT VS. VALUE OF  $R_{SET}$  (EXTERNAL RESISTOR) GRAPH**

**POWER SUPPLY FILTERING TECHNIQUES**

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS810001-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ ,  $V_{DDX}$ , and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 3* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each  $V_{DDA}$  pin.



**FIGURE 3. POWER SUPPLY FILTERING**



**RELIABILITY INFORMATION**

**TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 32 LEAD VFQFN**

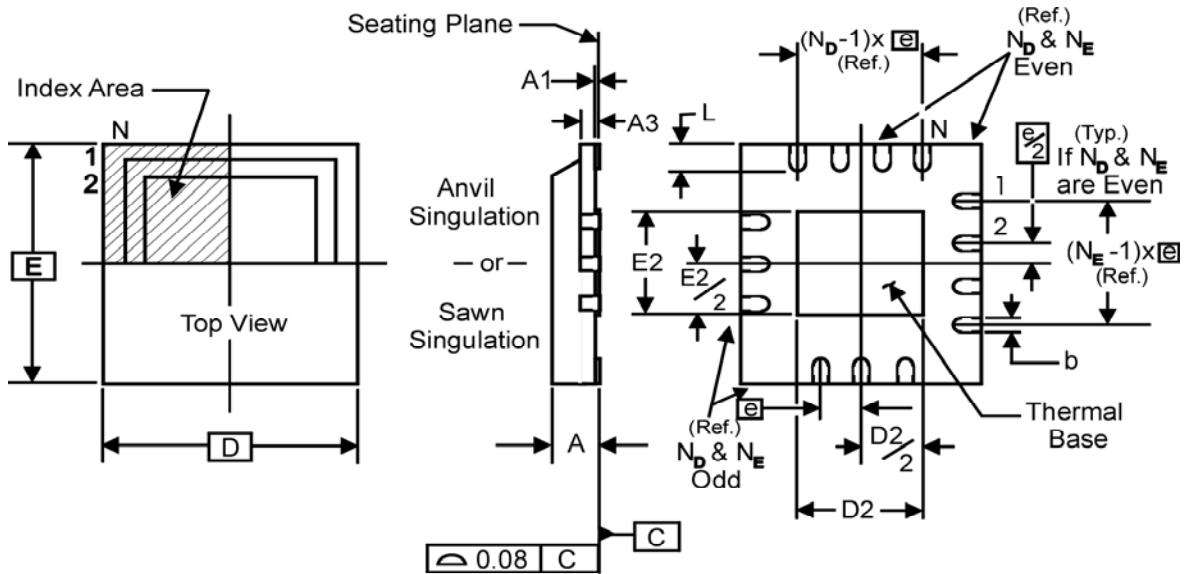
$\theta_{JA}$ vs. 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	0 34.8°C/W

**TRANSISTOR COUNT**

The transistor count for ICS810001-21 is: 9365



**PACKAGE OUTLINE AND DIMENSIONS - K SUFFIX FOR 32 LEAD VFQFN**



**TABLE 8. PACKAGE DIMENSIONS**

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N <sub>b</sub>	8		
N <sub>e</sub>	8		
D	5.00 BASIC		
D2	1.25	2.25	3.25
E	5.00 BASIC		
E2	1.25	2.25	3.25
e	0.50 BASIC		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220



Integrated  
Circuit  
Systems, Inc.

**PRELIMINARY**

**ICS810001-21**  
FEMTOCLOCKS™ DUAL VCXO VIDEO PLL

**TABLE 9. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
ICS810001BK-21	ICS10001B21	32 Lead VFQFN	tray	0°C to 70°C
ICS810001BK-21T	ICS10001B21	32 Lead VFQFN	2500 tape & reel	0°C to 70°C

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