FAIRCHILD SEMICONDUCTOR™

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FIN1108 • FIN1108T (Preliminary) LVDS 8 Port High Speed Repeater

General Description

This 8 port repeater is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology.

The FIN1108 accepts and outputs LVDS levels with a typical differential output swing of 330 mV which provides low EMI at ultra low power dissipation even at high frequencies. The FIN1108 provides a V_{BB} reference for AC coupling on the inputs. In addition the FIN1108 can directly accept LVPECL, HSTL, and SSTL-2 for translation to LVDS.

The FIN1108T has internal termination across the receiver inputs for reduced part count, reduced stub length and better noise immunity. See Applications section.

Features

- Greater than 800 Mbps data rate
- 3.3V power supply operation
- 3.5 ps maximum random jitter and 135 ps maximum deterministic jitter
- Wide rail-to-rail common mode range
- LVDS receiver inputs accept LVPECL, HSTL, and SSTL-2 directly
- Ultra low power consumption
- 20 ps typical channel-to-channel skew
- Power off protection
- > 7.5 kV HBM ESD Protection
- Meets or exceeds the TIA/EIA-644-A LVDS standard
- Available in space saving 48-lead TSSOP package
- Open circuit fail safe protection
- V_{BB} reference output
- FIN1108T (R_T) features Internal Termination Resistors

Ordering Code:

Order Number	Package Number	Package Description
FIN1108MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN1108TMTD (Preliminary)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Pin Descriptions

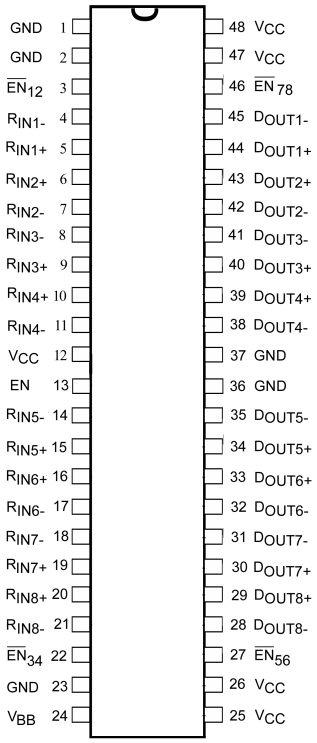
Pin Name	Description
R_{IN1+}, R_{IN2+}, R_{IN3+}, R_{IN4+}, R_{IN5+}, R_{IN6+}, R_{IN7+}, R_{IN8+}	Non-inverting LVDS Input
R_{IN1-}, R_{IN2-}, R_{IN3-}, R_{IN4-}, R_{IN5-}, R_{IN6-}, R_{IN7-}, R_{IN8-}	Inverting LVDS Input
D_{OUT1+}, D_{OUT2+}, D_{OUT3+}, D_{OUT4+}, D_{OUT5+}, D_{OUT6+}, D_{OUT7+}, D_{OUT8+}	Non-inverting Driver Output
D_{OUT1-}, D_{OUT2-}, D_{OUT3-}, D_{OUT4-}, D_{OUT5-}, D_{OUT6-}, D_{OUT7-}, D_{OUT8-}	Inverting Driver Output
EN	Driver Enable Pin for All Output
$\overline{EN}_{12}$	Inverting Driver Enable Pin for D_{OUT1} and D_{OUT2}
$\overline{EN}_{34}$	Inverting Driver Enable Pin for D_{OUT3} and D_{OUT4}
$\overline{EN}_{56}$	Inverting Driver Enable Pin for D_{OUT5} and D_{OUT6}
$\overline{EN}_{78}$	Inverting Driver Enable Pin for D_{OUT7} and D_{OUT8}
V_{CC}	Power Supply
GND	Ground
V_{BB}	Reference Voltage Output

Function Table

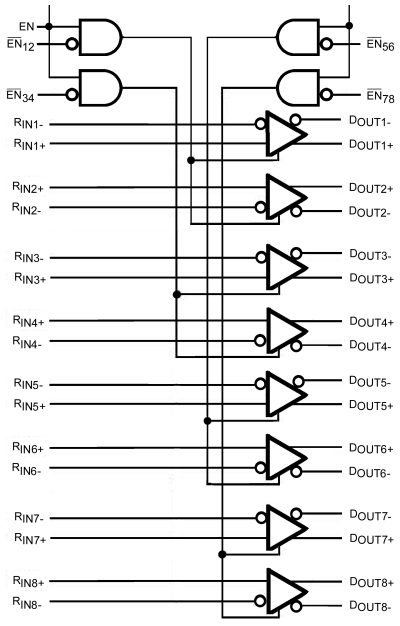
Inputs				Outputs	
EN	$\overline{EN}_{xx}$	D_{IN+}	D_{IN-}	D_{OUT+}	D_{OUT-}
H	L	H	L	H	L
H	L	L	H	L	H
H	L	Fail Safe Case		H	L
X	H	X	X	Z	Z
L	X	X	X	Z	Z

H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care
Z = High Impedance

Connection Diagram



Functional Diagram



Applications

Signal Optimization via Internal Termination

For LVDS signaling in point-to-point applications, receivers or repeaters with on-chip termination are preferable to reduce the overshoot or undershoot due to the reflection caused by stubs at receiver inputs. As a rule of thumb, usually the termination resistor for an LVDS receiver should be placed as close as possible to the receiver, especially for high speed applications. If the distance between termination resistors and receivers is too long, the interconnection will be seen as an un-terminated stub which can produce reflections resulting in higher EMI. Internal termination can effectively smooth out this ringing which can otherwise jeopardize the receiver noise margin. This is important for reliable high-speed operation with tighter required signal settling times. Below is a list of the advantages/disadvantages of internal termination.

Internal termination is not suitable for all applications. In order to set a proper V_{OD} at the driver outputs, receivers with on-chip termination resistors only work for point-to-point applications since multi-drop applications would require termination resistor for each receiver, reducing the equivalent termination to $R_{T/n}$. This would reduce the driver output swing by n.

Advantages:

1. Reduced device count resulting in reduced board space and production cost.
2. Reduced reflections caused by the stub length on the receiver inputs, improving the signal integrity.

Disadvantages:

1. Without special process treatment, on-chip termination can experience greater temperature variation. This is usually tolerable for low speed applications that have a sufficient unit interval.
2. For applications with high common-mode noise, a center tapped capacitor at the receiver side is desirable to filter out the common-mode voltage noise of the input LVDS signal. This scheme works for an external termination scheme with two (50Ω each for nominal 100Ω termination resistor) half-value termination resistors connected in series and center tapped to a capacitor to Ground. To implement this scheme using internal termination resistors, a center tap pin would have to be used. This would increase the package size of the part.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
LVDS DC Input Voltage (V_{IN})	−0.5V to +4.6V
LVDS DC Output Voltage (V_{OUT})	−0.5V to +4.6V
Driver Short Circuit Current (I_{OSD})	Continuous 10 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
ESD (Human Body Model)	7500V
ESD (Machine Model)	400V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Magnitude of Differential Voltage ($\|V_{ID}\|$)	100 mV to V_{CC}
Common Mode Voltage Range (V_{IC})	$(0V + \|V_{ID}\|/2)$ to $(V_{CC} - \|V_{ID}\|/2)$
Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1; V_{IC} = +0.05V, + 1.2V, or V_{CC} − 0.05V				100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1; V_{IC} = +0.05V, + 1.2V, or V_{CC} − 0.05V		−100			mV
V_{IH}	Input HIGH Voltage (EN or $\overline{EN}$)			2.0		V_{CC}	V
V_{IL}	Input LOW Voltage (EN or $\overline{EN}$)			GND		0.8	V
V_{OD}	Output Differential Voltage	R_L = 100 Ω, Driver Enabled, See Figure 2		250	330	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH					25	mV
V_{OS}	Offset Voltage			1.125	1.23	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH					25	mV
I_{OS}	Short Circuit Output Current	D_{OUT+} = 0V and D_{OUT-} = 0V, Driver Enabled			−3.4	−6	mA
		V_{OD} = 0V, Driver Enabled			±3.4	±6	mA
I_{IN}	Input Current (EN, $\overline{EN}$, D_{INx+}, D_{INx-})	V_{IN} = 0V to V_{CC}, Other Input = V_{CC} or 0V (for Differential Inputs)				±20	µA
I_{OFF}	Power Off Input or Output Current	V_{CC} = 0V, V_{IN} or V_{OUT} = 0V to 3.6V				±20	µA
I_{CCZ}	Disabled Power Supply Current	Drivers Disabled				20	mA
I_{CC}	Power Supply Current	Drivers Enabled, Any Valid Input Condition				80	mA
I_{OZ}	Disabled Output Leakage Current	Driver Disabled, D_{OUT+} = 0V to 3.6V or D_{OUT-} = 0V to 3.6V				±20	µA
V_{IC}	Common Mode Voltage Range			$V_{ID}/2$		$V_{CC} - (V_{ID}/2)$	V
C_{IN}	Input Capacitance		Enable Input		3		pF
			LVDS Input		3		
C_{OUT}	Output Capacitance				3		pF
V_{BB}	Output Reference Voltage	V_{CC} = 3.3V, I_{BB} = 0 to −275 µA		1.125	1.2	1.375	V
R_T	Terminating Resistance				100		Ω

Note 2: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLHD}	Differential Output Propagation Delay LOW-to-HIGH	R_L = 100 Ω, C_L = 5 pF, V_{ID} = 200 mV to 450 mV, V_{IC} = V_{ID}/2 to V_{CC} – (V_{ID}/2), Duty Cycle = 50%, See Figure 1 and Figure 1	0.75	1.1	1.75	ns
t_{PHLD}	Differential Output Propagation Delay HIGH-to-LOW		0.75	1.1	1.75	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.29	0.4	0.58	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.29	0.4	0.58	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$			0.02	0.2	ns
$t_{SK(LH)}$, $t_{SK(HL)}$	Channel-to-Channel Skew (Note 4)			0.02 0.02	0.15	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)				0.5	ns
f_{MAX}	Maximum Frequency (Note 6)(Note 7)		400	>630		MHz
t_{PZHD}	Differential Output Enable Time from Z to HIGH	R_L = 100 Ω, C_L = 5 pF, See Figure 2 and Figure 3		3	5	ns
t_{PZLD}	Differential Output Enable Time from Z to LOW			3.1	5	ns
t_{PHZD}	Differential Output Disable Time from HIGH to Z			2.2	5	ns
t_{PLZD}	Differential Output Disable Time from LOW to Z			2.5	5	ns
t_{DJ}	LVDS Data Jitter, Deterministic	V_{ID} = 300 mV, PRBS = 2^{23} - 1, V_{IC} = 1.2V at 800 Mbps		80	135	ps
t_{RJ}	LVDS Clock Jitter, Random (RMS)	V_{ID} = 300 mV, V_{IC} = 1.2V at 400 MHz		1.9	3.5	ps

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 6: Passing criteria for maximum frequency is the output V_{OD} > 250 mV and the duty cycle is better than 45% / 55% with all channels switching.

Note 7: Output loading is transmission line environment only; C_L is < 1 pF of stray test fixture capacitance.

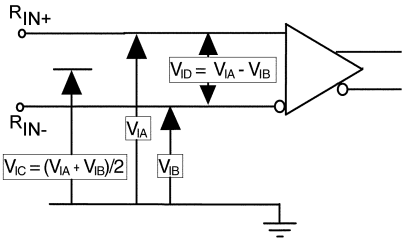


FIGURE 1. Differential Receiver Voltage Definitions

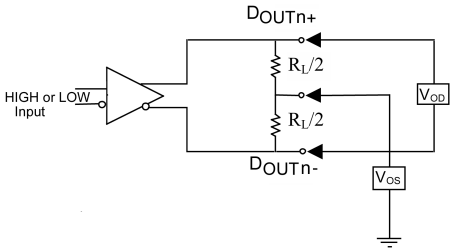
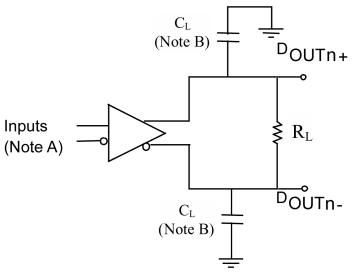


FIGURE 2. Differential Driver DC Test Circuit



Note A: All LVDS input pulses have frequency = 10 MHz, t_R or t_F < = 0.5 ns

Note B: C_L includes all probe and jig capacitances

FIGURE 3. Differential Driver Propagation Delay and Transition Time Test Circuit

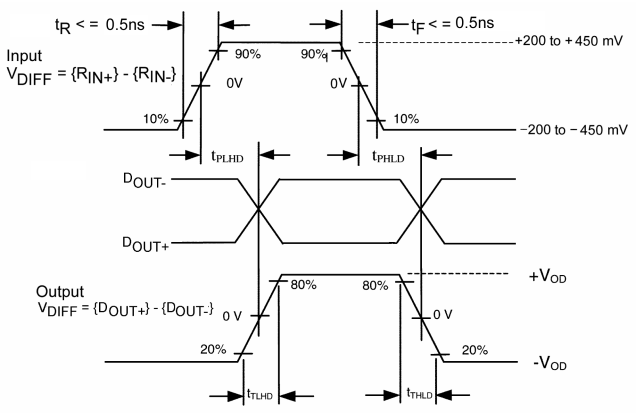
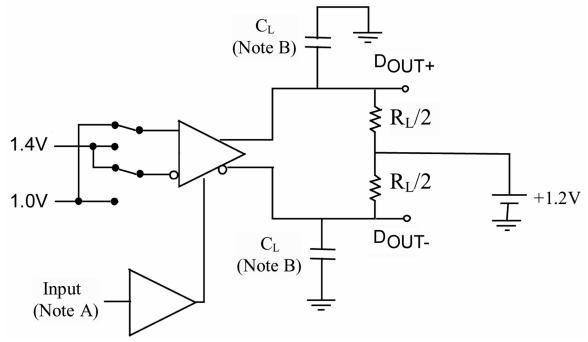


FIGURE 4. AC Waveform



Note A: All LVTTL input pulses have frequency = 10MHz, t_R or t_F < = 2 ns

Note B: C_L includes all probe and jig capacitances

FIGURE 5. Differential Driver Enable and Disable Circuit

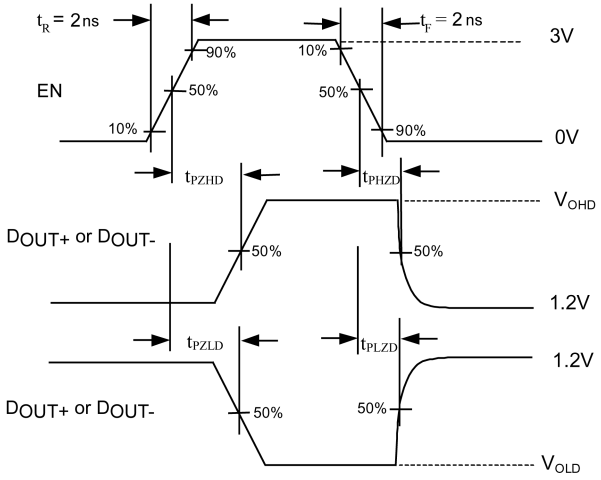
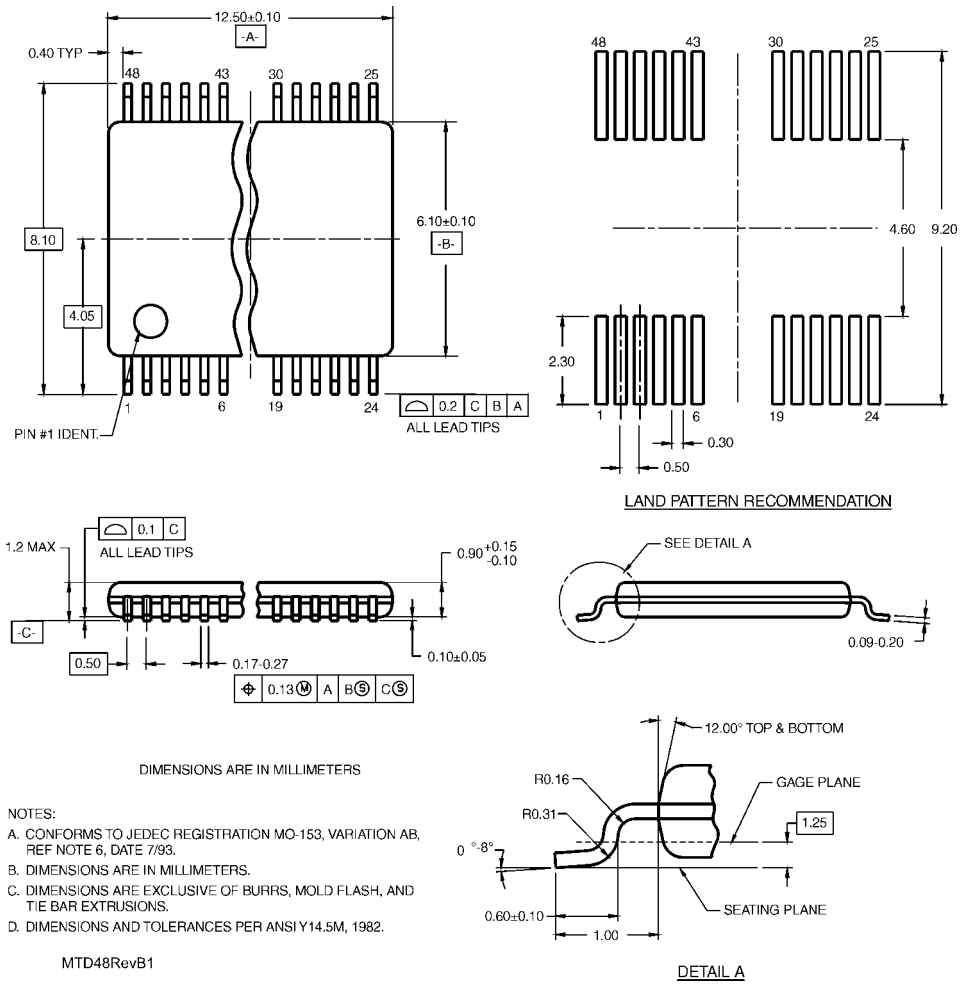


FIGURE 6. Enable and Disable AC Waveforms



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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