



Advanced  
Micro  
Devices

# Am27S29/Am27S29A/Am27S29SA

4,096-Bit (512x8) Bipolar PROM

## DISTINCTIVE CHARACTERISTICS

- High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

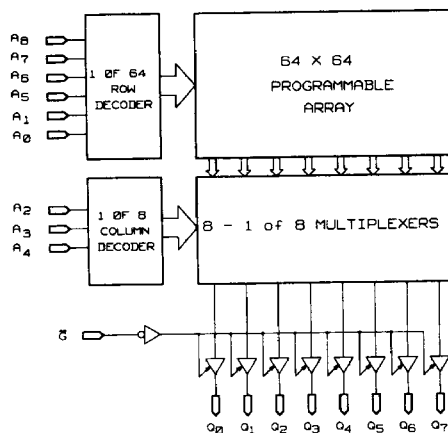
## GENERAL DESCRIPTION

The Am27S29 (512-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs, compatible with low-power Schottky bus standards capable of satisfying the

requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word depth expansion is facilitated by an active LOW ( $\bar{G}$ ) output enable.

## FUNCTIONAL BLOCK DIAGRAM



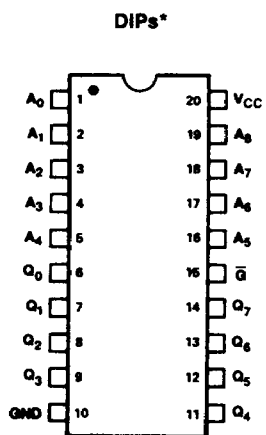
BD006182

## PRODUCT SELECTOR GUIDE

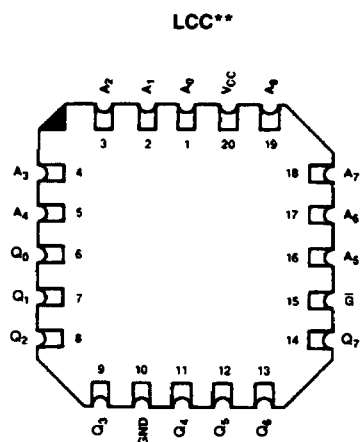
| Three-State Part Number | Am27S29SA |       | Am27S29A |       | Am27S29 |       |
|-------------------------|-----------|-------|----------|-------|---------|-------|
| Address Access Time     | 30 ns     | 40 ns | 35 ns    | 45 ns | 55 ns   | 70 ns |
| Operating Range         | C         | M     | C        | M     | C       | M     |

## CONNECTION DIAGRAMS

### Top View



CD000681



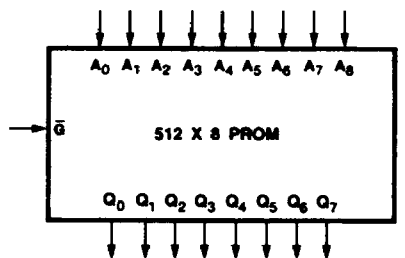
CD000691

\*Also available in a 20-pin Flatpack. Pinout identical to DIPs.

\*\*Also available in a 20-pin PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



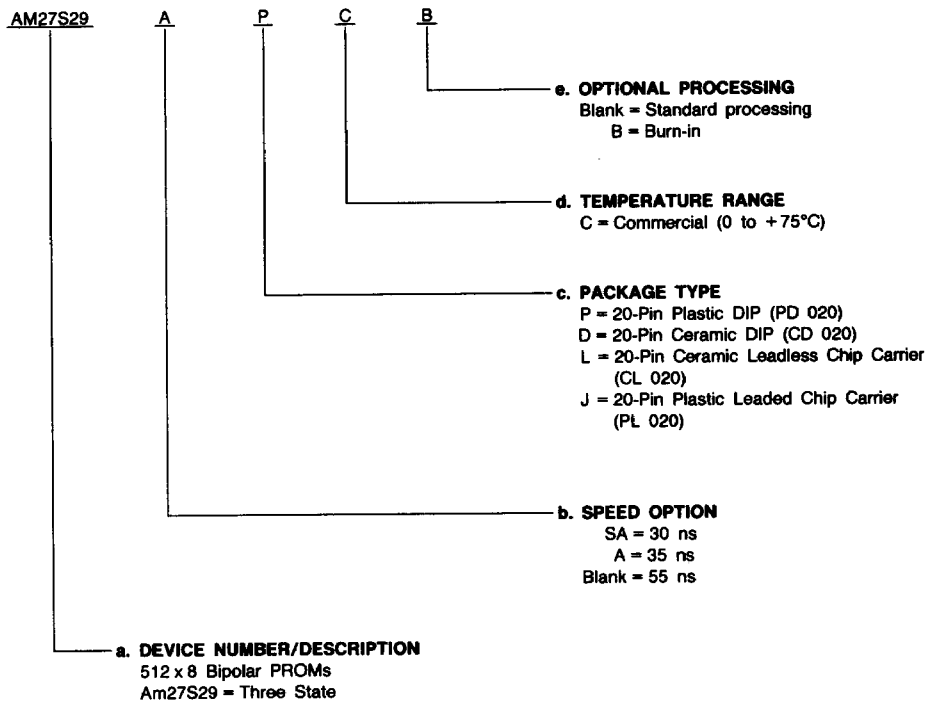
LS000141

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



| Valid Combinations |                   |
|--------------------|-------------------|
| AM27S29            | PC, PCB, DC, DCB, |
| AM27S29A           | LC, LCB, JC, JCB  |
| AM27S29SA          |                   |

### Valid Combinations

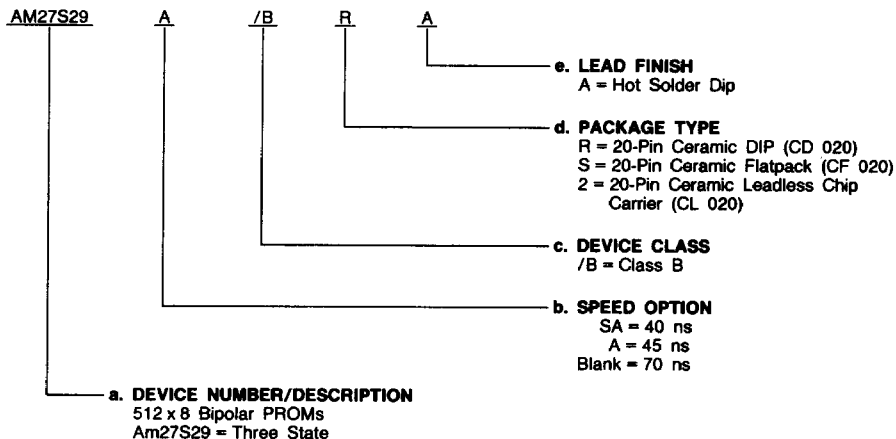
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



| Valid Combinations |                  |
|--------------------|------------------|
| AM27S29            | /BRA, /BSA, /B2A |
| AM27S29A           |                  |
| AM27S29SA          |                  |

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A Tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>8</sub> Address (Inputs)

The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

### Q<sub>0</sub> - Q<sub>7</sub> Data Output Port

The outputs whose state represents the data read from the selected memory locations.

### $\bar{Q}$ Output Enable (Input)

Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

Enable =  $\bar{Q}$

Disable = G

### V<sub>CC</sub> Device Power Supply Pin

The most positive of the logic power supply pins.

### GND Device Power Supply Pin

The most negative of the logic power supply pins.

## ABSOLUTE MAXIMUM RATINGS

|                                                                                  |                                   |
|----------------------------------------------------------------------------------|-----------------------------------|
| Storage Temperature .....                                                        | - 65 to + 150°C                   |
| Ambient Temperature with<br>Power Applied .....                                  | - 55 to + 125°C                   |
| Supply Voltage .....                                                             | - 0.5 V to + 7.0 V                |
| DC Voltage Applied to Outputs<br>(Except During Programming) .....               | - 0.5 V to + V <sub>CC</sub> Max. |
| DC Voltage Applied to Outputs<br>During Programming .....                        | 21 V                              |
| Output Current into Outputs During<br>Programming (Max. Duration of 1 sec) ..... | 250 mA                            |
| DC Input Voltage .....                                                           | - 0.5 V to + 5.5 V                |
| DC Input Current .....                                                           | - 30 mA to + 5 mA                 |

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

|                                             |                      |
|---------------------------------------------|----------------------|
| Ambient Temperature (T <sub>A</sub> ) ..... | 0 to + 75°C          |
| Supply Voltage (V <sub>CC</sub> ) .....     | + 4.75 V to + 5.25 V |

### Military (M) Devices\*

|                                          |                    |
|------------------------------------------|--------------------|
| Case Temperature (T <sub>C</sub> ) ..... | - 55 to + 125°C    |
| Supply Voltage (V <sub>CC</sub> ) .....  | + 4.5 V to + 5.5 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military product 100% tested at T<sub>C</sub> = + 25°C, + 125°C, and - 55°C.

## DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol         | Parameter Description        | Test Conditions                                                                                           | Min. | Typ. | Max.   | Unit |
|--------------------------|------------------------------|-----------------------------------------------------------------------------------------------------------|------|------|--------|------|
| V <sub>OH</sub> (Note 1) | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 2.4  |      |        | V    |
| V <sub>OL</sub>          | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |      |      | 0.50   | V    |
| V <sub>IH</sub>          | Input HIGH Level             | Guaranteed input logical HIGH voltage for all inputs (Note 2)                                             | 2.0  |      |        | V    |
| V <sub>IL</sub>          | Input LOW Level              | Guaranteed input logical LOW voltage for all inputs (Note 2)                                              |      |      | 0.8    | V    |
| I <sub>IL</sub>          | Input LOW Current            | V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.45 V                                                          |      |      | -0.250 | mA   |
| I <sub>IH</sub>          | Input HIGH Current           | V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V                                                           |      |      | 25     | μA   |
| I <sub>SC</sub> (Note 1) | Output Short-Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 3)                                                 | -20  |      | -90    | mA   |
| I <sub>CC</sub>          | Power Supply Current         | All inputs = GND<br>V <sub>CC</sub> = Max.                                                                |      |      | 160    | mA   |
| V <sub>I</sub>           | Input Clamp Voltage          | V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA                                                          |      |      | -1.2   | V    |
| I <sub>CEX</sub>         | Output Leakage Current       | V <sub>CC</sub> = Max.<br>V <sub>G</sub> = 2.4 V (Note 1)                                                 |      |      | 40     | μA   |
|                          |                              | V <sub>OUT</sub> = 0.4 V                                                                                  |      |      | -40    |      |
| C <sub>IN</sub>          | Input Capacitance            | V <sub>IN</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V;<br>T <sub>A</sub> = 25°C              |      | 4    |        | pF   |
| C <sub>OUT</sub>         | Output Capacitance           | V <sub>OUT</sub> = 2.0 V @ f = 1 MHz (Note 4) V <sub>CC</sub> = 5 V;<br>T <sub>A</sub> = 25°C             |      | 8    |        |      |

- Notes: 1. This applies to three-state devices only.  
2. V<sub>IL</sub> and V<sub>IH</sub> are input conditions of output tests and are not themselves directly tested. V<sub>IL</sub> and V<sub>IH</sub> are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.  
4. These parameters are not 100% tested, but are periodically evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted\*)

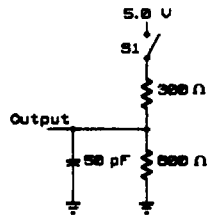
| No. | Parameter Symbol | Parameter Description                          | "SA" Version |      |      |      | "A" Version |      |      |      | Standard Version |      |      |      | Units |
|-----|------------------|------------------------------------------------|--------------|------|------|------|-------------|------|------|------|------------------|------|------|------|-------|
|     |                  |                                                | COM'L        |      | MIL  |      | COM'L       |      | MIL  |      | COM'L            |      | MIL  |      |       |
|     |                  |                                                | Min.         | Max. | Min. | Max. | Min.        | Max. | Min. | Max. | Min.             | Max. | Min. | Max. |       |
| 1   | TAVQV            | Address Valid to Output Valid Access Time      |              | 30   |      | 40   |             | 35   |      | 45   |                  | 55   |      | 70   | ns    |
| 2   | TGVQZ            | Delay from Output Enable Valid to Output Hi-Z  |              | 20   |      | 25   |             | 20   |      | 25   |                  | 25   |      | 30   | ns    |
| 3   | TGVQV            | Delay from Output Enable Valid to Output Valid |              | 20   |      | 25   |             | 20   |      | 25   |                  | 25   |      | 30   | ns    |

See also Switching Test Circuits.

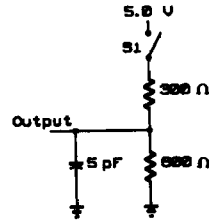
- Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Figure A.  
2. TGVQZ is measured at steady state HIGH output voltage - 0.5 V and steady state LOW output voltage + 0.5 V output levels using the test load in Figure B.

\*Subgroups 7 and 8 apply to functional tests.

## SWITCHING TEST CIRCUITS



TC003442



TC003452

### A. Output Load for all A-C tests except TGVQZ

### B. Output Load for TGVQZ

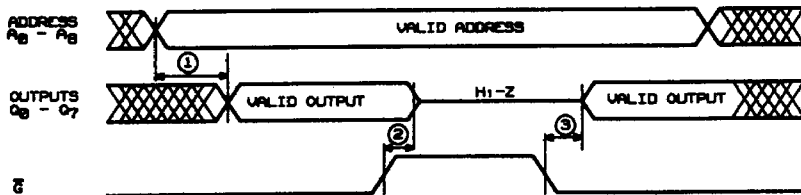
- Notes: 1. All device test loads should be located within 2" of device output pin.  
 2.  $S_1$  is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.  
 $S_1$  is closed for all other AC tests.  
 3. Load capacitance includes all stray and fixture capacitance.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS                           | OUTPUTS                                   |
|----------|----------------------------------|-------------------------------------------|
|          | MUST BE STEADY                   | WILL BE STEADY                            |
|          | MAY CHANGE FROM H TO L           | WILL BE CHANGING FROM H TO L              |
|          | MAY CHANGE FROM L TO H           | WILL BE CHANGING FROM L TO H              |
|          | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN                   |
|          | DOES NOT APPLY                   | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

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