

MOS FIELD EFFECT TRANSISTOR μ PA2752GR

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2752GR is Dual N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Dual chip type
- Low on-state resistance

 $R_{DS(on)1} = 23.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, Ip} = 4.0 \text{ A)}$

 $R_{DS(on)2} = 35.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.5 \text{ V, Ip} = 4.0 \text{ A)}$

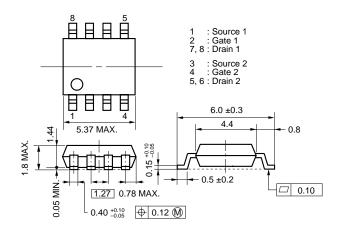
 $R_{DS(on)3} = 41.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.0 \text{ V, Ip} = 4.0 \text{ A)}$

- Low Ciss: Ciss = 480 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2752GR	Power SOP8

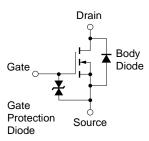
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±8.0	Α
Drain Current (pulse) Note1	I _{D(pulse)}	±32	Α
Total Power Dissipation (1 unit) Note2	Рт	1.7	W
Total Power Dissipation (2 unit) Note2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current Note3	las	8	Α
Single Avalanche Energy Note3	Eas	6.4	mJ

EQUIVALENT CIRCUIT (1/2 Circuit)



- **Notes 1.** PW \leq 10 μ s, Duty cycle \leq 1%
 - **2.** TA = 25° C, Mounted on ceramic substrate of 2000 mm² x 2.2 mm
 - 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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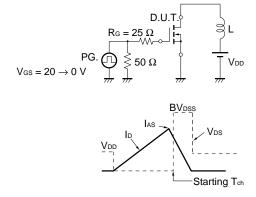


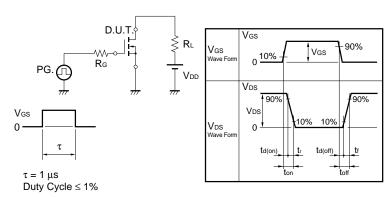
ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	Vps = 30 V, Vgs = 0 V			10	μΑ
Gate Leakage Current	Igss	Vgs = ±18 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	3.5	7.0		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 4.0 A		18.0	23.0	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 4.0 A		25.0	35.0	mΩ
	RDS(on)3	VGS = 4.0 V, ID = 4.0 A		28.5	41.0	mΩ
Input Capacitance	Ciss	Vps = 10 V		480		pF
Output Capacitance	Coss	Vgs = 0 V		190		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		70		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 4.0 A		9.9		ns
Rise Time	tr	Vgs = 10 V		6.2		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 10 \Omega$		25		ns
Fall Time	t f			5.8		ns
Total Gate Charge	Q _G	V _{DD} = 24 V		10		nC
Gate to Source Charge	Qgs	Vgs = 10 V		1.9		nC
Gate to Drain Charge	Q _{GD}	ID = 8.0 A		2.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 8.0 A, VGS = 0 V		0.81		V
Reverse Recovery Time	trr	IF = 8.0 A, VGS = 0 V		28		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μs		23		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



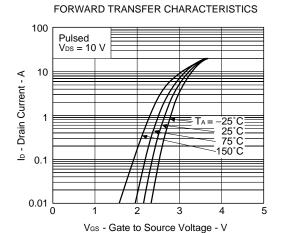


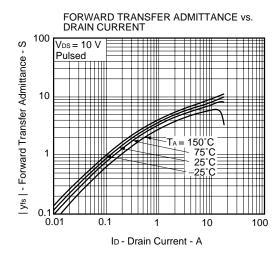
TEST CIRCUIT 3 GATE CHARGE

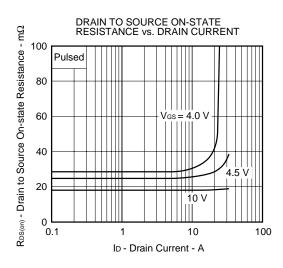
$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \begin{array}{c} MA \\ \hline \end{array} \\ PG. \\ \begin{array}{c} \\ \\ \\ \end{array} \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \end{array} \\ V_{DD}$$

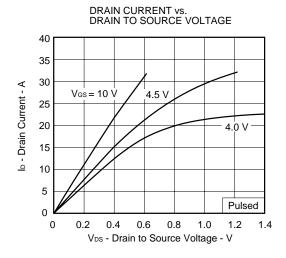


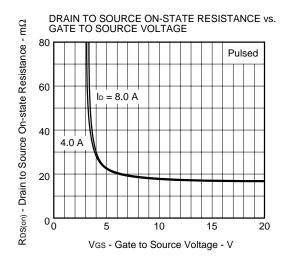
TYPICAL CHARACTERISTICS (TA = 25°C)

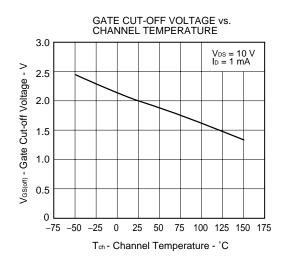


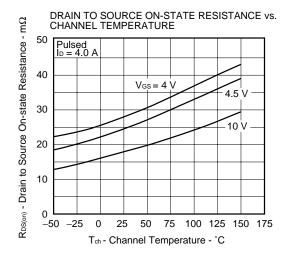


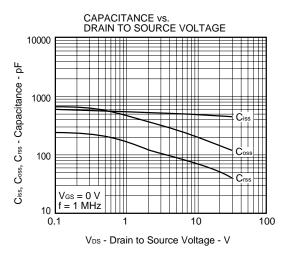


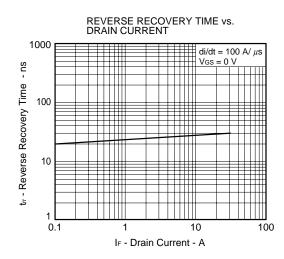


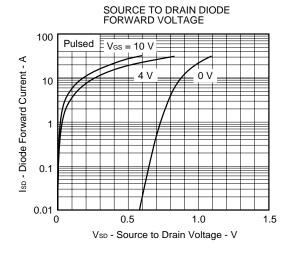


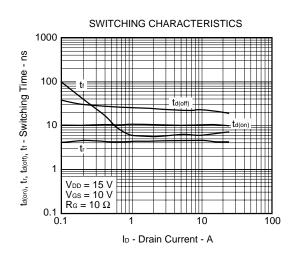


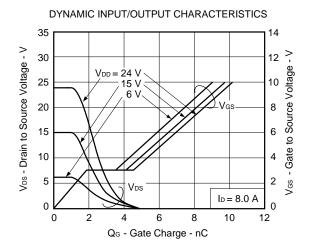


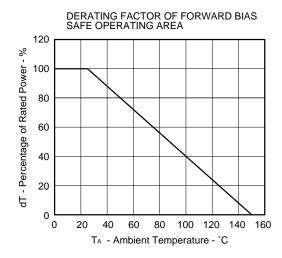


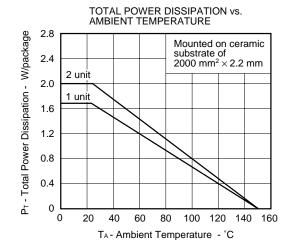




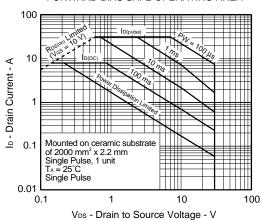




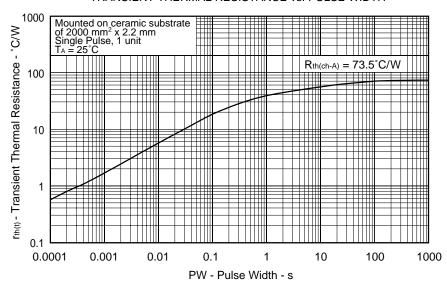




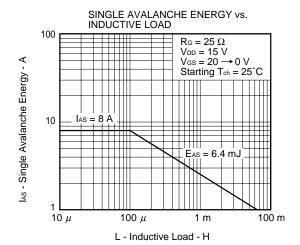


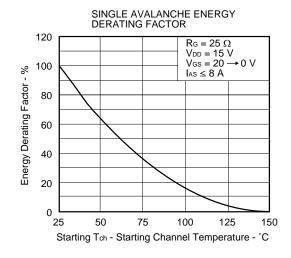


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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NEC μ PA2752GR

[MEMO]

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