Multi LDOs for Cellular-phone

R5312L SERIES

APPLICATION MANUAL

NO. EA-068-0006

R5312L SERIES

OUTLINE

The R5312L series are Multi LDO regulators for power management of cellular phones. All of regulators are low noise and extremely low quiescent current by CMOS process. Each of these ICs consists of eight LDOs, voltage detectors for supply voltage monitoring, and two LED drivers. Each of them can be controlled by CPU via 3-wire serial interface. These ICs make it possible to integrate almost all of power management and analog drivers in cellular-phone systems. The output voltage of regulators can be set individually by laser trim as well as detector thresholds.

A tiny 32-pin QFP, 0.5mm lead pitch, is available.

FEATURES

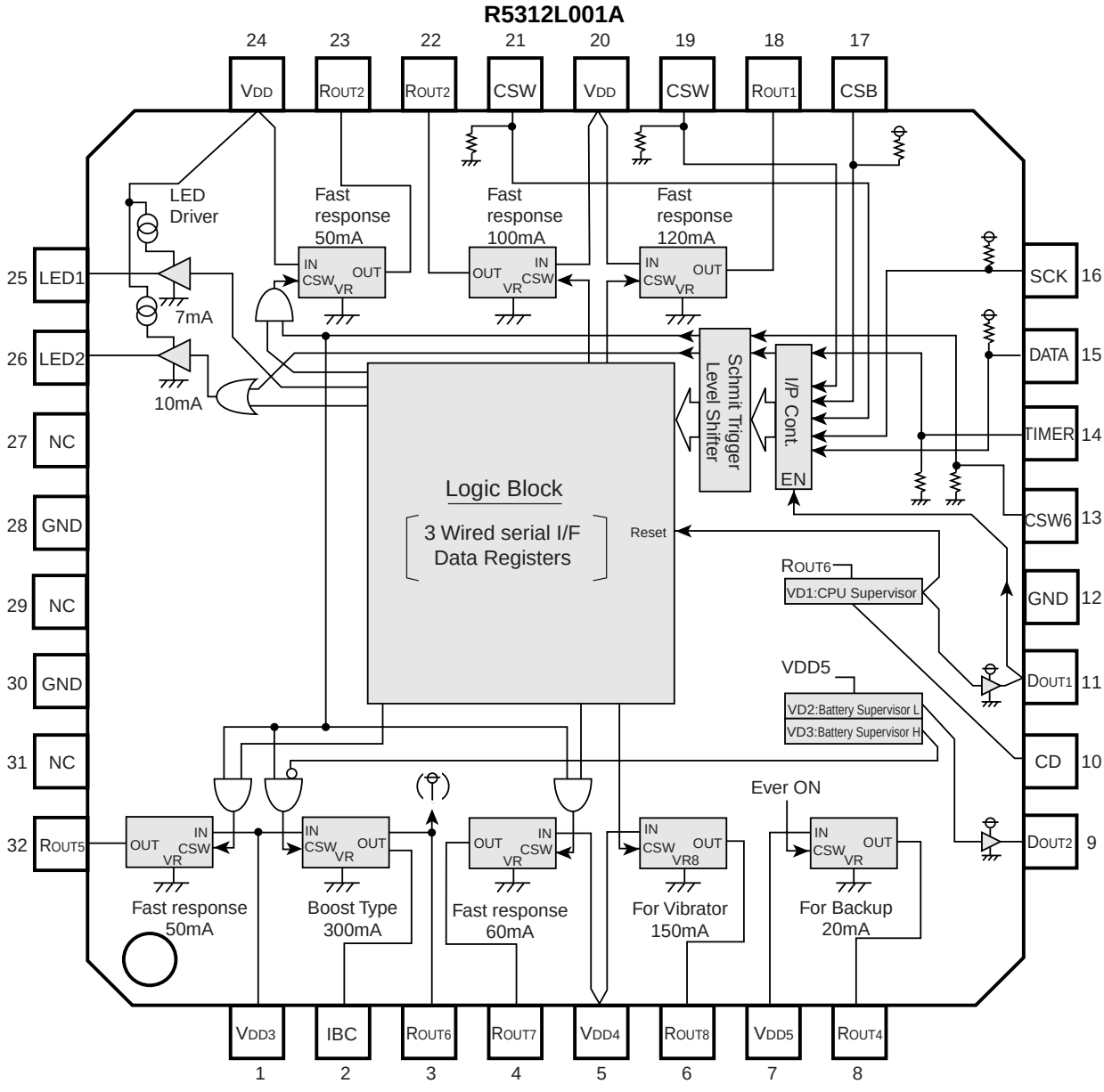
- Ultra Low Standby Current .....10μA TYP. with only VR4 is enabled at no load
- High Accuracy Output Voltage and Detector Threshold.....±2.0% (except VR7 and VR8)
- Output Voltage and Detector Threshold .....Stepwise setting with a step of 0.1V is possible
- Low Temperature-Drift-Coefficients of Output Voltage and Detector Threshold.....TYP. 100ppm/°C
- Low Dropout Voltage .....150mV at 120mA for VR1
  150mV at 100mA for VR2
- High Ripple Rejection .....65dB at 1kHz for VR1, VR2, VR5 and VR7
  60dB at 1kHz for VR6
- 3-wire serial interface .....Shut-down for each of regulators, except VR4
- Monitoring Supply Voltage.....Analog Output of Supply Voltage
- Package .....QFP 32pin with 0.5mm lead pitch

APPLICATIONS

- Portable Phones such as GSM, PDC and CDMA as well as other analog phones.
- Power supply for battery-powered appliances.

Notes: The product specifications described in this preliminary documents are subject to change without notice for reasons such as improvement.

BLOCK DIAGRAM



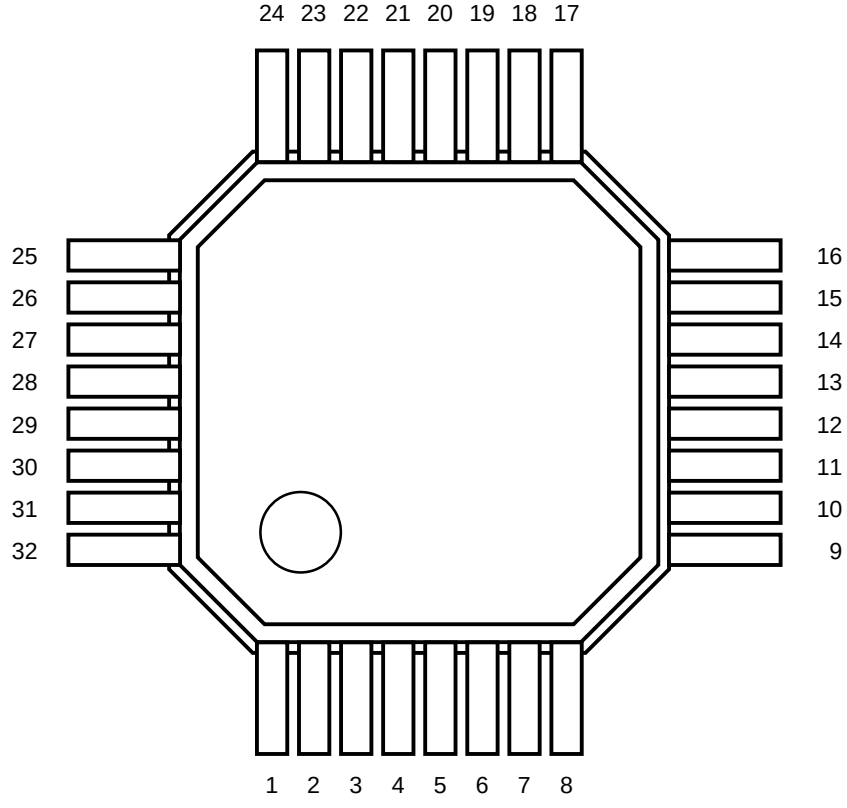
SELECTION GUIDE

In the R5312LXXXX series, Voltage settings for eight Regulators and two Detectors can be designated.
Part Number is designated as follows:

R5312L<u>X X X</u> <u>X</u> Part Number
| |
a b

Code	Descriptions
a	Serial Number for Voltage setting
b	Alphabetical Code for Mask Versions:

PIN CONFIGURATION



PIN DESCRIPTION

R5312LXXXA

Pin No.	Symbol	Descriptions
1	V_{DD3}	Power supply for VR5, VR6
2	I_{BC6}	Connected to Base of external PNP transistor for Voltage Regulator6, VR6.
3	R_{OUT6}	Output pin for VR6. Connected to Collector of external PNP transistor.
4	R_{OUT7}	Output pin for VR7
5	V_{DD4}	Power supply for VR7, VR8, Logic Block
6	R_{OUT8}	Output pin for VR8
7	V_{DD5}	Output pin for VR4, VD1, VD2, VD3
8	R_{OUT4}	Output pin for VR4
9	D_{OUT2}	Output pin for Voltage Detector2, VD2. CMOS output.
10	C_D	Pin for an external capacitor for output delay time setting of VD1
11	D_{OUT1}	Output pin for VD1. CMOS output.
12	GND2	Ground for Voltage Detectors and Logic Block
13	CSW6	Control switch input pin for VR6.
14	TIMER	Input pin for a blink signal of LED2.
15	DATA	The DATA pin inputs written data in synchronization with shift clock pulses from the SCK pin.
16	SCK	The SCK pin is used to input shift clock pulses to synchronize data input to the DATA Pin.
17	CSB	The CSB pin is used to interface with the CPU and is accessible when it is held at the Low Level. Pulled up through internal resistor.
18	R_{OUT1}	Output pin for VR1
19	CSW1	Control switch input pin for VR1. Pulled down through 300kΩ to the GND internally.
20	V_{DD1}	Power supply for VR1, VR2
21	CSW2	Control switch input pin for VR2. Output pin for VR2
22	R_{OUT2}	Output pin for VR2
23	R_{OUT3}	Output pin for VR3
24	V_{DD2}	Power supply for VR3, LED Drivers, Charge Pump Circuit
25	LED1	Output port for LED Driver1
26	LED2	Output port for LED Driver2
27	NC	No Connection

Pin No.	Symbol	Descriptions
28	GND3	Ground pin
29	NC	No Connection
30	GND1	Ground pin for VRs, LED Drivers
31	NC	No Connection
32	R_{OUT5}	Output pin for VR5

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Conditions	Ratings	Unit
V_{DD}	Supply Voltage		6.5	V
V_{IN}	Input Voltage	CSB, SCK, DATA, CSW1/2/6, TIMER	-0.3 to V_{DD}+0.3	V
I_{OUT1}	Output Current for VR1	R_{OUT1}	120	mA
I_{OUT2}	Output Current for VR2	R_{OUT2}	100	mA
I_{OUT3}	Output Current for VR3	R_{OUT3}	50	mA
I_{OUT4}	Output Current for VR4	R_{OUT4}	20	mA
I_{OUT5}	Output Current for VR5	R_{OUT5}	50	mA
I_{OUT7}	Output Current for VR7	R_{OUT7}	60	mA
I_{OUT8}	Output Current for VR8	R_{OUT8}	150	mA
P_D	Power Dissipation	Mounted on a substrate Topt=+25°C	1000	mW
		In the open air Topt=+25°C	500	mW
Topt	Operating Temperature		-40 to +85	°C
Tstg	Storage Temperature		-55 to +125	°C
Tsolder	Soldering Temperature		260°C 10sec (Lead)	

OVERALL CHARACTERISTICS

R5312LXXXA series

Symbol	Item	Conditions	MIN.	TYP.	MAX	Unit
V_{DD}	Operating Voltage		1.5*Note3		6.0	V
Istandby	Standby Current	All regulators are disabled except VR4 at no load		10	20	μA
R_{SET1}	Output Voltage setting range	for VR1	2.5		3.3	V
R_{SET2}	Output Voltage setting range	for VR2	2.5		3.3	V
R_{SET3}	Output Voltage setting range	for VR3	2.5		3.3	V
R_{SET4}	Output Voltage setting range	for VR4	2.5		3.3	V
R_{SET5}	Output Voltage setting range	for VR5	2.5		3.3	V
R_{SET6}	Output Voltage setting range	for VR6	2.5		3.3	V
R_{SET7}	Output Voltage setting range	for VR7	2.5		3.3	V
R_{SET8}	Output Voltage setting range	for VR8 compatible with 1.3V Vibrator driver	1.2		1.7	V
V_{SET1}	Detect Voltage setting range	for VD1, High to Low	1.2		3.3	V
V_{SET2}	Detect Voltage setting range	for VD2, High to Low	1.2		3.3	V
V_{SET3}	Reset Voltage setting range	for VD3, High to Low	5.3		6.6	V

Note1: All of above setting voltages can be designated by user's requirement.
Note2: The Reset voltage is equal to the Detect Voltage in the VD3 because there is no hysteresis in the VD3.
Note3: This value means the minimum operating voltage of VD1, VD2, and VD3.

ELECTRICAL CHARACTERISTICS

R5312L001A

Voltage Regulator1/ VR1: 120mA output for RF / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT1}	Output Voltage		2.94	3.00	3.06	V
V_{DIF1}	Dropout Voltage	I_{OUT1}=120mA		150	200	mV
Iss1	Supply Current			80	160	μA
Ilim1	Current Limit	V_{ROUT1}=0V		60		mA
RR1	Ripple Rejection1	V_{DD} with sinusoidal 0.2Vpp, f=1kHz		65		dB
$\Delta V_{OUT1}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT1} ≤ 120mA			40	mV
$\Delta V_{OUT1}/\Delta V_{IN}$	Line Regulation	R_{OUT1}+0.2V ≤ V_{DD} ≤ 6.0V		0.05	0.2	%/V
$\Delta V_{OUT1}/\Delta Topt$	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT1}=60mA.

Voltage Regulator2/ VR2: 100mA output for RF / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT2}	Output Voltage		2.94	3.00	3.06	V
V_{DIF2}	Dropout Voltage	I_{OUT2}=100mA		150	200	mV
Iss2	Supply Current			80	160	μA
Ilim2	Current Limit	V_{ROUT2}=0V		40		mA
RR2	Ripple Rejection2	V_{DD} with sinusoidal 0.2Vpp, f=1kHz		65		dB
$\Delta V_{OUT2}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT2} ≤ 100mA			40	mV
$\Delta V_{OUT2}/\Delta V_{IN}$	Line Regulation	R_{OUT2}+0.2V ≤ V_{DD} ≤ 6.0V		0.05	0.2	%/V
$\Delta V_{OUT2}/\Delta Topt$	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT2}=50mA.

Voltage Regulator3/ VR3: 50mA output for Analog Block II / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT3}	Output Voltage		2.94	3.00	3.06	V
V_{DIF3}	Dropout Voltage	I_{OUT3}=50mA		150	200	mV
Iss3	Supply Current			40	80	μA
Ilim3	Current Limit	V_{ROUT3}=0V		25		mA
RR3	Ripple Rejection3	V_{DD} with sinusoidal 0.2Vpp, f=1kHz		55		dB
$\Delta V_{OUT3}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT3} ≤ 50mA			40	mV
$\Delta V_{OUT3}/\Delta V_{IN}$	Line Regulation	R_{OUT3F}+0.2V ≤ V_{DD} ≤ 6.0V		0.05	0.2	%/V
$\Delta V_{OUT3}/\Delta$Topt	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT3}=25mA.

Voltage Regulator4/ VR4: 20mA output for Digital Block / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT4}	Output Voltage		2.940	3.000	3.060	V
V_{DIF4}	Dropout Voltage	I_{OUT4}=20mA		150	200	mV
Iss4	Supply Current			6	15	μA
Ilim4	Current Limit	V_{ROUT4}=0V		20		mA
RR4	Ripple Rejection4	V_{DD} with sinusoidal 0.2Vpp, f=1kHz		40		dB
$\Delta V_{OUT4}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT4} ≤ 20mA			40	mV
$\Delta V_{OUT4}/\Delta V_{IN}$	Line Regulation	R_{OUT4F}+0.2V ≤ V_{DD} ≤ 6.0V		0.2	0.4	%/V
$\Delta V_{OUT4}/\Delta$Topt	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT4}=10mA.

Voltage Regulator5/ VR5: 50mA output for Analog Block II / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT5}	Output Voltage		2.744	2.800	2.856	V
V_{DIF5}	Dropout Voltage	I_{OUT5}=50mA		150	200	mV
Iss5	Supply Current			40	80	μA
Ilim5	Current Limit	V_{ROUT5}=0V		25		mA
RR5	Ripple Rejection5	V_{DD} with sinusoidal 0.2Vpp, f=1kHz		65		dB
$\Delta V_{OUT5}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT5} ≤ 50mA			40	mV
$\Delta V_{OUT5}/\Delta V_{IN}$	Line Regulation	R_{OUT5}+0.2V ≤ V_{DD} ≤ 6.0V		0.05	0.2	%/V
$\Delta V_{OUT5}/\Delta Topt$	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT5}=25mA.

Voltage Regulator6/ VR6: 300mA output for Base Band with External PNP Transistor / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT6}	Output Voltage		2.744	2.800	2.856	V
V_{DIF6}	Dropout Voltage	I_{OUT6}=300mA		150	200	mV
Iss6	Supply Current			8	16	μA
Ilim6	Current Limit	V_{ROUT6}=0V	3	7	20	mA
RR6	Ripple Rejection6	V_{DD} with sinusoidal 0.2Vpp, f=1kHz		60		dB
$\Delta V_{OUT6}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT6} ≤ 300mA			40	mV
$\Delta V_{OUT6}/\Delta V_{IN}$	Line Regulation	R_{OUT6}+0.2V ≤ V_{DD} ≤ 6.0V		0.05	0.2	%/V
$\Delta V_{OUT6}/\Delta Topt$	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT6}=150mA.

Voltage Regulator7/ VR7: 60mA output for Digital Block / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT7}	Output Voltage		2.744	2.800	2.856	V
V_{DIF7}	Dropout Voltage	I_{OUT7}=60mA		150	200	mV
Iss7	Supply Current			40	80	μA
Ilim7	Current Limit	V_{ROUT7}=0V		30		mA
RR7	Ripple Rejection5	V_{DD} with sinusoidal 0.2Vpp, f=1kHz		65		dB
$\Delta V_{OUT7}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT7} ≤ 60mA			40	mV
$\Delta V_{OUT7}/\Delta V_{IN}$	Line Regulation	R_{OUT7}+0.2V ≤ V_{DD} ≤ 6.0V		0.05	0.2	%/V
$\Delta V_{OUT7}/\Delta$Topt	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT7}=30mA.

Voltage Regulator8/ VR8: 150mA output for Vibrator / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{ROUT8}	Output Voltage		1.643	1.700	1.757	V
V_{DIF8}	Dropout Voltage	I_{OUT8}=150mA		1300		mV
Iss8	Supply Current			5	15	μA
Ilim8	Current Limit	V_{ROUT8}=0V		75		mA
RR8	Ripple Rejection5	V_{DD} with sinusoidal 0.2Vpp, f=120Hz		40		dB
$\Delta V_{OUT8}/\Delta I_{OUT}$	Load Regulation	1mA ≤ I_{OUT8} ≤ 150mA			60	mV
$\Delta V_{OUT8}/\Delta V_{IN}$	Line Regulation	3.0V ≤ V_{DD} ≤ 6.0V		0.05	0.2	%/V
$\Delta V_{OUT8}/\Delta$Topt	Output Voltage Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm/°C

Unless otherwise provided, V_{DD}=3.6V I_{OUT8}=75mA.

Voltage Detector1/ VD1: for CPU Reset with external capacitor / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DET1}	Detect Voltage		1.960	2.000	2.040	V
V_{HYS1}	Hysteresis Range		$V_{DET1}\times$ 1.5%	$V_{DET1}\times$ 3%	$V_{DET1}\times$ 5%	V
T_{VDET1}	Output Delay time	C_D=0.15μF	60	100	180	ms
$\Delta V_{DET1}/\Delta Topt$	Detector Threshold Temperature Coefficient	Topt= -40 to +85°C		±100		ppm/°C

Voltage Detector2/ VD2: for Battery Low Voltage Detection / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DET2}	Detect Voltage		3.136	3.200	3.264	V
V_{HYS2}	Hysteresis Range		$V_{DET2}\times$ 1.5%	$V_{DET2}\times$ 3%	$V_{DET2}\times$ 5%	V
$\Delta V_{DET2}/\Delta Topt$	Detector Threshold Temperature Coefficient	Topt= -40 to +85°C		±100		ppm/°C

Voltage Detector3/ VD3: for Excess input Voltage Detection / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DET3}	Reset Voltage		6.048	6.300	6.552	V
$\Delta V_{DET3}/\Delta Topt$	Detector Threshold Temperature Coefficient	Topt= -40 to +85°C		±100		ppm/°C

Output port 1/ 7mA: for LED Driver1 / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
I_{POH1}	"H" Output Current	V_{OH1}=2V	5.6	7	8.4	mA
R_{PO1}	Pull-Down Resistance		3	5	8	kΩ

Output port 2/ 10mA: for LED Driver2 / R5312L001A Topt=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
I_{POH2}	"H" Output Current	V_{OH2}=2V	8	10	12	mA
R_{PO2}	Pull-Down Resistance		3	5	8	kΩ

Digital Input / Output Conditions / R5312L001A Topt=25°C

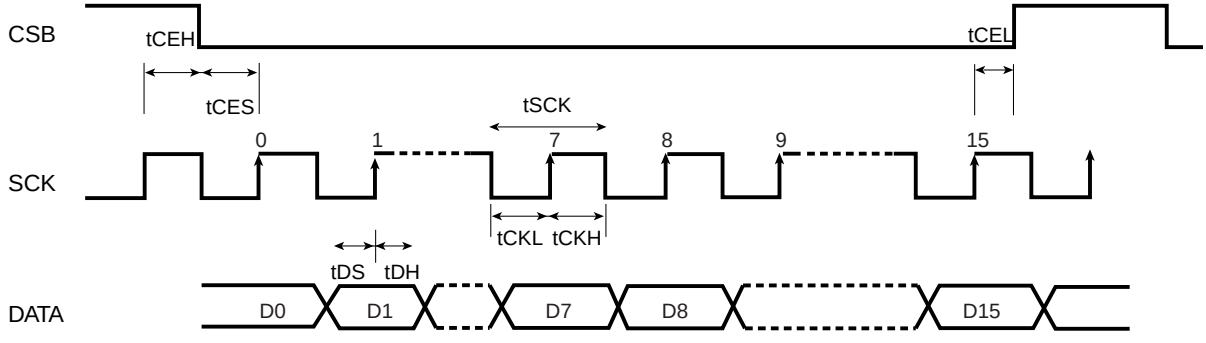
Symbol	Item	Pins	MIN.	TYP.	MAX.	Unit
V_{IH1}	'H' Input Voltage	CSW1, 2, TIMER	0.8× V_{ROUT6}		V_{DD}+ 0.3	V
V_{IH2}	'H' Input Voltage	CSW6	0.8× V_{ROUT6}		V_{DD}+ 0.3	V
V_{IH3}	'H' Input Voltage	CSB, SCK, DATA	0.8× V_{ROUT6}		R_{OUT6}*1	V
V_{IL1}	'L' Input Voltage	CSW1, 2, TIMER, SCK, DATA, CSB	-0.3		0.2× V_{ROUT6}	V
V_{IL2}	'L' Input Voltage	CSW6	-0.3		0.2× V_{DD}	V
V_{HYS1}	Hysteresis range	CSW1, 2, TIMER, SCK, DATA, CSB		0.25× V_{ROUT6}		V
V_{HYS2}	Hysteresis range	CSW6		0.25× V_{DD}		V
V_{OH}	'H' Output Voltage	D_{OUT1}, D_{OUT2}, I_{OH}= -0.2mA	V_{ROUT6}- 0.4			V
V_{OL}	'L' Output Voltage	D_{OUT1}, D_{OUT2}, I_{OL}=1mA			0.4	V
R_{PU}	Pull-up Resistance	CSB, SCK, DATA	0.12	0.3	0.8	MΩ
R_{PD1}	Pull-down Resistance	CSW1, 2, TIMER	0.12	0.3	0.8	MΩ
R_{PD2}	Pull-down Resistance	CSW6	0.24	0.6	1.6	MΩ

*1: The pins specified as above are pulled up to the R_{OUT6} pin through resistors internally. Therefore the higher input voltage than V_{ROUT6} cause a rising of V_{ROUT6} incorrectly ,particularly with small load current.

AC CHARACTERISTICS / R5312L001A V_{DD}=3.6V, Vss=0V, C_L=20pF, Topt=25°C

Symbol	Item	MIN.	TYP.	MAX.	Unit
t_{CEH}	SCK to CSB 'H' hold time	100			ns
t_{CES}	CSB to SCK setup time	200			ns
t_{CEL}	SCK to CSB 'L' hold time	100			ns
t_{CR}	CSB recovery time	100			ns
t_{SCK}	SCK cycle	500			ns
t_{CKL}	SCK 'L' time	250			ns
t_{CKH}	SCK 'H' time	250			ns
t_{DS}	DATA to SCK setup time	100			ns
t_{DH}	SCK to DATA hold time	100			ns

Timing Diagram



Refer to the specification of "Digital AC Characteristics"

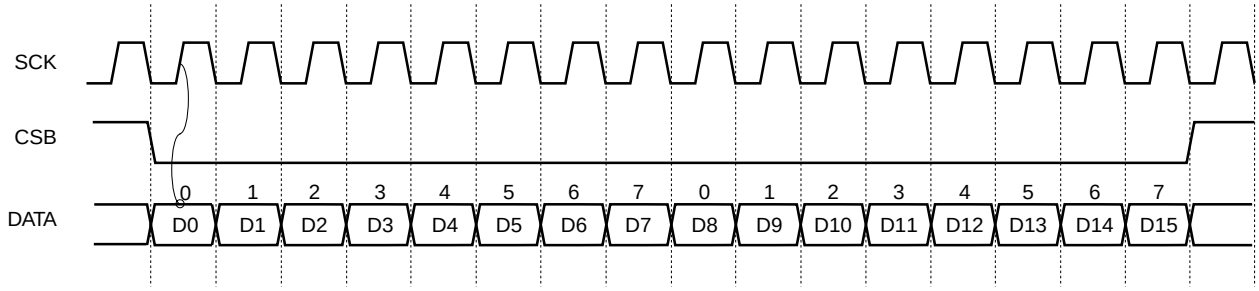
V_{IH}=0.8×V_{ROUT6}

V_{IL}=0.2×V_{ROUT6}

FUNCTIONAL DESCRIPTION

1. Serial Interface

1-1. Data Transfer Summary



All data transfers are initiated by driving the CSB input low. The CSB input serves two functions. First, CSB turns on the control logic which allows access to the shift register for the address/command sequence. Second, the CSB signal provides a method of terminating data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock.

All data transfer terminates if the CSB input is high. Data transfer is illustrated as above.

1-2. Command Byte

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The Command byte is shown as above. Each data transfer is initiated by a command byte.

The LSB (Bit 0) must be a logic zero. An any data for each of bit six and bit seven which might be zero or one, is ignored. Bits one through five can be specified by the designated registers to be input.

The command byte is always input starting with the LSB (bit zero).

1-3. Data Input

Following the eight SCK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCK cycles. And any successive instruction set which consists of command byte and data byte is allowable. The data byte is always input starting with the LSB (bit zero).

1-4. Regulators Switch

Each of regulators can be enabled or disabled independently. By the VR switch register, designations for each of six regulators' ON/OFF can be written to bit 8 through 13.

1-5. LED Driver Switch

Constant Current Output of each of LED drivers can be enabled or disabled independently. These switches are controlled with Output Port registers. Bit 14 and 15 are for designation of ON/OFF of LED drivers.

1-6. Register Address / Register Definition

VR and LED Driver switch Register Address

D7	D6	D5	D4	D3	D2	D1	D0
-	-	0	0	0	1	0	-

VR and LED Driver switch Register Definition

D7	D6	D5	D4	D3	D2	D1	D0
LED1	LED2	VR8	VR7	VR5	VR3	VR2	VR1
1:LED1=ON 0:LED1=OFF	1:LED2=ON 0:LED2=OFF	1:VR8=ON 0:VR8=OFF	1:VR7=ON 0:VR7=OFF	1:VR5=ON 0:VR5=OFF	1:VR3=ON 0:VR3=OFF	1:VR2=ON 0:VR2=OFF	1:VR1=ON 0:VR1=OFF

1-6. Operation after Interrupt Procedure

In the case that CSB input becomes to high by interrupting while a command-set which has not yet been acknowledged, the command-set is disabled by internal reset signal, therefore, after this case, transaction should be executed from the initial condition.

2. Voltage Regulators

Embedded 8 regulators are classified into 6 groups as follows by their characteristics:

[High Speed and Low Noise Type] VR1, 2
With High ripple rejection (Typ. 65dB at 1kHz) and Low Noise, they are suitable for RF circuits.

[High Speed Type I] VR3
With High ripple rejection (Typ. 55dB at 1kHz) and Low Noise, they are suitable for analog circuits.
And the load transient response is also good, therefore they are recommendable for DSP which requires fast dynamic response to load current.

[High Speed Type II] VR5, 7
With High ripple rejection (Typ. 65dB at 1kHz) and Low Noise, they are suitable for analog circuits.
And the load transient response is also good, therefore they are recommendable for DSP which requires fast dynamic response to load current.

[Ever ON Type] VR4
VR4 is used as ever-ON regulator, therefore its supply current is enough minimized to save invalid current by design (Typ. 6μA).

[Boost Type] VR6
VR6 is used with an external PNP transistor and can supply large output current.

[For Vibrator] VR8

VR8 can drive a vibrator (which requires 1.3V as a supply voltage) directly.

3. Voltage Detectors

VD1 monitors the voltage of VR6, when the voltage becomes lower than setting detector threshold voltage, D_{OUT1} pin becomes "L", and internal logic is initialized, furthermore does not accept input signal. It is suitable for reset CPU. Output type is Nch open drain and pull-up resistance to VR6. Setting output delay time (Reset Released Delay Time) is possible with connecting an external capacitance to C_D pin. The formula which shows the relation between External capacitance value (C_D) and output delay time is as follows:

$$tD = 0.67 \times 10^6 \times C_D$$

VD2 monitors V_{DD} voltage, when the voltage becomes lower than setting output voltage threshold, D_{OUT2} becomes "L", and disables VR6. It is suitable for detecting cutting off a battery voltage in a flash and can be used to set a operation starting voltage. Output Type is CMOS and its "H" level equals to voltage of R_{OUT6}.

VD3 monitors also V_{DD} voltage, when the voltage becomes higher than setting output threshold, VD3 disables VR6. It is necessary to protect circuits from too large input voltage.

5. LED Drivers

Two LED drivers are embedded and each of them can control independently, and ON/OFF condition can be controlled via 3-wire interface. LED1 is 7mA Constant Current Output. LED2 is applicable for display of receiving a call and 10mA Constant Current Output. Output is controlled with "ON" command or input signal for TIMER pin via 3-wire interface, lighting and flashing can be set freely.

TECHNICAL NOTES

- **Operation with rising and falling of Supply Voltage**

1. Supply voltage condition --- from 0V to a designated voltage

To make the explanation be easier, we call a voltage which is monitored and rising voltage threshold, as "Released Voltage". On the contrary, we call the falling voltage threshold as "Detector Threshold Voltage". And the difference between them is specified as a Hysteresis Voltage.

While the supply voltage is from 0V to VD2 (Released Voltage), all the circuits except VDs are "OFF" state, thus both levels of D_{OUT1} and 2 are "L". However, we cannot guarantee the operation with a V_{DD} at voltage below the minimum operating voltage (V_{DDMIN}) with both a rising and a falling conditions. When the supply voltage crosses over the Released Voltage for VD2, D_{OUT2} becomes "H" and VR6 is enabled.

Further, when R_{OUT6} crosses over the Released Voltage for VD1, after a setting delay time by an external capacitor to C_D pin, D_{OUT1} becomes "H", then internal logic circuits and reset condition for input control pins (3-wire interface inputs and CSWX etc.) are released. Therefore circuits' operations can become to control by these input pins.

2. Supply voltage condition --- from a designated voltage to 0V

When the supply voltage becomes lower than Detector Threshold Voltage for VD2, D_{OUT2} becomes "L" and disables VR6. Further, VR6 level becomes lower than Detector Threshold Voltage for VD1, then D_{OUT1} becomes "L" and reset internal logic circuits and input controller pins (3-wire inputs and CSWX etc.)

Then all the circuits except VDs are OFF (See the Note below), and input signals for control are not accepted.

The lower voltage than this is as same as above.

Summary

Operation of VD1

VD1 senses R_{OUT6} and D_{OUT1} is at "L" when R_{OUT6} is equal or less than its Detector Threshold Voltage.

Under this condition, when CSW6 is at "L", all VDs and VR4 are ON, others are at OFF state. Input Control Circuits (3-wire input, CSW1, 2, and TIMER) are disabled except CSW6 and any input is not accepted.

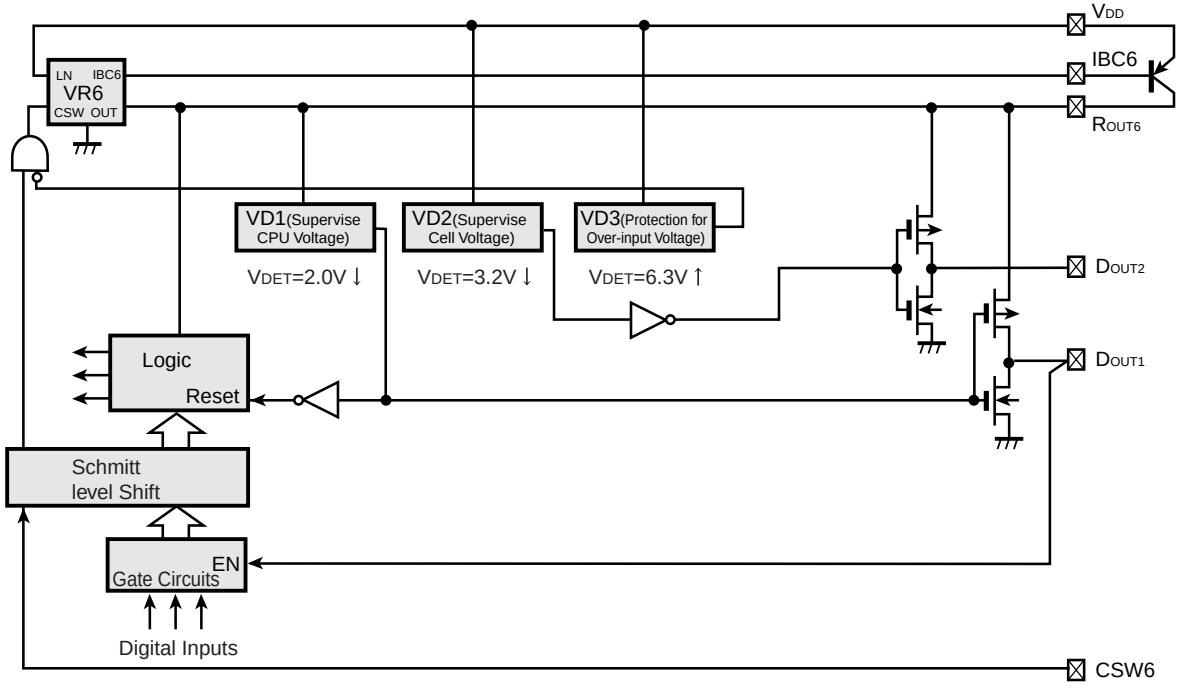
After that, CSW6 is made to be at "H", VR3, 5, 6, and 7 turn on. When R_{OUT6} is beyond the Released Voltage, D_{OUT1} becomes "H", and input controls are accepted.

Operation of VD2

VD2 senses V_{DD} and D_{OUT2} is at "L" when V_{DD} is equal or less than its Detector Threshold Voltage.

When V_{DD} is beyond the Released Voltage, D_{OUT1} becomes "H", however, when CSW6 level is at "L", D_{OUT2} becomes "L" (High Impedance State). There is no effect against the operation of circuits including VRs by VD2 operation.

- **Block Diagram of VDs**



TEST CIRCUITS

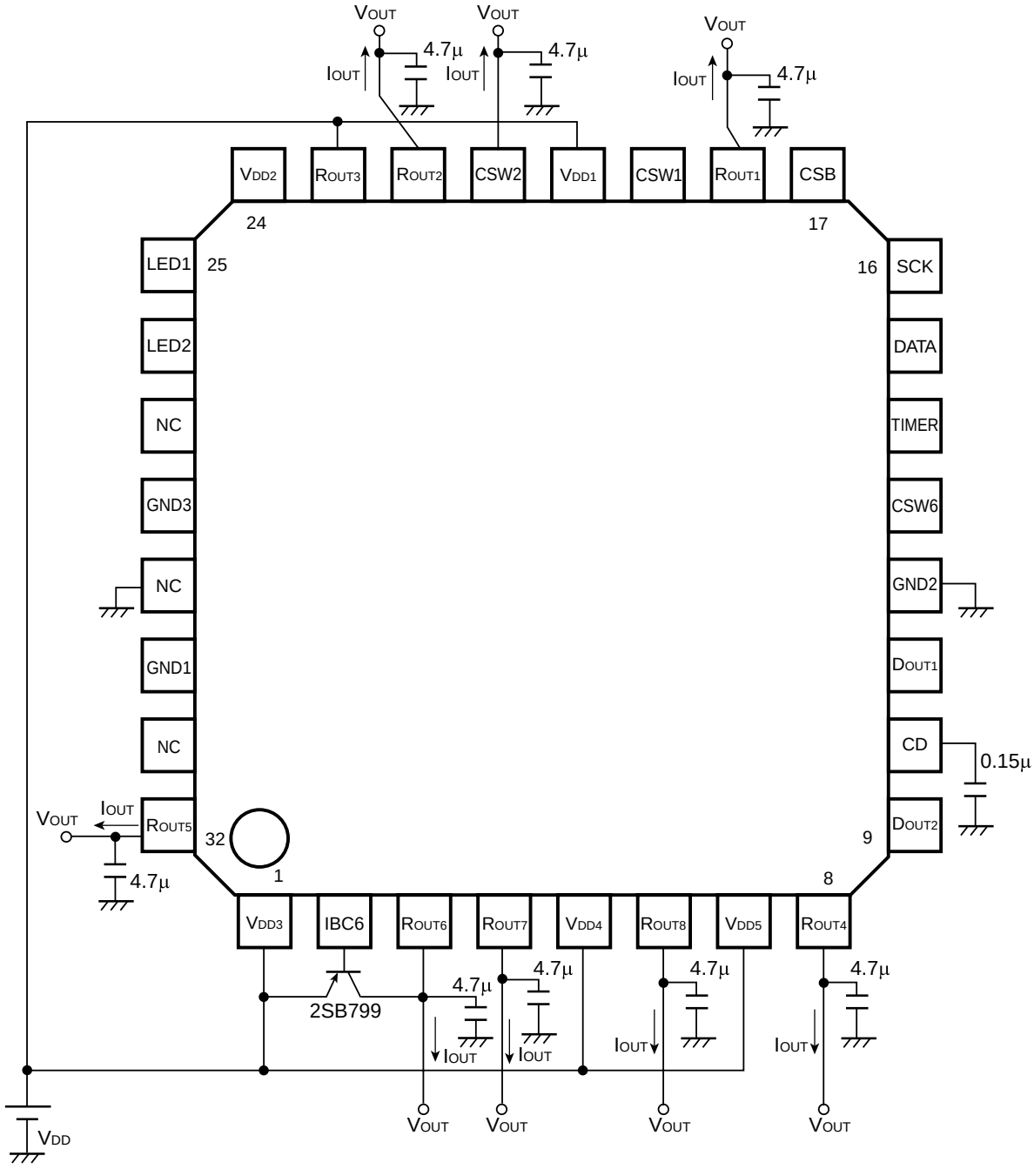


Figure-1 : Standard Test Circuit

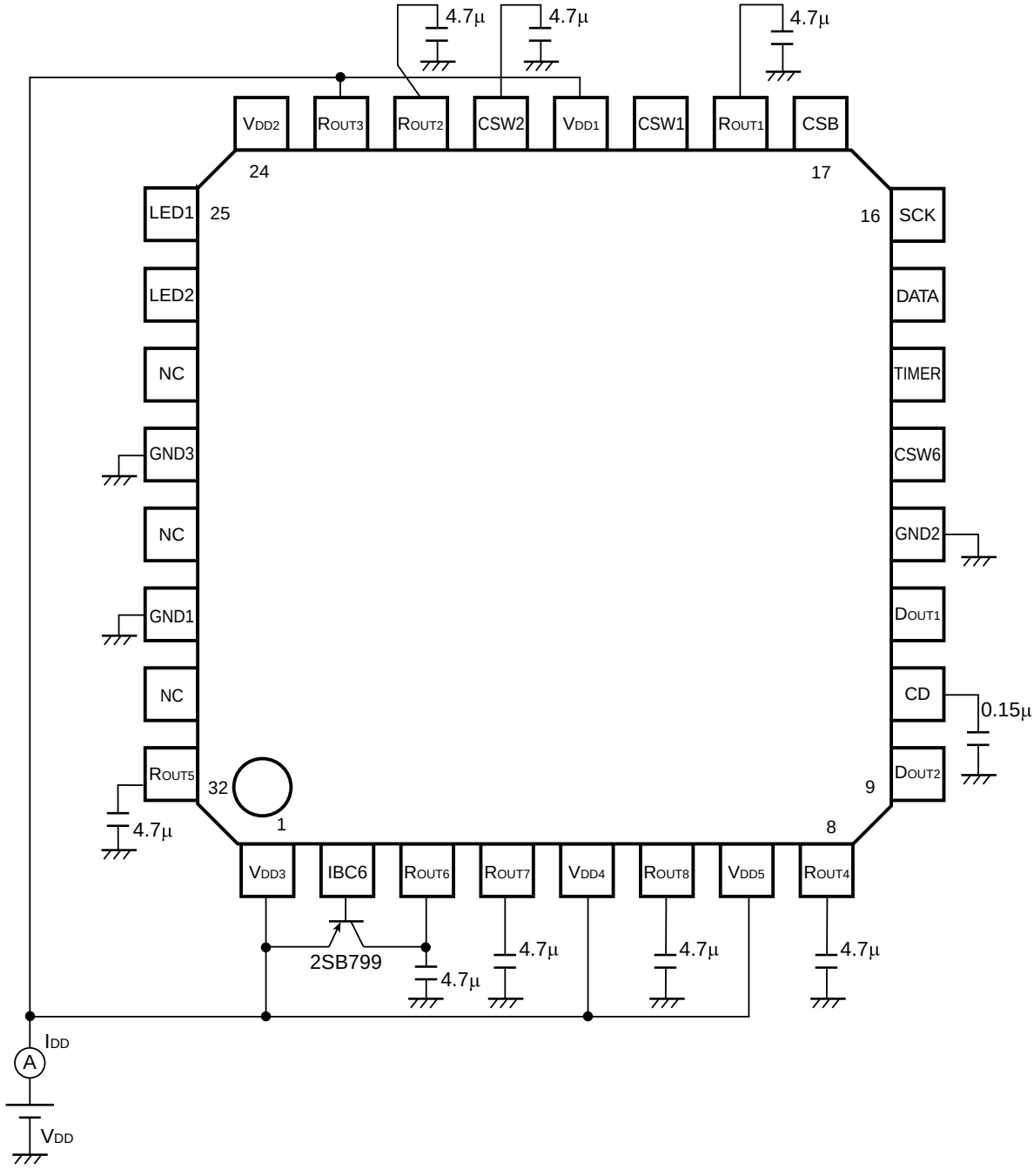


Figure-2 : Test Circuit for Supply Current

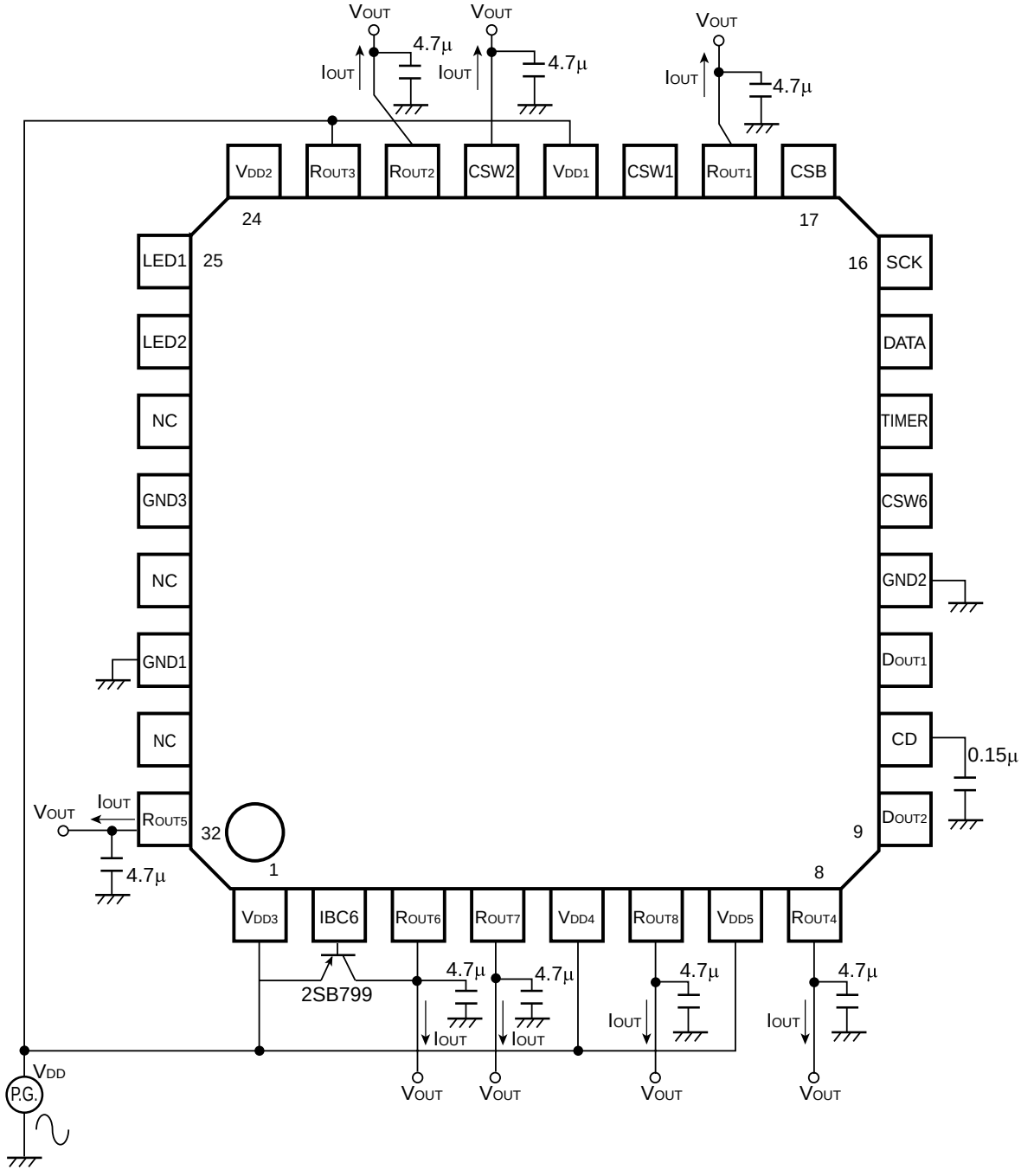


Figure-3 : Test Circuit for Ripple Rejection

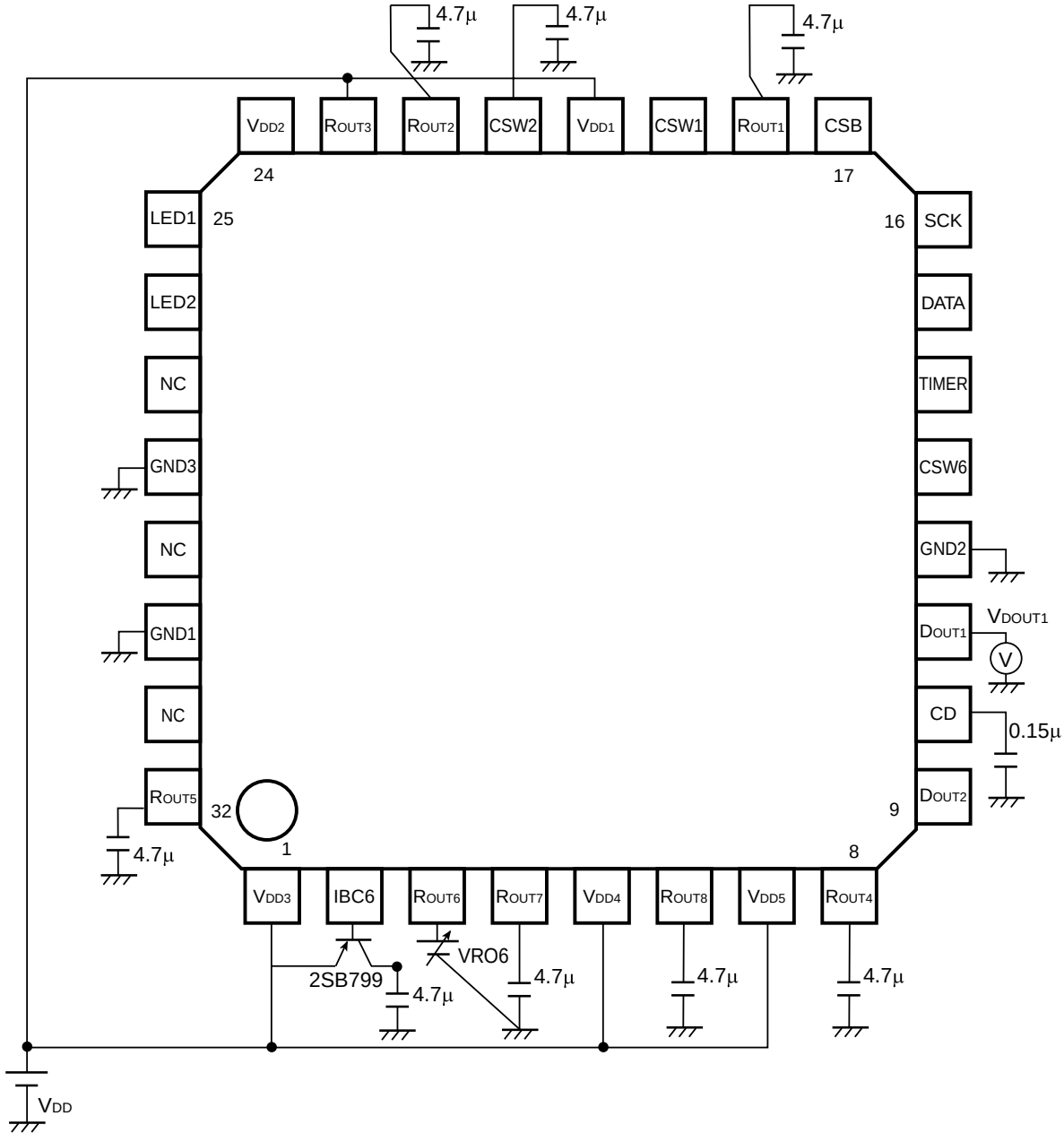


Figure-4 : Test Circuit for VD1

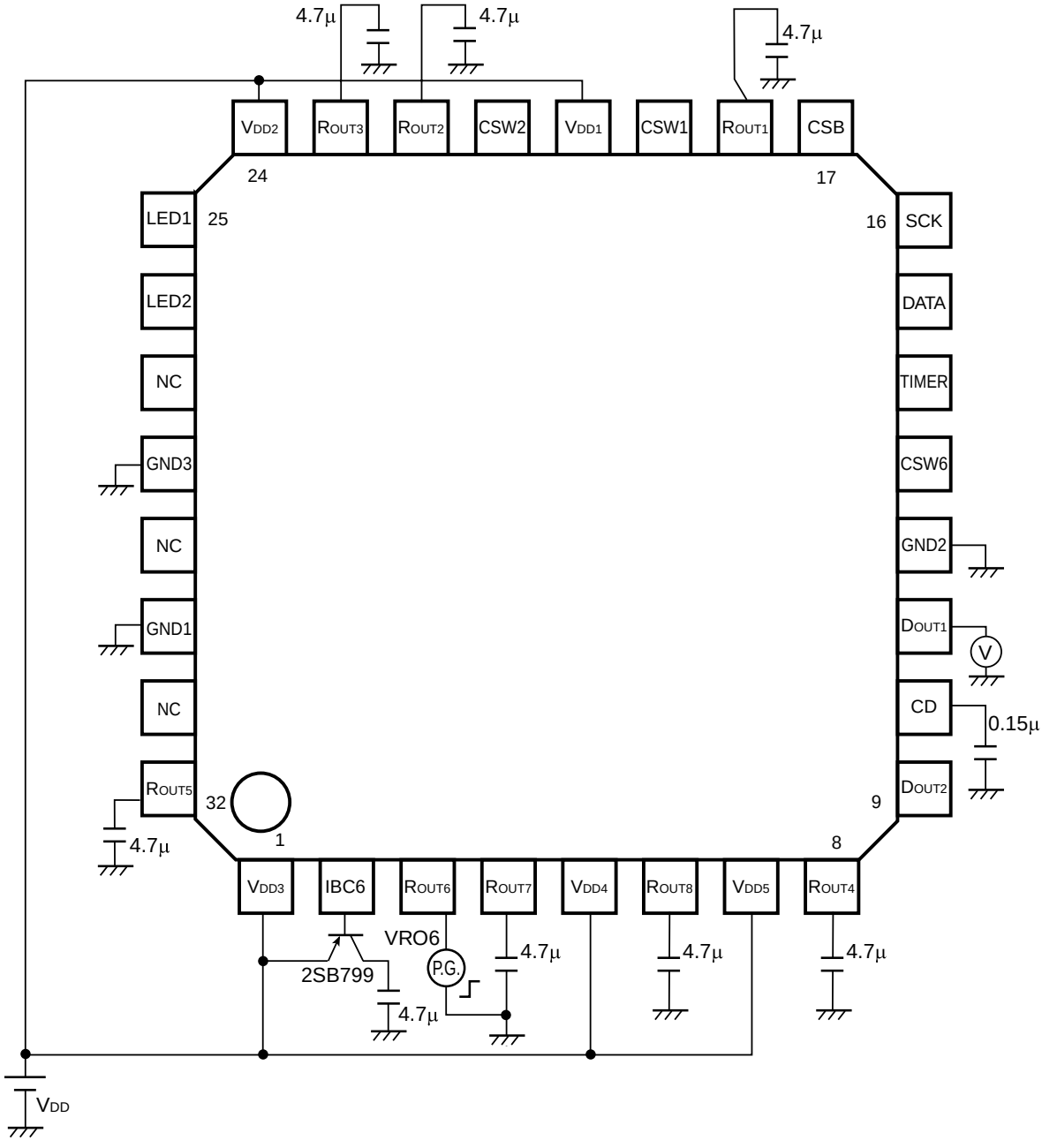


Figure-5 : Test Circuit for Output Delay Time of VD1 Released Voltage

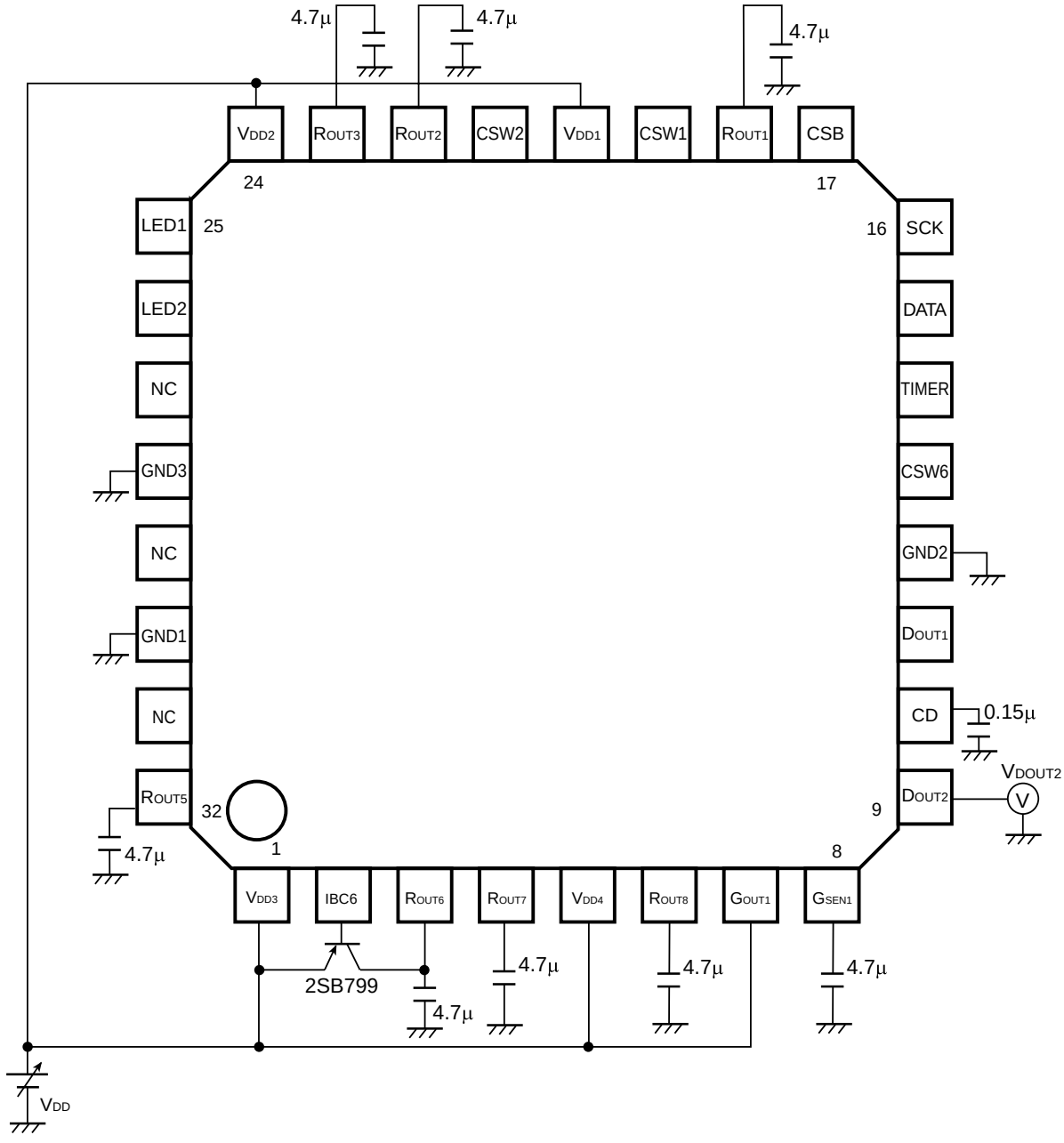


Figure-6 : Test Circuit for VD2 and VD3

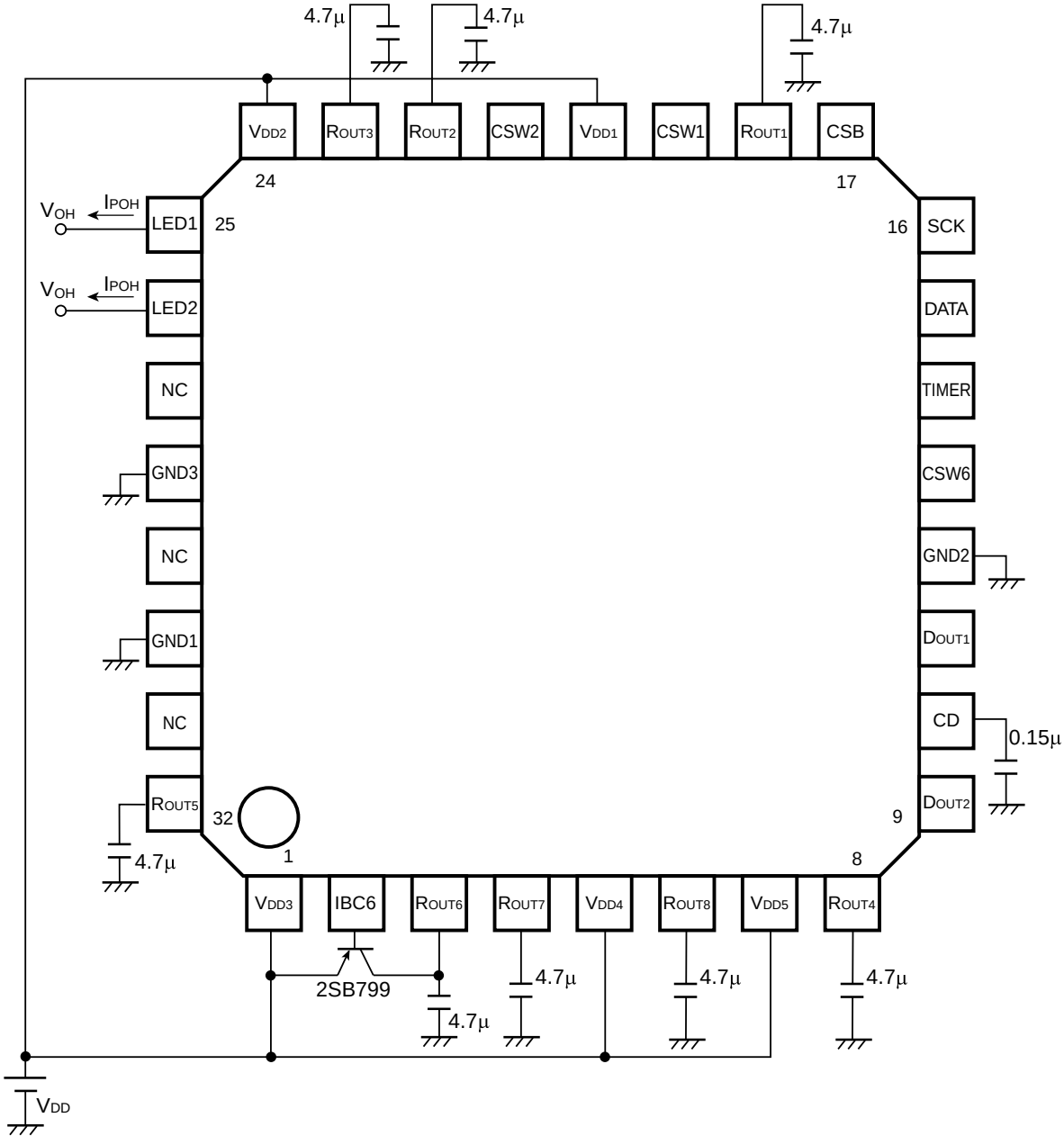
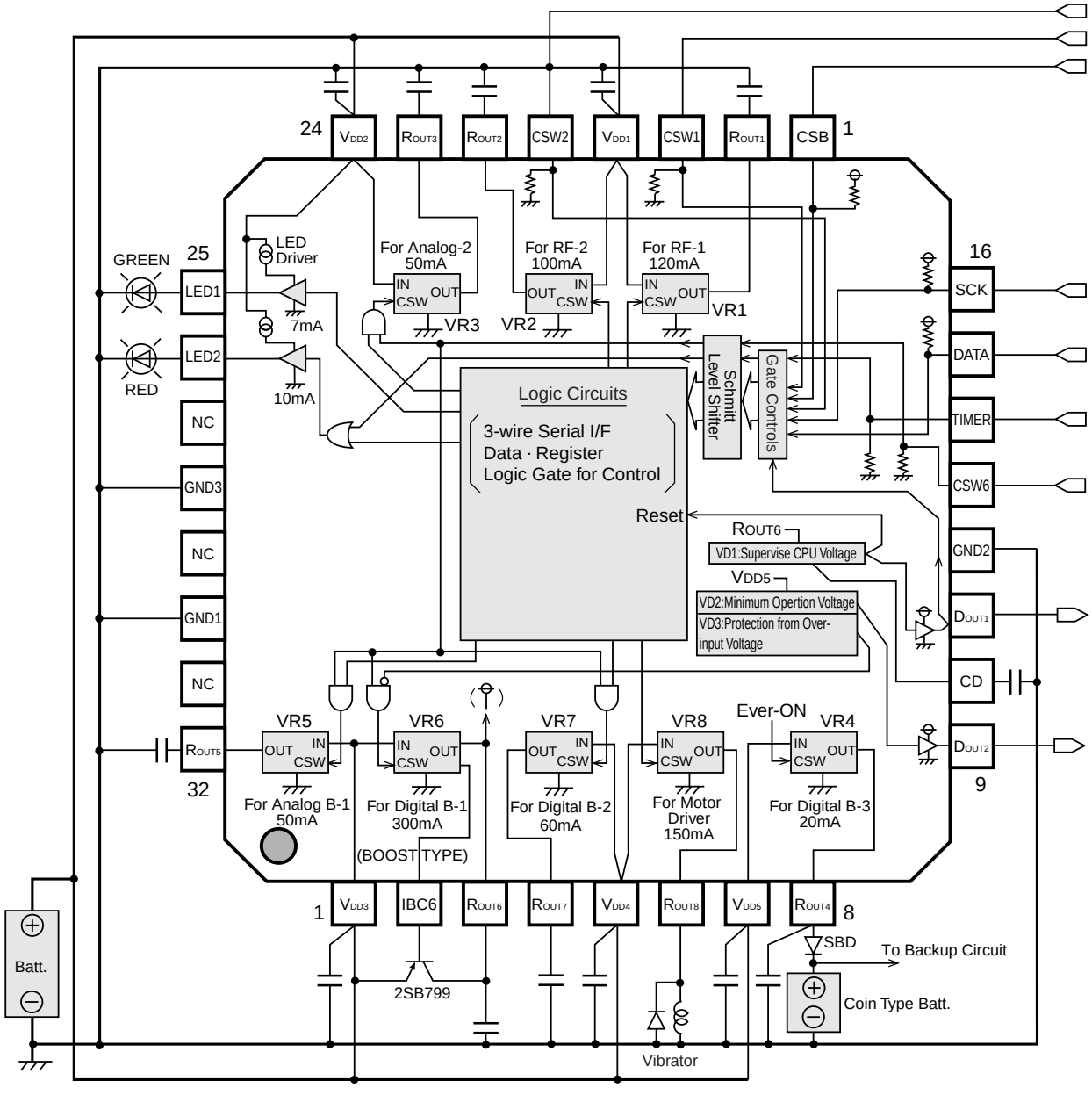


Figure-7 : Test Circuit for LED Drivers

TYPICAL APPLICATION

- **R5312LxxxA**

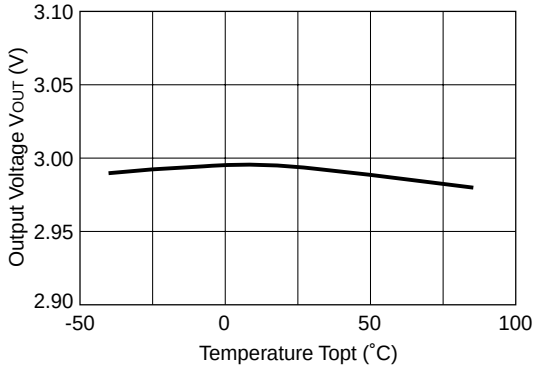


TYPICAL CHARACTERISTICS

1) Output Voltage vs. Temperature

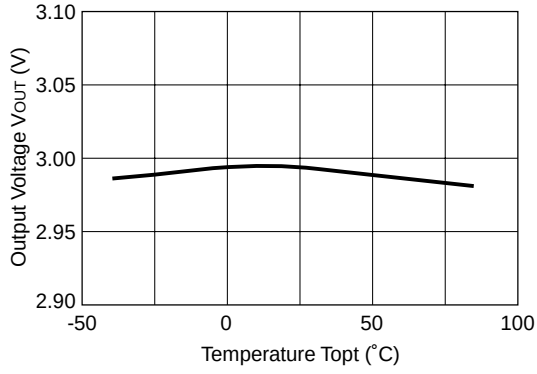
Regulator1 (3.0V)

V_{DD}=3.6V I_{OUT}=60mA



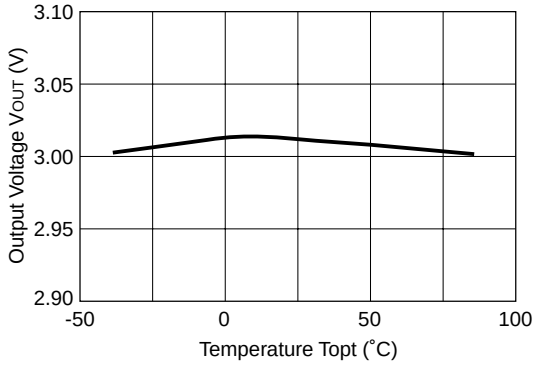
Regulator2 (3.0V)

V_{DD}=3.6V I_{OUT}=50mA



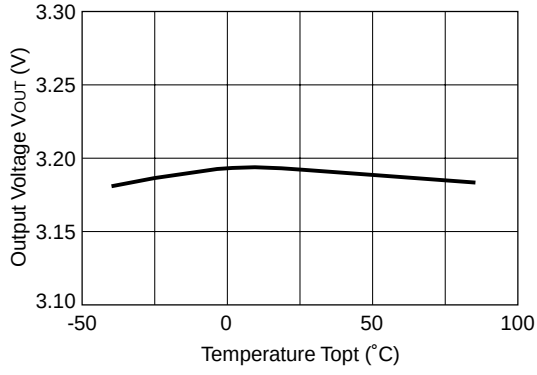
Regulator3 (3.0V)

V_{DD}=3.6V I_{OUT}=25mA



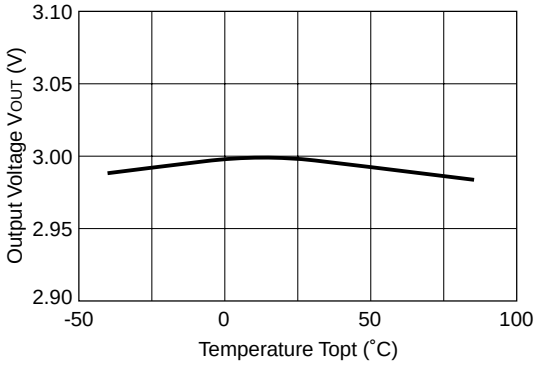
Regulator4 (3.2V)

V_{DD}=3.6V I_{OUT}=10mA



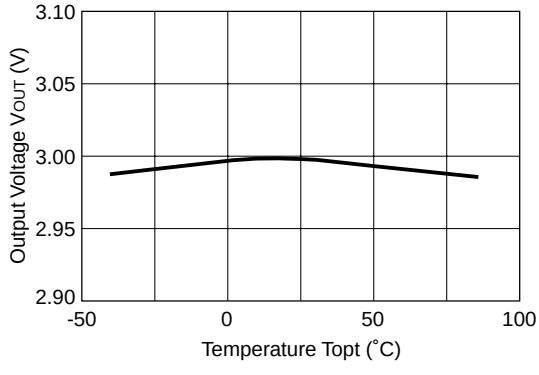
Regulator5 (3.0V)

V_{DD}=3.6V I_{OUT}=25mA



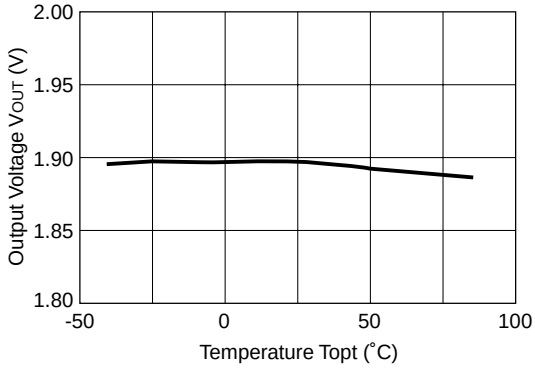
Regulator6 (3.2V)

V_{DD}=3.6V I_{OUT}=150mA



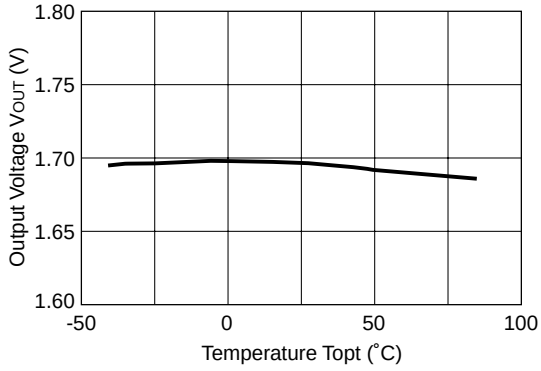
Regulator7 (1.9V)

V_{DD}=3.6V I_{OUT}=30mA



Regulator8 (1.7V)

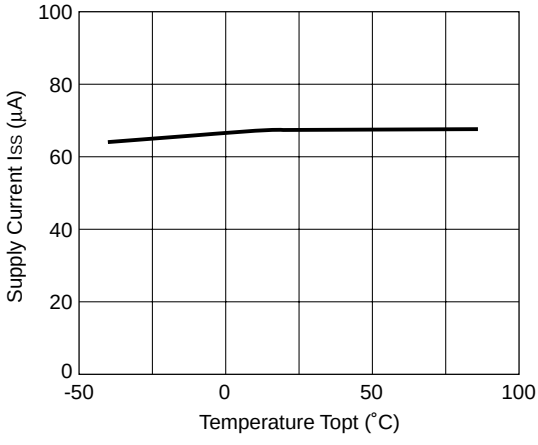
V_{DD}=3.6V I_{OUT}=75mA



2) Supply Current vs. Temperature

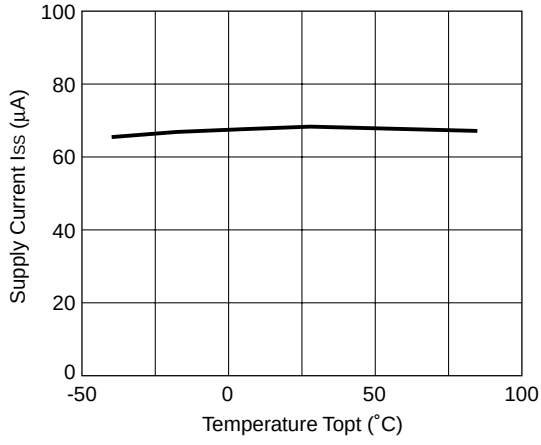
Regulator1 (3.0V)

V_{DD}=3.6V



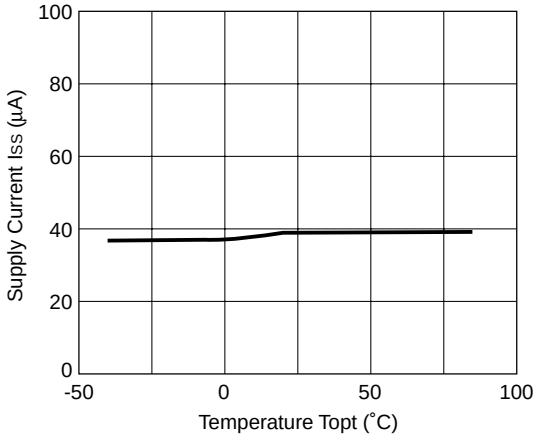
Regulator2 (3.0V)

V_{DD}=3.6V



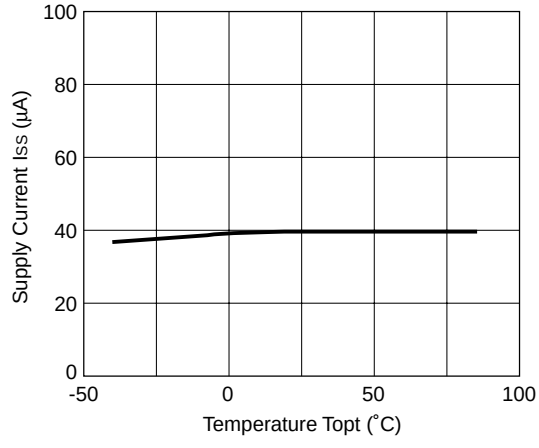
Regulator3 (3.0V)

V_{DD}=3.6V

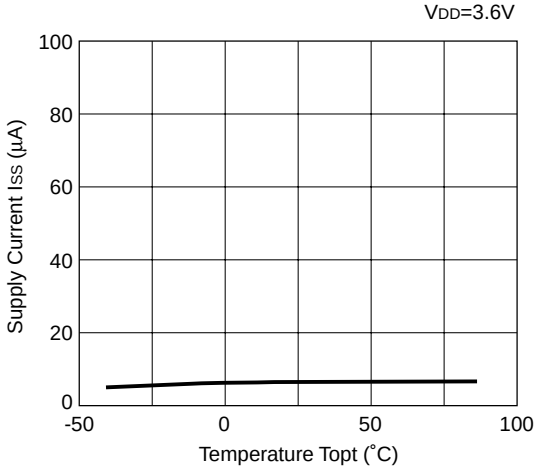


Regulator5 (3.0V)

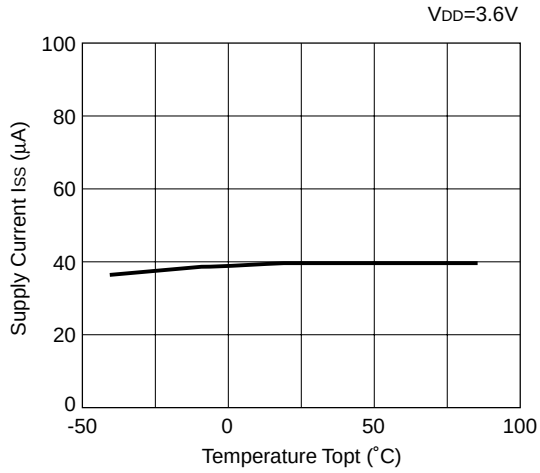
V_{DD}=3.6V



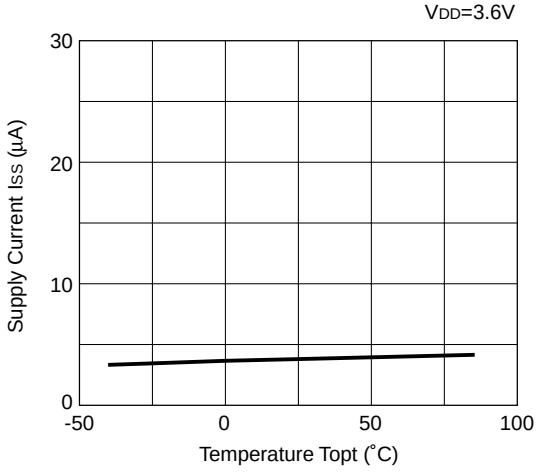
Regulator6 (3.0V)



Regulator7 (1.9V)

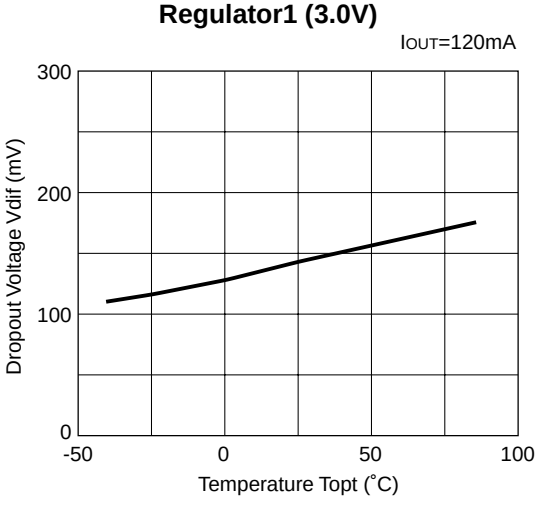


Regulator8 (1.7V)

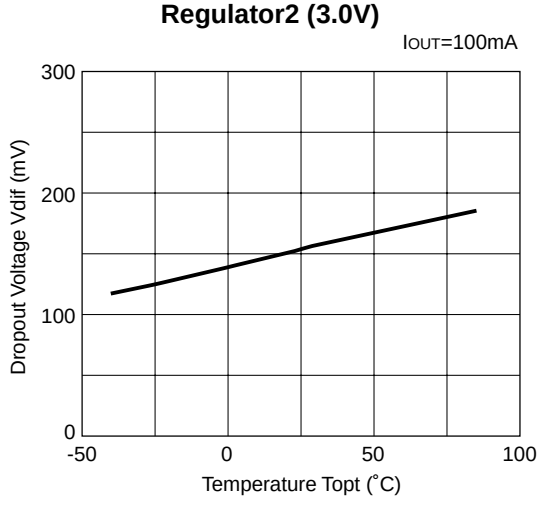


3) Dropout Voltage vs. Temperature

Regulator1 (3.0V)

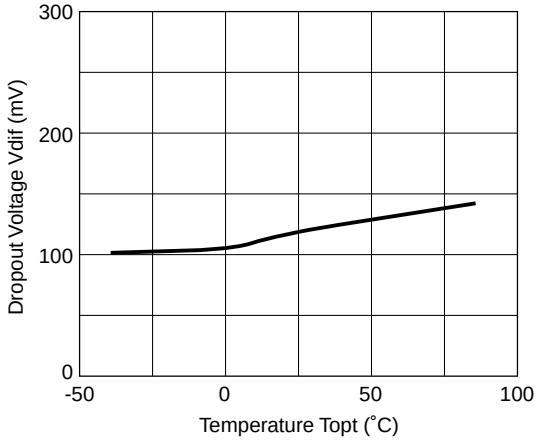


Regulator2 (3.0V)



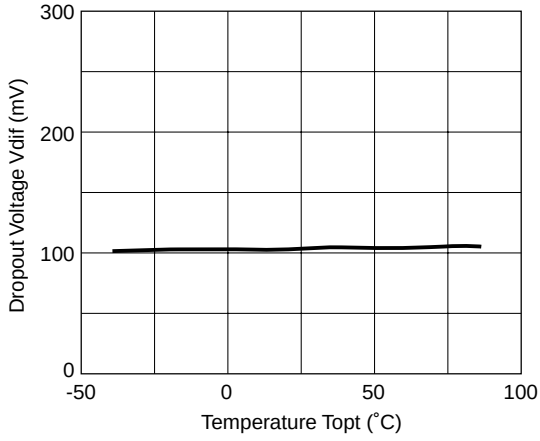
Regulator3 (3.0V)

I_{OUT}=50mA



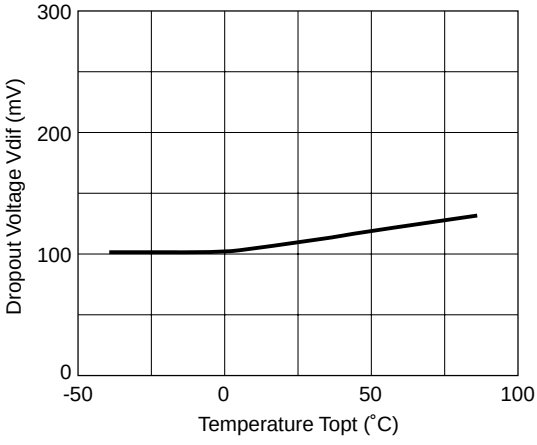
Regulator4 (3.2V)

I_{OUT}=20mA



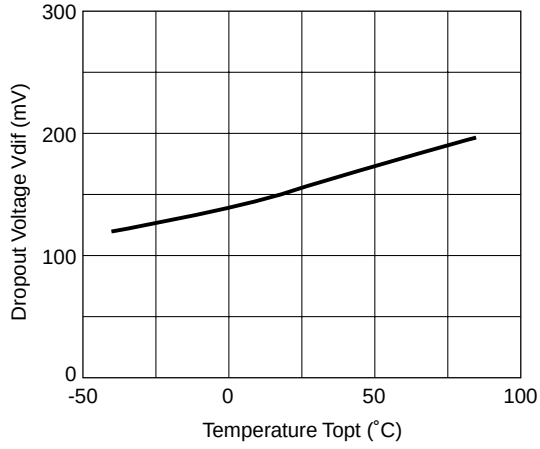
Regulator5 (3.0V)

I_{OUT}=50mA



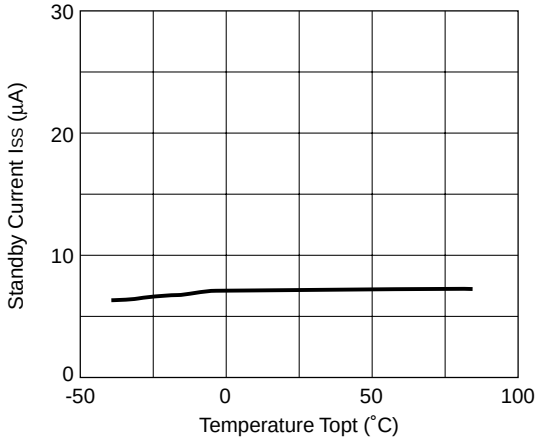
Regulator6 (3.0V)

I_{OUT}=300mA



4) Standby Current vs. Temperature

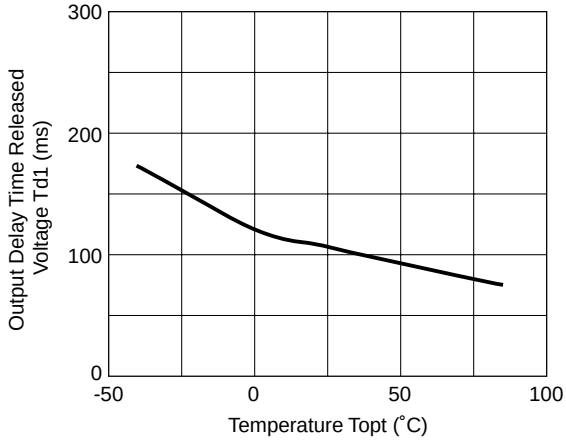
V_{DD}=3.6V



5) VD1 Output Delay Time of Released Voltage vs. Temperature

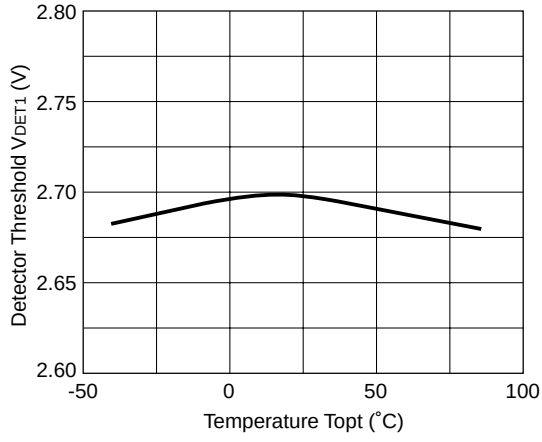
Detector1 (2.7V)

V_{DD}=3.6V C_D=0.15µF

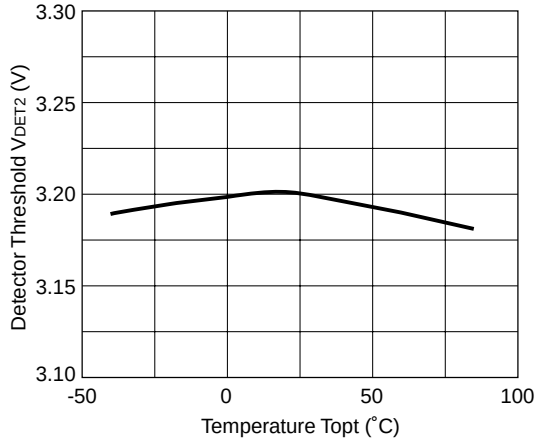


6) Detector Threshold • Released Voltage vs. Temperature

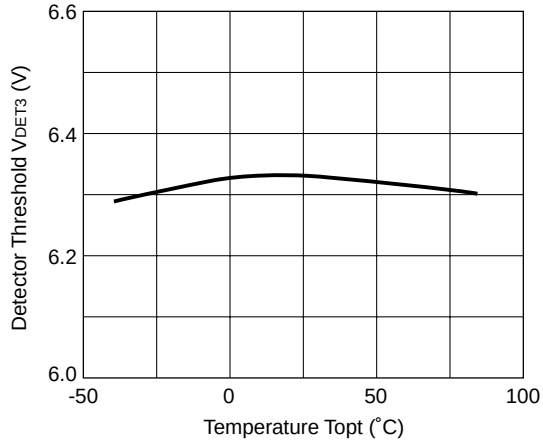
Detector1 (2.7V)



Detector2 (3.2V)

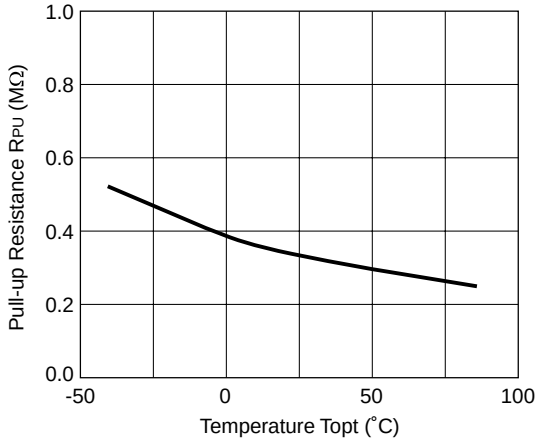


Detector3 (6.3V)

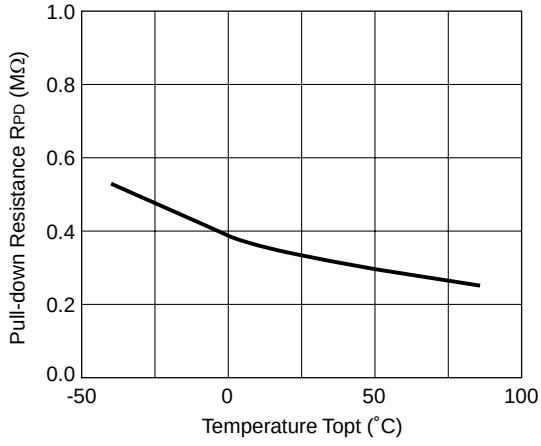


7) Digital Input / Output Resistance value vs. Temperature

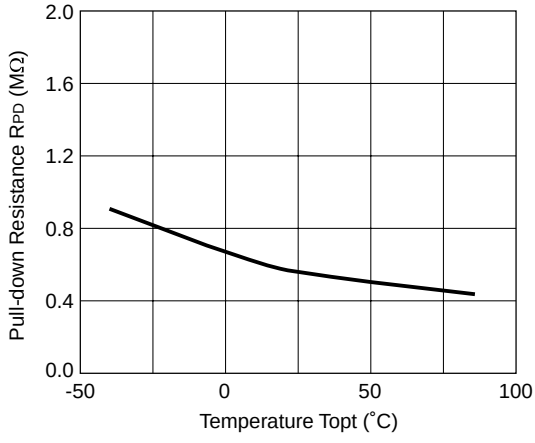
Pull-up Resistance R_{PU1}



Pull-down Resistance R_{PD1}



Pull-down Resistance R_{PD2}



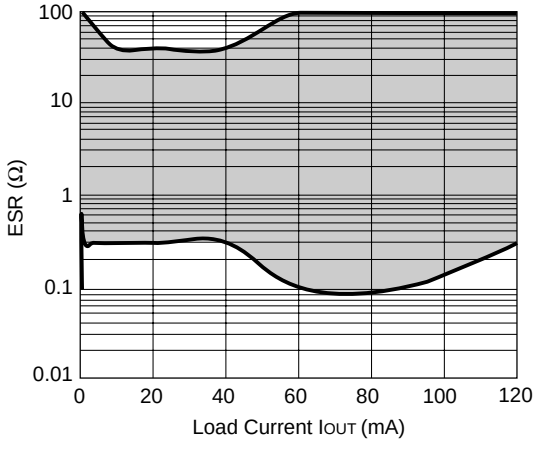
8) Load Current, Capacitance, ESR Noise Characteristics

VR1 Noise Frequency Band 100Hz~1MHz

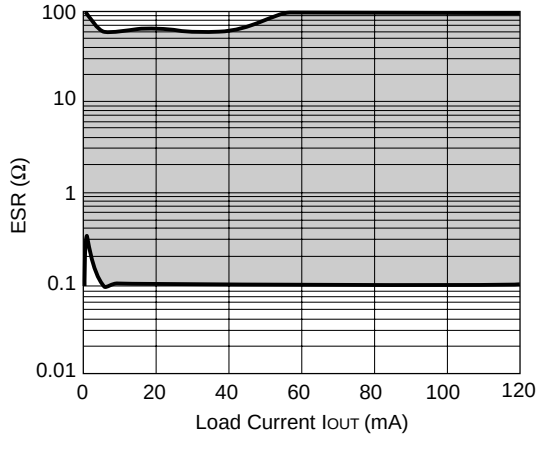
Topt=25°C

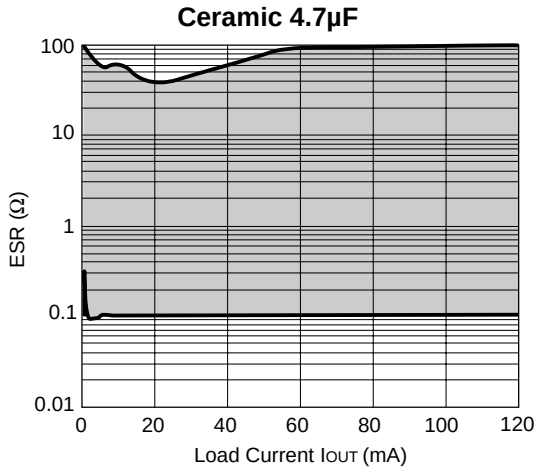
Hatched area shows the combination of ESR and Load current of which noise level is equal or less than 40μV.

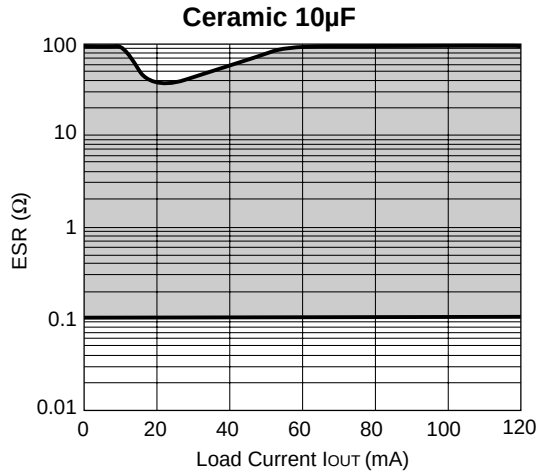
Ceramic 1µF



Ceramic 2.2µF







VR6 Noise Frequency Band 100Hz~1MHz Topt=25°C Hatched area shows the combination of ESR and Load current of which noise level is equal or less than 40μV.