

WIDE BAND VIDEO SWITCH WITH I²C BUS

■ GENERAL DESCRIPTION

The **NJW1320** is a Wide Band Video Switch with I²C BUS. The **NJW1320** includes switch of 4-input 3-output and 6dB amplifier. It is suitable for Y, Pb, and Pr signal because frequency range is 50MHz. The **NJW1320** includes external logic control terminals and external logic discernment terminals. The **NJW1320** is suitable for PTV, DTV, PDP and other high quality AV systems.

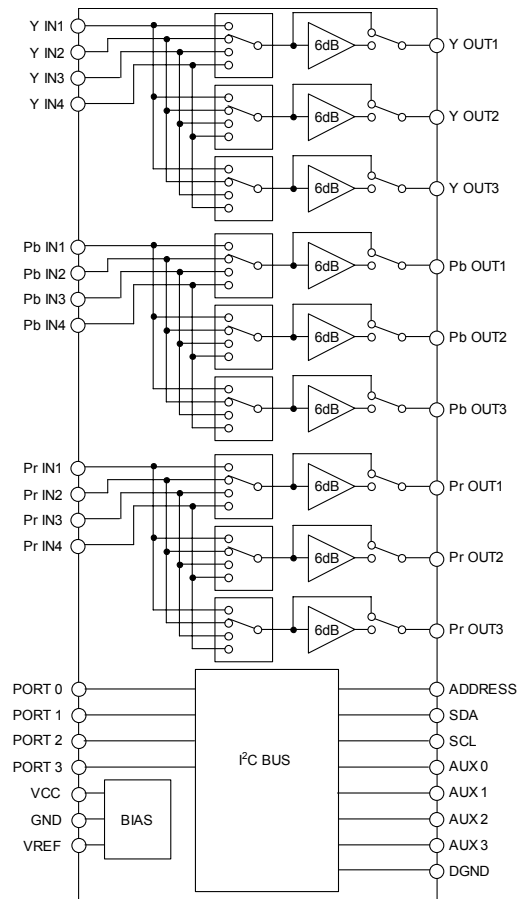


NJW1320FP1

■ FEATURES

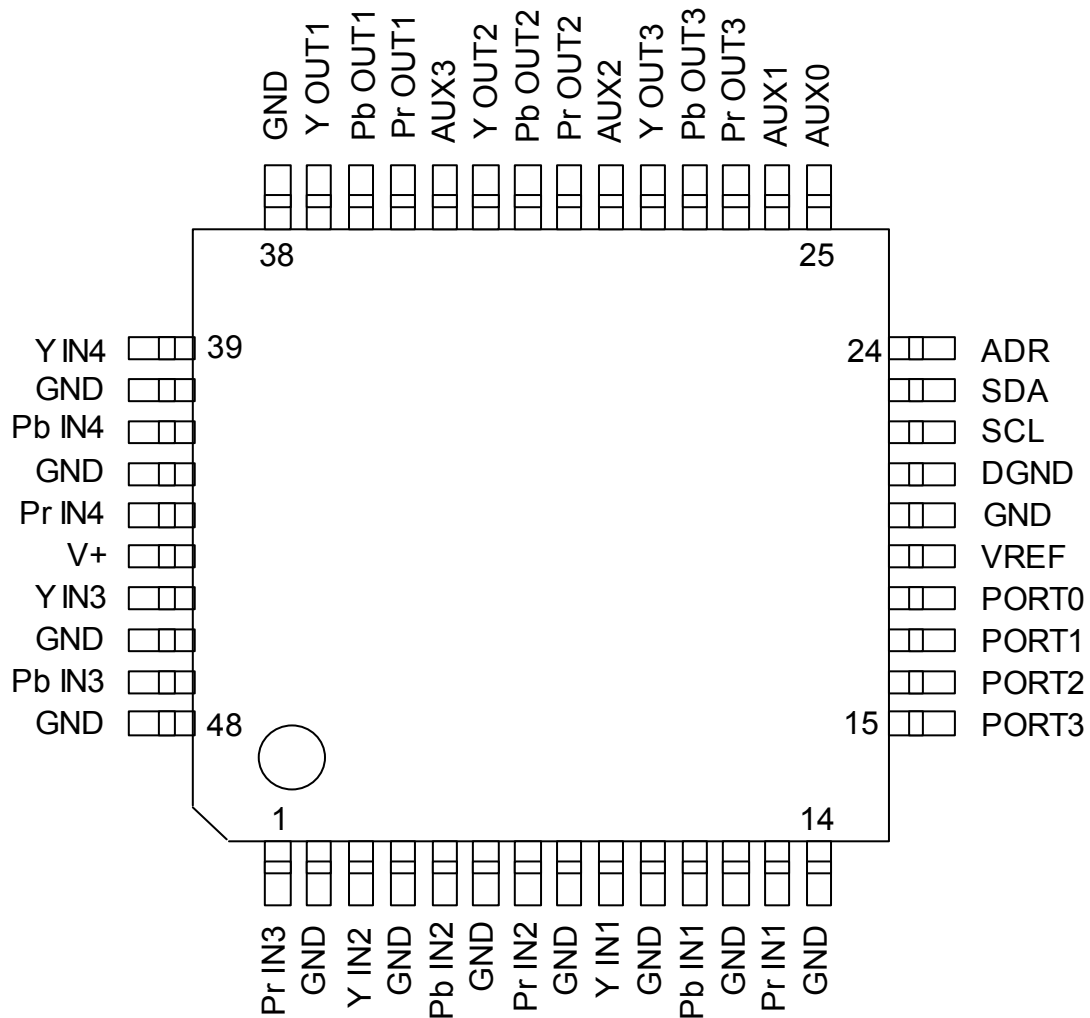
- Operating Voltage 9.0V
- 4-input 3-output 3-Circuits (Y, Pb, and Pr signal)
- Wide frequency range 0dB at 50MHz typ.
- Internal 6dB amplifier (Selectable Bypass or 6dB)
- External logic discernment terminal
- External logic control terminal
- Selectable slave address
- Power Save Circuit
- I²C BUS control
- Bi-CMOS Technology
- Package Outline QFP48

■ BLOCK DIAGRAM



NJW1320

■PIN CONFIGURATION



- | | | | |
|------------|-----------|-------------|------------|
| 1. Pr IN3 | 15. PORT3 | 25. AUX0 | 39. Y IN4 |
| 2. GND | 16. PORT2 | 26. AUX1 | 40. GND |
| 3. Y IN2 | 17. PORT1 | 27. Pr OUT3 | 41. Pb IN4 |
| 4. GND | 18. PORT0 | 28. Pb OUT3 | 42. GND |
| 5. Pb IN2 | 19. VREF | 29. Y OUT3 | 43. Pr IN4 |
| 6. GND | 20. GND | 30. AUX2 | 44. V+ |
| 7. Pr IN2 | 21. DGND | 31. Pr OUT2 | 45. Y IN3 |
| 8. GND | 22. SCL | 32. Pb OUT2 | 46. GND |
| 9. Y IN1 | 23. SDA | 33. Y OUT2 | 47. Pb IN3 |
| 10. GND | 24. ADR | 34. AUX3 | 48. GND |
| 11. Pb IN1 | | 35. Pr OUT1 | |
| 12. GND | | 36. Pb OUT1 | |
| 13. Pr IN1 | | 37. Y OUT1 | |
| 14. GND | | 38. GND | |

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	12.0	V
Power Dissipation	P _D	1875(note)	mW
Operating Temperature Range	Topr	-25 to +75	°C
Storage Temperature Range	Tstg	-40 to +150	°C

(Note) At on a board of EIA/JEDEC specification. (76.2 × 114.3 × 1.6mm Two layers, FR-4)

■ ELECTRICAL CHARACTERISTICS (V⁺=9.0V, R_L=10KΩ, Ta=25°C)

●VIDEO

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		8.0	9.0	10.0	V
Operating Current	I _{cc}	No signal	-	70	100	mA
Maximum Output Voltage	V _{om}	f=100kHz, THD=1%	2.0	2.5	-	Vp-p
Voltage Gain 1	Gv1	Vin=100kHz, 1.0Vp-p Sin signal 6dB Mode	6.0	6.4	6.8	dB
Voltage Gain 2	Gv2	Vin=100kHz, 1.0Vp-p Sin signal Bypass Mode	-0.5	0.0	0.5	dB
Frequency Characteristic 1	Gf1	Vin=50MHz / 100kHz, 1.0Vp-p Sin signal 6dB Mode	-	0	-	dB
Frequency Characteristic 2	Gf2	Vin=50MHz / 100kHz, 1.0Vp-p Sin signal Bypass Mode	-	0	-	dB
Cross talk 1	CTB1	Vin=4.43MHz, 1.0Vp-p Sin signal	-	-60	-50	dB
Cross talk 2	CTB2	Vin=30MHz, 1.0Vp-p Sin signal	-	-40	-	dB
Differential Gain	DG	Vin=1.0Vp-p 10step Video signal	-	0.3	-	%
Differential Phase	DP	Vin=1.0Vp-p 10step Video signal	-	0.3	-	deg
S/N	SNv	Vin=1.0Vp-p, 100% White Video Signal	-	65	-	dB

●PORT, AUX

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PORT Input Voltage H	V _{PTH}		3.5	-	5.5	V
PORT Input Voltage M	V _{PTM}		1.4	-	2.4	V
PORY Input Voltage L	V _{PTL}		0	-	0.8	V
AUX Output Voltage H	V _{AUXH}		3.5	-	5.5	V
AUX Output Voltage M	V _{AUXM}		1.4	-	2.4	V
AUX Output Voltage L	V _{AUXL}		0	-	0.8	V
ADR Input Voltage H	V _{ADRH}		3.5	-	5.0	V
ADR Input Voltage L	V _{ADRL}		0	-	1.0	V

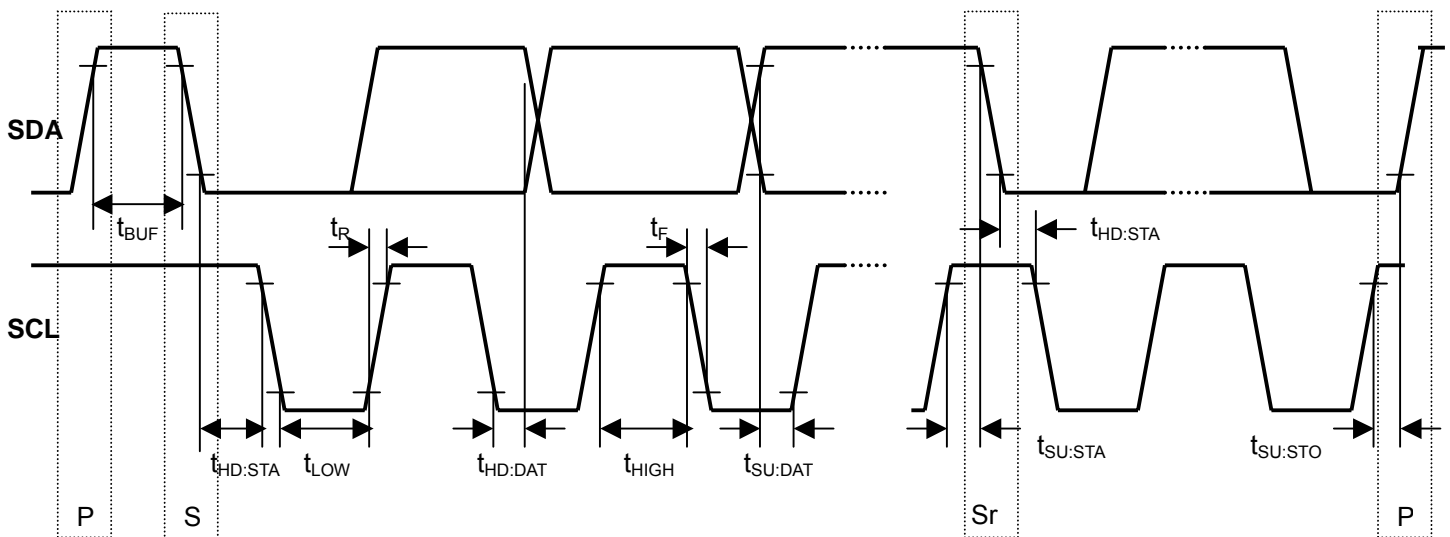
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■ I²C BUS BLOCK CHARACTERISTICS (SDA,SCL)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V _{IH}	3.0	-	5.0	V
Low Level Input Voltage	V _{IL}	0	-	1.5	V
High Level Input Current	I _{IH}	-	-	10	μA
Low Level Input Current	I _{IL}	-	-	10	μA
Low Level Output Voltage (3mA at SDA pin)	V _{OL}	0	-	0.4	V
Maximum Output Current	I _{OL}	-3.0	-	-	mA
Maximum Clock Frequency	f _{SCL}	-	-	100	kHz
Data Change Minimum Waiting Time	t _{BUF}	4.7	-	-	μs
Data Transfer Start Minimum Waiting Time	t _{HD:STA}	4.0	-	-	μs
Low Level Clock Pulse Width	t _{LOW}	4.7	-	-	μs
High Level Clock Pulse Width	t _{HIGH}	4.0	-	-	μs
Minimum Start Preparation Waiting Time	t _{SU:STA}	4.7	-	-	μs
Minimum Data Hold Time	t _{HD:DAT}	5.0	-	-	μs
Minimum Data Preparation Time	t _{SU:DAT}	250	-	-	ns
Rise Time	t _R	-	-	1.0	μs
Fall Time	t _F	-	-	300	ns
Minimum Stop Preparation Waiting Time	t _{SU:STO}	4.7	-	-	μs

I²C BUS Load Condition: Pull up resistance 4kΩ (Connected to +5V)

Load capacitance 200pF (Connected to GND)



■ TERMINAL DESCRIPTION

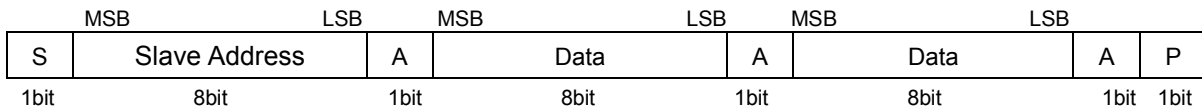
No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
9 11 13 3 5 7 45 47 1 39 41 43	Y1 IN Pb1 IN Pr1 IN Y2 IN Pb2 IN Pr2 IN Y3 IN Pb3 IN Pb4 IN Pr3 IN Y4 IN Pb4 IN Pr4 IN	Component signal input terminal		4.4V
18 17 16 15	PORT0 PORT1 PORT2 PORT3	Logic input terminal		-
19	VREF	Reference voltage terminal		5.0V
2 4 6 8 10 12 14 20 38 40 42 46 48	GND	Ground terminal		-
21	DGND	Ground terminal		-

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No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
22 23	SCL SDA	I ² C clock terminal I ² C data terminal		-
24	ADR	Slave address setting terminal		-
25 26 27 28	AUX0 AUX1 AUX2 AUX3	Auxiliary 3 values voltage output terminal		0V 1.9V 5.0V
37 34 31 36 33 30 35 32 29	Y1 OUT Y2 OUT Y3 OUT Pb1 OUT Pb2 OUT Pb3 OUT Pr1 OUT Pr2 OUT Pr3 OUT	Component signal output terminal		3.0V
44	V+	Supply voltage terminal		-

■ DEFINITION OF I²C REGISTER

◆ I²C BUS FORMAT



S: Starting Term

A: Acknowledge Bit

P: Ending Term

◆ SLAVE ADDRESS

R/W: Set the Write Mode or Read Mode.

ADR : Set the Slave Address by "ADR" terminal.

Slave Address								Hex
MSB				LSB				
1	0	0	0	0	0	ADR	R/W	-
◆ R/W = 0 : Write Mode, ADR = 0/1								-
1	0	0	1	0	1	0	0	94(h)
1	0	0	1	0	1	1	0	96(h)
◆ R/W = 1 : Read Mode, ADR = 0/1								-
1	0	0	1	0	1	0	1	95(h)
1	0	0	1	0	1	1	1	97(h)

◆ CONTROL REGISTER TABLE

< Write Mode >

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data1	PS2	PS3	OUT1			OUT2		
Data2	OUT3				*			
Data3	AUX0		AUX1		AUX2		AUX3	

* : Don't Care

< Read Mode >

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	PORT0		PORT1		PORT2		PORT3	

◆ CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data1	0	0	0	0	0	0	0	0
Data2	0	0	0	0	0	0	0	0
Data3	0	0	0	0	0	0	0	0

■ INSTRUCTION CODE

◆ POWER SAVE, OUTPUT SETTING

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data1	PS2	PS3	OUT1			OUT2		
Data2	OUT3			*				

* : Don't Care

● PS2, PS3: Power Save Setting

Power Save			D7	D6
OUT1 ON	OUT2 ON	OUT3 ON	0	0
OUT1 ON	OUT2 ON	OUT3 OFF	0	1
OUT1 ON	OUT2 OFF	OUT3 ON	1	0
OUT1 ON	OUT2 OFF	OUT3 OFF	1	1

ON: Power Save OFF, OFF: Power Save ON

● OUT1: Output 1 Setting

Output 1			D5	D4	Gain	D3
YIN1	PbIN1	PrIN1	0	0	6dB	0
YIN2	PbIN2	PrIN2	0	1	0dB	1
YIN3	PbIN3	PrIN3	1	0		
YIN4	PbIN4	PrIN4	1	1		

● OUT2: Output 2 Setting

Output 2			D2	D1	Gain	D0
YIN1	PbIN1	PrIN1	0	0	6dB	0
YIN2	PbIN2	PrIN2	0	1	0dB	1
YIN3	PbIN3	PrIN3	1	0		
YIN4	PbIN4	PrIN4	1	1		

● OUT3: Output 3 Setting

Output 3			D7	D6	Gain	D5
YIN1	PbIN1	PrIN1	0	0	6dB	0
YIN2	PbIN2	PrIN2	0	1	0dB	1
YIN3	PbIN3	PrIN3	1	0		
YIN4	PbIN4	PrIN4	1	1		

◆AUX: AUXILIARY SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data3	AUX0		AUX1		AUX2		AUX3	

AUX0	D7	D6
L	0	0
M	0	1
H	1	1

AUX1	D5	D4
L	0	0
M	0	1
H	1	1

AUX2	D3	D2
L	0	0
M	0	1
H	1	1

AUX3	D1	D0
L	0	0
M	0	1
H	1	1

◆PORT: PORT SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	PORT0		PORT1		PORT2		PORT3	

PORT0	D7	D6
OPEN	0	0
L	0	0
M	0	1
H	1	1

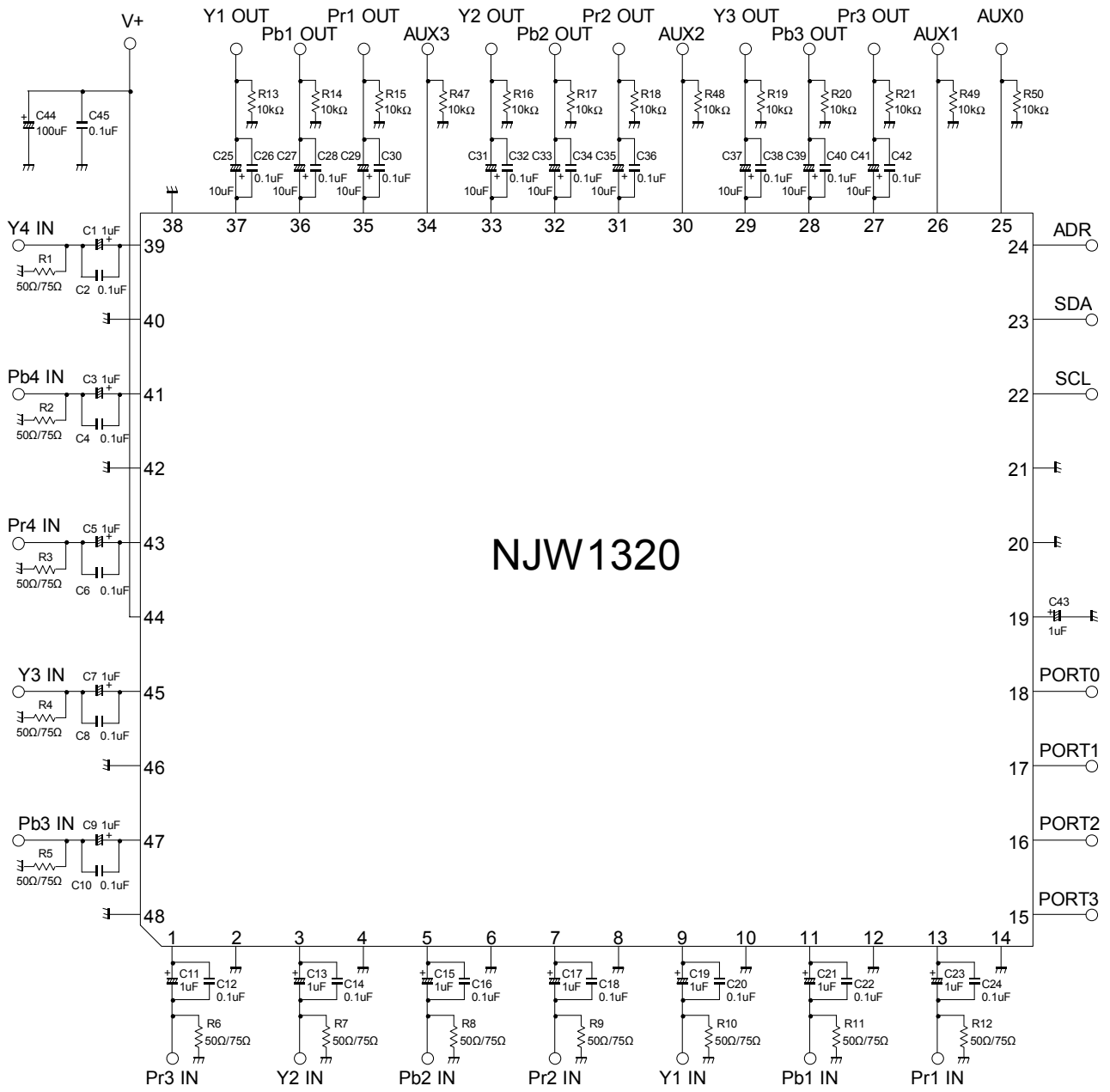
PORT0	D7	D6
OPEN	0	0
L	0	0
M	0	1
H	1	1

PORT0	D7	D6
OPEN	0	0
L	0	0
M	0	1
H	1	1

PORT3	D1	D0
OPEN	0	0
L	0	0
M	0	1
H	1	1

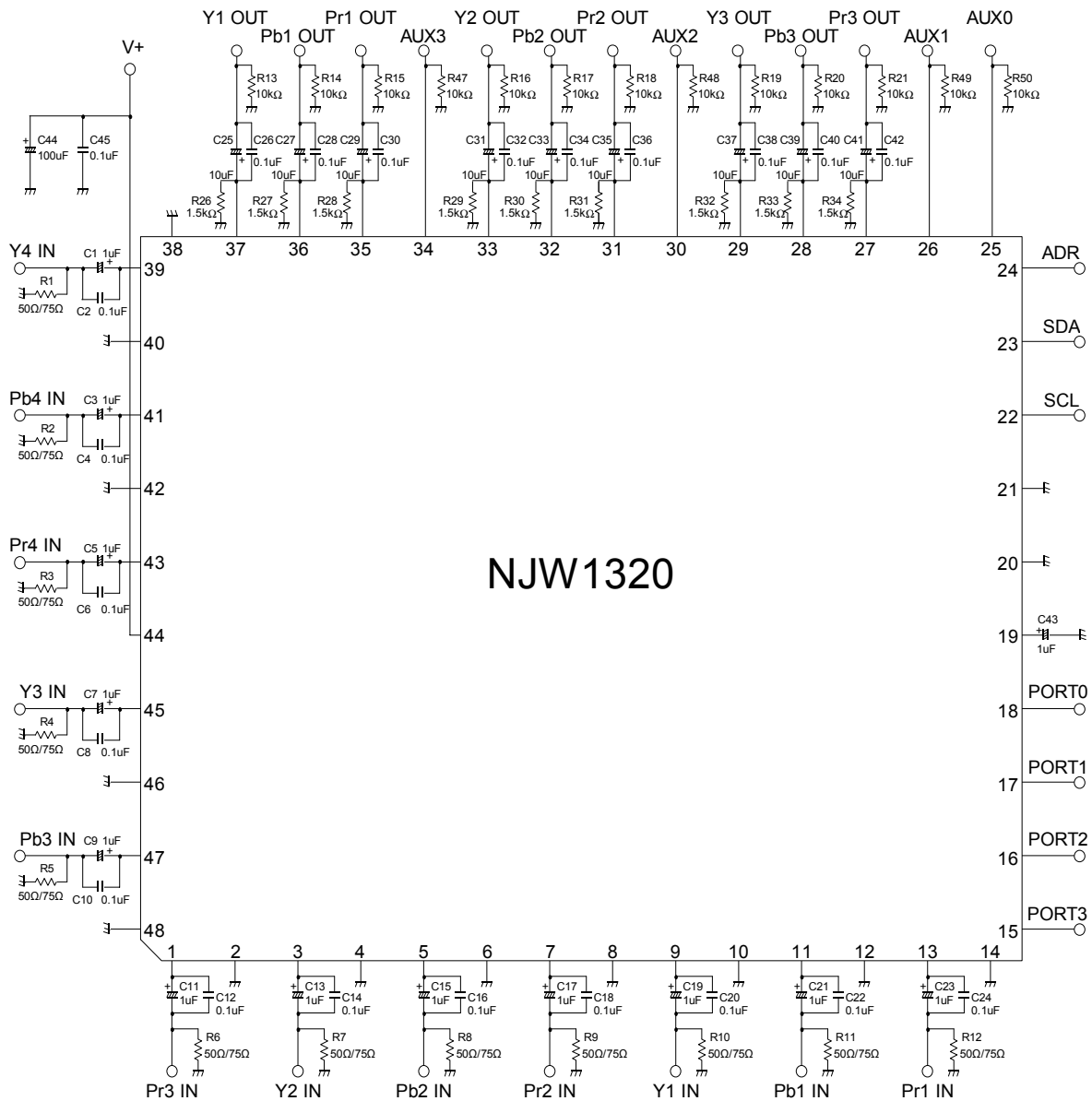
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TEST CIRCUIT



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■APPLICATION CIRCUIT



Addition of R26-R34 improves the through rate in high frequency. Resistance turns into a reference value.

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■NOTE

Please ground all of 2, 4, 6, 8, 10, 12, 14, 20, 21, 38, 40, 42, 46, and 48pin.

When the power supply voltage is not impressing, please do not impress voltage to the ADL terminal.

■NOTE

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