# MC74VHC1G01

# Single 2-Input NAND Gate with Open Drain Output

The MC74VHC1G01 is an advanced high speed CMOS 2−input NAND gate with an open drain output fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including an open drain output which provides the ability to set output switching level. This allows the MC74VHC1G01 to be used to interface 5.0 V circuits to circuits of any voltage between $V_{CC}$ and 7.0 V using an external resistor and power supply.

The MC74VHC1G01 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

### Features

- High Speed: $t_{PD}$ = 3.7 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Internal Power Dissipation: $I_{CC}$ = 1 μA (Max) at $T_A$ = 25°C
- Power Down Protection Provided on Inputs
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 62
- Pb−Free Packages are Available

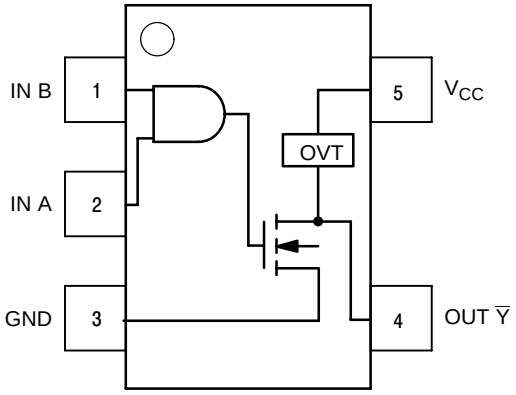



**Figure 1. Pinout** (Top View)

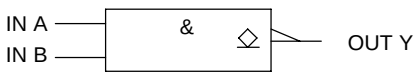


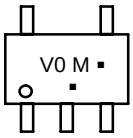

**Figure 2. Logic Symbol**

**ON Semiconductor®**

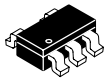
**http://onsemi.com**

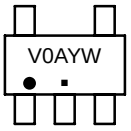
**MARKING DIAGRAMS**

**SC−88A / SOT−353 / SC−70**
**DF SUFFIX**
**CASE 419A**




**TSOP−5 / SOT−23 / SC−59**
**DT SUFFIX**
**CASE 483**






M = Date Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

| PIN ASSIGNMENT | |
|---|---|
| 1 | IN B |
| 2 | IN A |
| 3 | GND |
| 4 | OUT $\overline{Y}$ |
| 5 | $V_{CC}$ |

**FUNCTION TABLE**

| Inputs | | Output |
|---|---|---|
| **A** | **B** | **$\overline{Y}$** |
| L | L | Z |
| L | H | Z |
| H | L | Z |
| H | H | L |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

**MAXIMUM RATINGS**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | DC Input Diode Current | | −20 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND; $V_{OUT}$ > $V_{CC}$ | ±20 | mA |
| $I_{OUT}$ | DC Output Sink Current, per Pin | | 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pin | | ±25 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance | SC70−5/SC−88A (Note 1)<br>TSOP−5 | 350<br>230 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 85°C | SC70−5/SC−88A<br>TSOP−5 | 150<br>200 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4) | >2000<br>>200<br>N/A | V |
| $I_{LATCHUP}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 5) | ±500 | mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Characteristics | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | 2.0 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage | | 0.0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage | | 0.0 | 7.0 | V |
| $T_A$ | Operating Temperature Range | | −55 | +125 | °C |
| $t_r$ , $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 3.3 V ± 0.3 V<br>$V_{CC}$ = 5.0 V ± 0.5 V | 0<br>0 | 100<br>20 | ns/V |

**DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES**

| Junction Temperature °C | Time, Hours | Time, Years |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

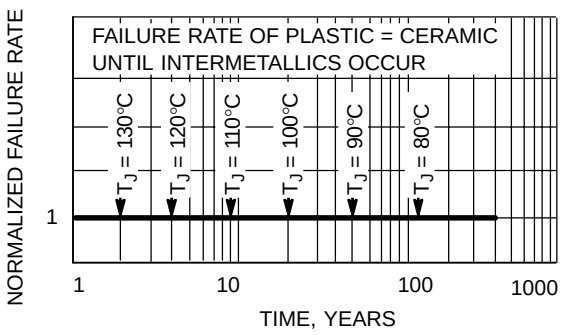



**Figure 3. Failure Rate vs. Time Junction Temperature**

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | $T_A \leq$ 85°C Min | $T_A \leq$ 85°C Max | −55°C ≤ $T_A \leq$ 125°C Min | −55°C ≤ $T_A \leq$ 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High−Level Input Voltage | | 2.0<br>3.0<br>4.5<br>5.5 | 1.5<br>2.1<br>3.15<br>3.85 | | | 1.5<br>2.1<br>3.15<br>3.85 | | 1.5<br>2.1<br>3.15<br>3.85 | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 2.0<br>3.0<br>4.5<br>5.5 | | | 0.5<br>0.9<br>1.35<br>1.65 | | 0.5<br>0.9<br>1.35<br>1.65 | | 0.5<br>0.9<br>1.35<br>1.65 | V |
| $V_{OL}$ | Maximum Low−Level Output Voltage $V_{IN} = V_{IH}$ or $V_{IL}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 50 μA | 2.0<br>3.0<br>4.5 | | 0.0<br>0.0<br>0.0 | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA | <br>3.0<br>4.5 | | | <br>0.36<br>0.36 | | <br>0.44<br>0.44 | | <br>0.52<br>0.52 | |
| $I_{LKG}$ | Z−State Output Leakage Current | $V_{IN} = V_{IL}$<br>$V_{OUT} = V_{CC}$ or GND | 5.5 | | | ±5 | | ±10 | | ±10 | μA |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 1.0 | | 20 | | 40 | μA |
| $I_{OFF}$ | Power Off−Output Leakage Current | $V_{OUT}$ = 5.5 V<br>$V_{IN}$ = 5.5 V | 0 | | | 0.25 | | 2.5 | | 5 | μA |

## AC ELECTRICAL CHARACTERISTICS Input $t_r = t_f$ = 3.0 ns

| Symbol | Parameter | Test Conditions | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | $T_A \leq$ 85°C Min | $T_A \leq$ 85°C Max | −55 ≤ $T_A \leq$ 125°C Min | −55 ≤ $T_A \leq$ 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PZL}$ | Maximum Output Enable Time, Input A or B to Y | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF<br>$R_L = R_I$ = 500 Ω $C_L$ = 50 pF | | 5.5<br>8.0 | 7.9<br>11.4 | | 9.5<br>13.0 | | 11.0<br>15.5 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF<br>$R_L = R_I$ = 500 Ω $C_L$ = 50 pF | | 3.7<br>5.2 | 5.5<br>7.5 | | 6.5<br>8.5 | | 8.0<br>10.0 | |
| $t_{PLZ}$ | Maximum Output Disable Time | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 50 pF<br>$R_L = R_I$ = 500 Ω | | 8.0 | 11.4 | | 13.0 | | 15.5 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 50 pF<br>$R_L = R_I$ = 500 Ω | | 5.2 | 7.5 | | 8.5 | | 10.0 | |
| $C_{IN}$ | Maximum Input Capacitance | | | 4 | 10 | | 10 | | 10 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 6) | 18 | pF |

6. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

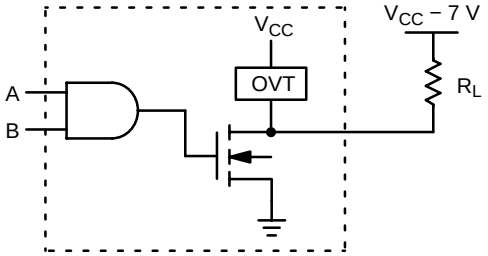



**Figure 4. Output Voltage Mismatch Application**

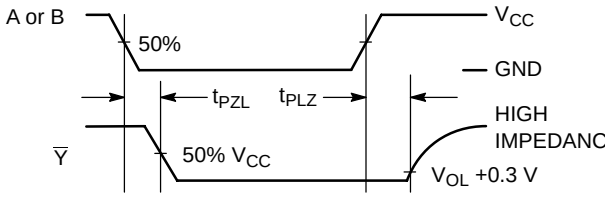
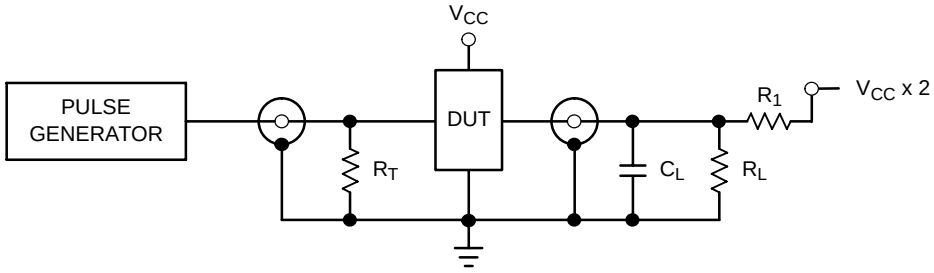
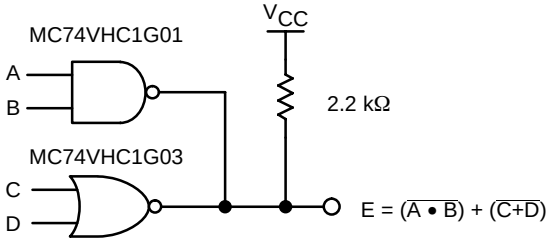


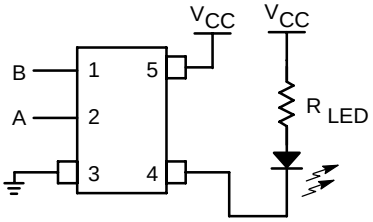

**Figure 5. Switching Waveforms**

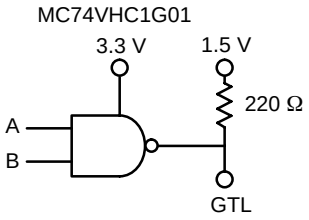



$C_L$ = 50 pF equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500 Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

**Figure 6. Test Circuit**



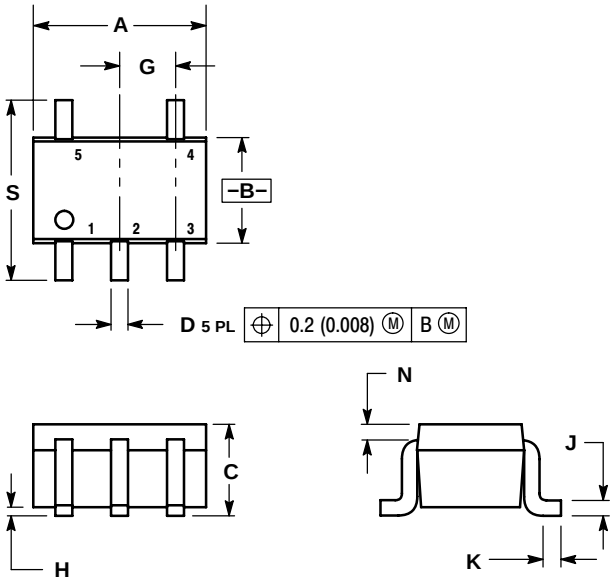

**DEVICE ORDERING INFORMATION**

| Device Order Number | Package Type | Tape and Reel Size† |
|---|---|---|
| MC74VHC1G01DFT1 | SC70−5 / SC−88A / SOT−353 | 178 mm (7”)<br>3000 Unit |
| MC74VHC1G01DFT1G | SC70−5 / SC−88A / SOT−353<br>(Pb−Free) | 178 mm (7”)<br>3000 Unit |
| MC74VHC1G01DFT2 | SC70−5 / SC−88A / SOT−353 | 178 mm (7”)<br>3000 Unit |
| MC74VHC1G01DFT2G | SC70−5 / SC−88A / SOT−353<br>(Pb−Free) | 178 mm (7”)<br>3000 Unit |
| MC74VHC1G01DTT1 | SOT23−5 / TSSOP−5 / SC59−5 | 178 mm (7”)<br>3000 Unit |
| MC74VHC1G01DTT1G | SOT23−5 / TSSOP−5 / SC59−5<br>(Pb−Free) | 178 mm (7”)<br>3000 Unit |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

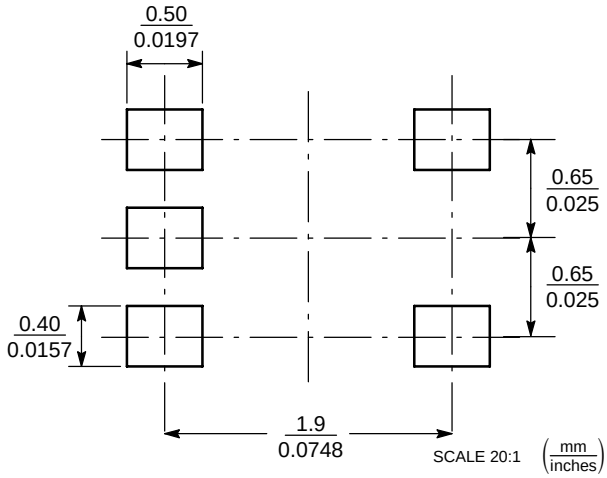
**SC−88A/SOT−353/SC−70**
CASE 419A−02
ISSUE H




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

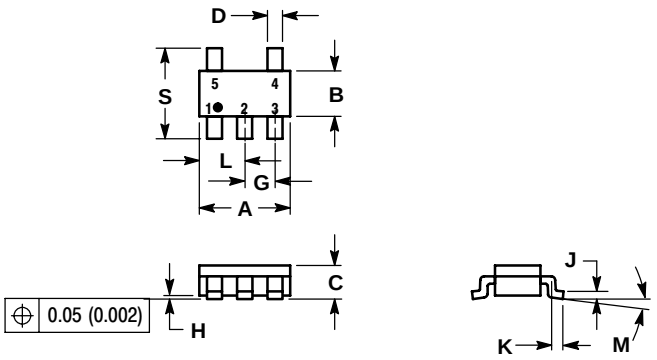
## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

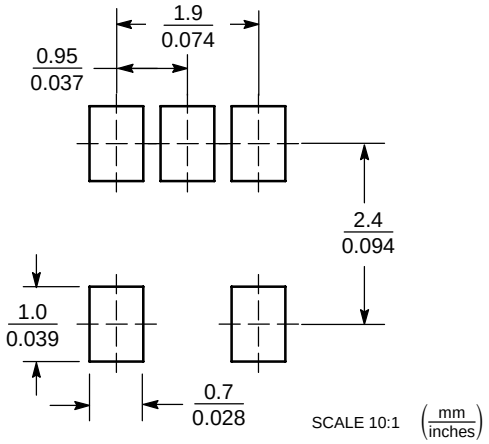
**TSOP−5/SOT−23/SC−59**
CASE 483−02
ISSUE D




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.1142 | 0.1220 |
| B | 1.30 | 1.70 | 0.0512 | 0.0669 |
| C | 0.90 | 1.10 | 0.0354 | 0.0433 |
| D | 0.25 | 0.50 | 0.0098 | 0.0197 |
| G | 0.85 | 1.05 | 0.0335 | 0.0413 |
| H | 0.013 | 0.100 | 0.0005 | 0.0040 |
| J | 0.10 | 0.26 | 0.0040 | 0.0102 |
| K | 0.20 | 0.60 | 0.0079 | 0.0236 |
| L | 1.25 | 1.55 | 0.0493 | 0.0610 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 2.50 | 3.00 | 0.0985 | 0.1181 |

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
**Phone**: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
**Fax**: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada

**Japan**: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
**Phone**: 81−3−5773−3850

**ON Semiconductor Website**: http://onsemi.com

**Order Literature**: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.