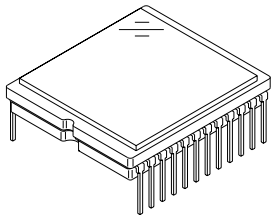
SONY

ICX282AK

Diagonal 11mm (Type 2/3) Frame Readout CCD Image Sensor with Square Pixel for Color Cameras

24 pin DIP (Plastic)



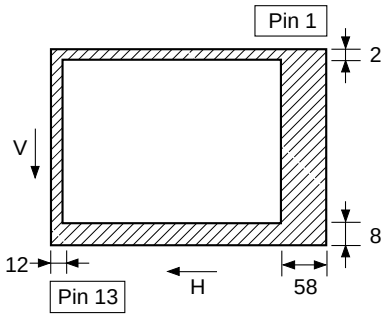
Description

The ICX282AK is a diagonal 11mm (Type 2/3) interline CCD solid-state image sensor with a square pixel array and 5.07M effective pixels. Frame readout allows all pixels' signals to be output independently within approximately 1/3.75 second. In addition, output is possible using various addition and pulse elimination methods. This chip features an electronic shutter with variable charge-storage time. Adoption of a design specially suited for frame readout ensures a saturation signal level equivalent to that when using field readout. High resolution and high color reproductively are achieved through the use of Ye, Cy, Mg and G complementary color mosaic filters as the color filters. Further, high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

This chip is suitable for applications such as electronic still cameras, PC input cameras, etc.

Features

- High horizontal and vertical resolution
- Supports 10 types of readout modes
  Frame readout mode, 2× speed mode (1), 2× speed mode (2), 8× speed mode, center scan mode (1), center scan mode (2), center scan mode (3), center scan mode (4), AF mode (1), AF mode (2)
- Square pixel
- Horizontal drive frequency: 22.5MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- Ye, Cy, Mg and G complementary color mosaic filters on chip
- High sensitivity, low dark current, excellent anti-blooming characteristics
- Continuous variable-speed shutter
- Horizontal register, reset gate: 3.3V drive
- 24-pin high-precision plastic package



Optical black position
(Top View)

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 11mm (Type 2/3)
- Total number of pixels: 2658 (H) × 1970 (V) approx. 5.24M pixels
- Number of effective pixels: 2588 (H) × 1960 (V) approx. 5.07M pixels
- Number of active pixels: 2580 (H) × 1944 (V) approx. 5.02M pixels
- Number of recommended recording pixels:
  2560 (H) × 1920 (V) approx. 4.92M pixels
- Chip size: 9.74mm (H) × 7.96mm (V)
- Unit cell size: 3.4µm (H) × 3.4µm (V)
- Optical black: Horizontal (H) direction: Front 12 pixels, rear 58 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28
  Vertical 1 (even fields only)
- Substrate material: Silicon

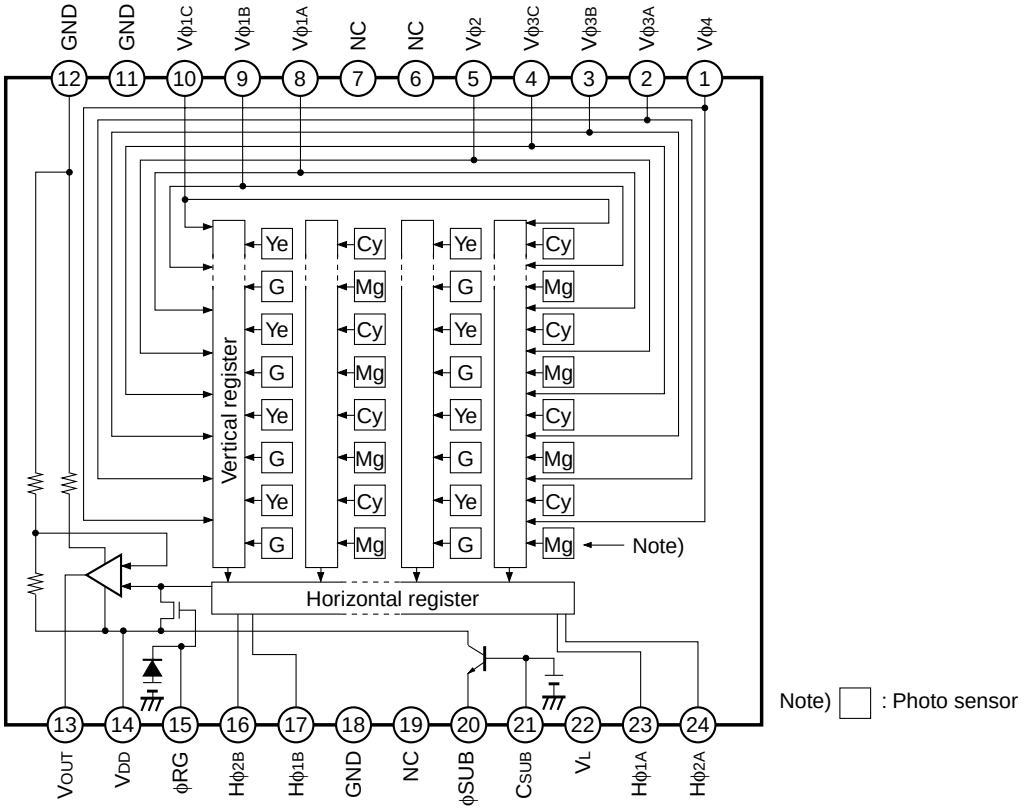
Super **HAD CCD** TM

* Super HAD CCD is a registered trademark of Sony Corporation. Super HAD CCD is a CCD that drastically improves sensitivity by introducing newly developed semiconductor technology by Sony Corporation into Sony's high-performance HAD (Hole-Accumulation Diode) sensor.

E01626A31-PS

Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	13	VOUT	Signal output
2	Vφ3A	Vertical register transfer clock	14	VDD	Supply voltage
3	Vφ3B	Vertical register transfer clock	15	φRG	Reset gate clock
4	Vφ3C	Vertical register transfer clock	16	Hφ2B	Horizontal register transfer clock
5	Vφ2	Vertical register transfer clock	17	Hφ1B	Horizontal register transfer clock
6	NC		18	GND	GND
7	NC		19	NC	
8	Vφ1A	Vertical register transfer clock	20	φSUB	Substrate clock
9	Vφ1B	Vertical register transfer clock	21	CSUB	Substrate bias*1
10	Vφ1C	Vertical register transfer clock	22	VL	Protective transistor bias
11	GND	GND	23	Hφ1A	Horizontal register transfer clock
12	GND	GND	24	Hφ2A	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +12	V	
	Vφ1α, Vφ3α – φSUB (α = A to C)	–50 to +15	V	
	Vφ2, Vφ4, V_L – φSUB	–50 to +0.3	V	
	Hφ1β, Hφ2β, GND – φSUB (β = A, B)	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against GND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +22	V	
	Vφ1α, Vφ2, Vφ3α, Vφ4 – GND (α = A to C)	–10 to +18	V	
	Hφ1β, Hφ2β – GND (β = A, B)	–10 to +6.5	V	
Against V_L	Vφ1α, Vφ3α – V_L (α = A to C)	–0.3 to +28	V	
	Vφ2, Vφ4, Hφ1β, Hφ2β, GND – V_L (β = A, B)	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	Hφ1β – Hφ2β (β = A, B)	–6.5 to +6.5	V	
	Hφ1β, Hφ2β – Vφ4 (β = A, B)	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	φSUB	*2				
Reset gate clock	φRG	*2				

*1 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}	4.0	7.0	10.0	mA	

Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V\phi_V$	6.8	7.5	8.05	V	2	$V\phi_V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.6	V	2	High-level coupling
	V_{VHL}			0.9	V	2	High-level coupling
	V_{VLH}			0.9	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	3.0	3.3	3.6	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	0.5	1.65		V	3	Cross-point voltage
Reset gate clock voltage	$V\phi_{RG}$	3.0	3.3	3.6	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	21.5	22.5	23.5	V	5	

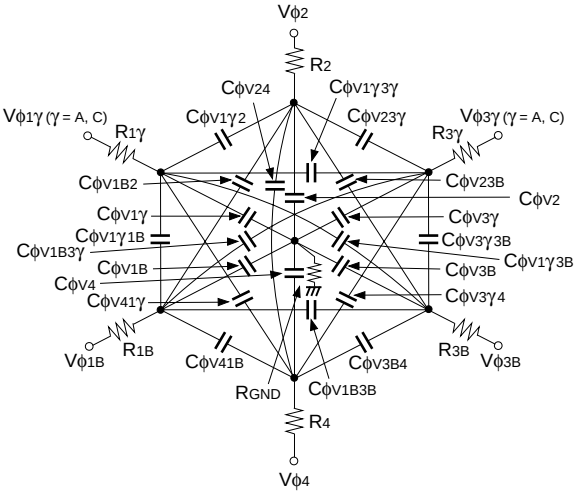
Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1\gamma$, $C\phi V3\gamma$		1800		pF	
	$C\phi V1B$, $C\phi V3B$		6800		pF	
	$C\phi V2$, $C\phi V4$		5600		pF	
Capacitance between vertical transfer clocks	$C\phi V1\gamma 2$, $C\phi V3\gamma 4$		560		pF	
	$C\phi V1B2$, $C\phi V3B4$		680		pF	
	$C\phi V23\gamma$, $C\phi V41\gamma$		180		pF	
	$C\phi V23B$, $C\phi V41B$		270		pF	
	$C\phi V1\gamma 3\gamma$		56		pF	
	$C\phi V1B3B$		330		pF	
	$C\phi V1\gamma 3B$, $C\phi V1B3\gamma$		91		pF	
	$C\phi V24$		120		pF	
	$C\phi V1\gamma 1B$, $C\phi V3\gamma 3B$		100		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1$		82		pF	
	$C\phi H2$		62		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		110		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		5		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		1500		pF	
Vertical transfer clock series resistor	$R1\gamma$, $R3\gamma$		62		Ω	
	$R1B$, $R2$, $R3B$, $R4$		43		Ω	
Vertical transfer clock ground resistor	R_{GND}		16		Ω	
Horizontal transfer clock series resistor	$R\phi H$		7.5		Ω	

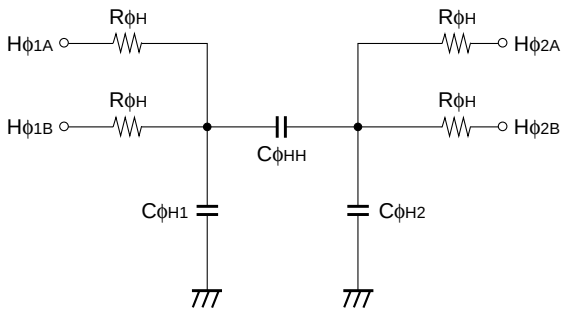
Note 1) γ = A, C for each vertical transfer clock capacitance.

Note 2) The relationships of V1A = V1C and V3A = V3C are established for each vertical transfer clock capacitance.

Note 3) $C\phi V1A1C$ and $C\phi V3A3C$ are sufficiently small relative to other capacitance between vertical transfer clocks, and are also below the measurement limit, so these are omitted from the equivalent circuit diagrams and the above table.



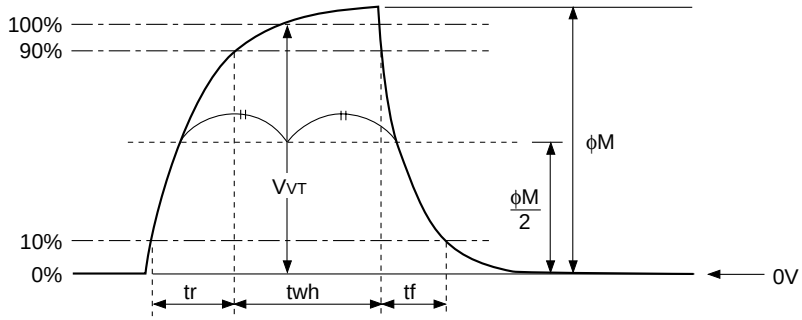
Vertical transfer clock equivalent circuit



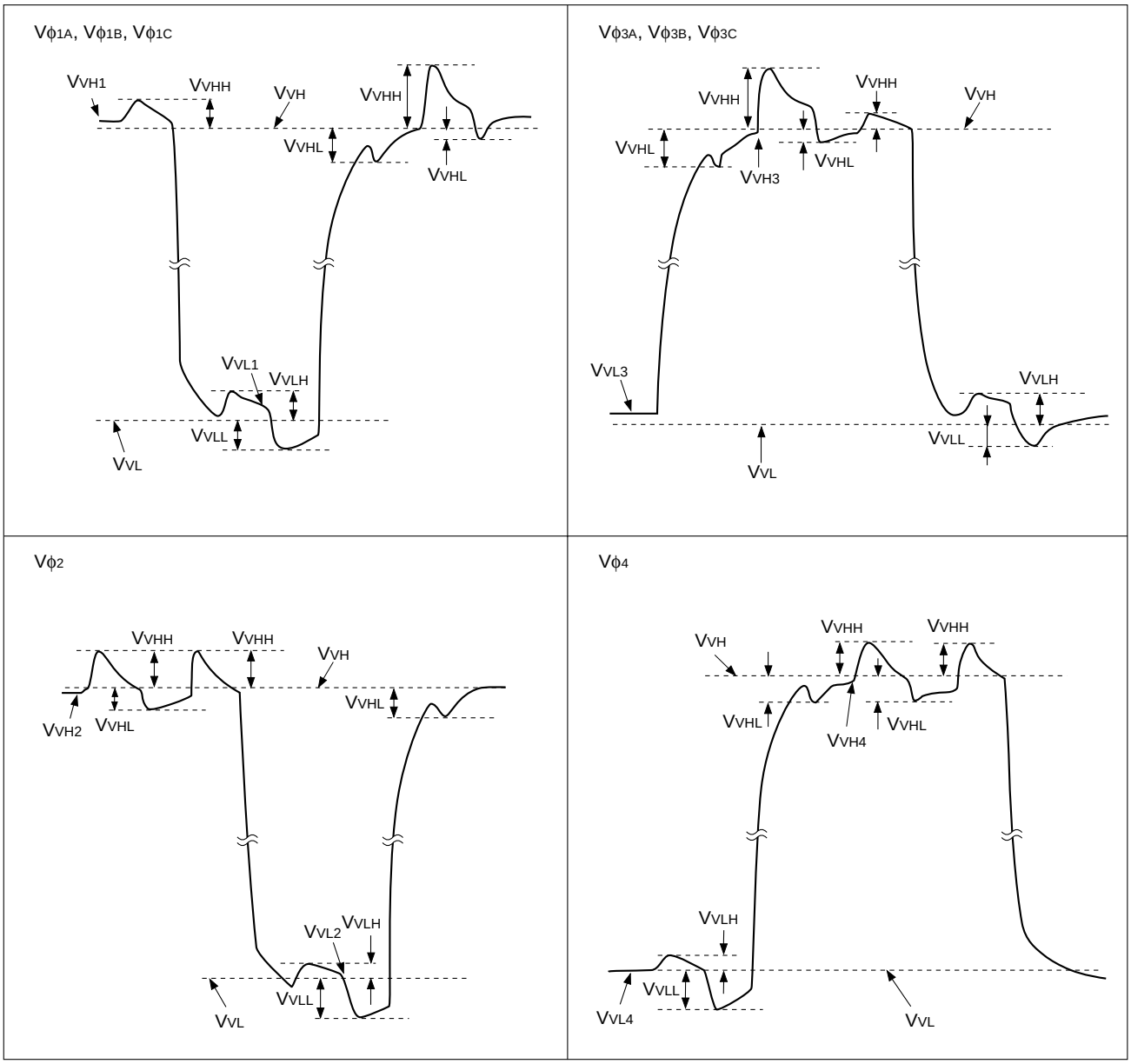
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform

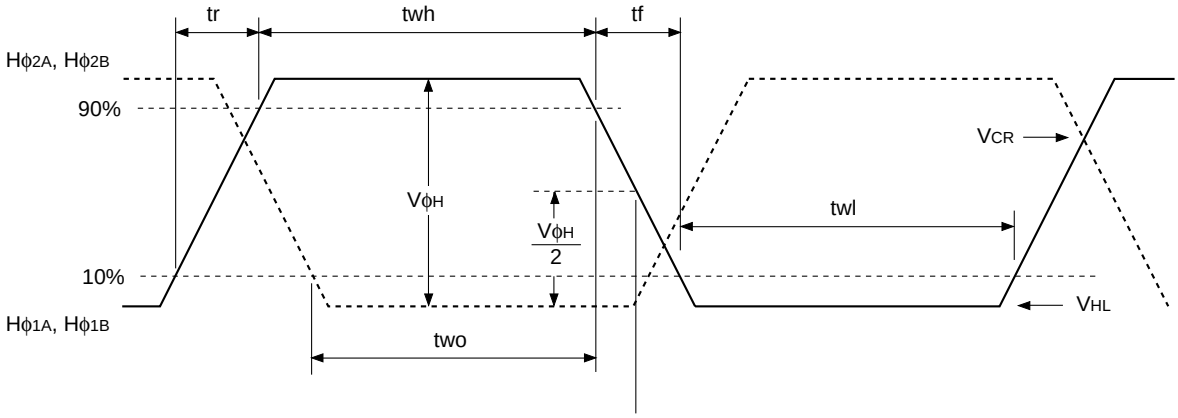


(2) Vertical transfer clock waveform



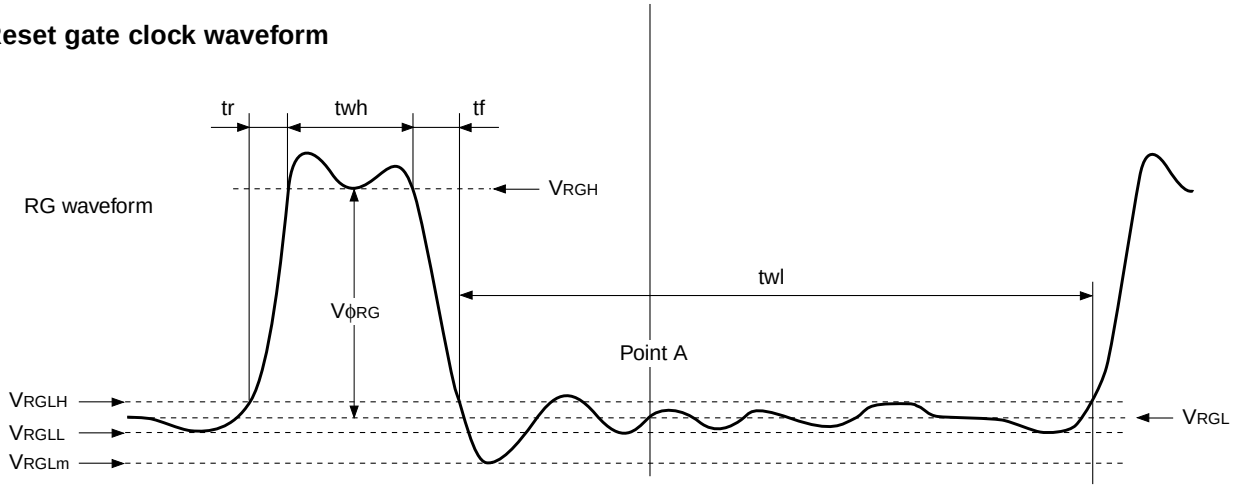
$V_{VH} = (V_{VH1} + V_{VH2})/2$
$V_{VL} = (V_{VL3} + V_{VL4})/2$
$V_{\phi V} = V_{VH}n - V_{VL}n$ (n = 1 to 4)

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is two.

(4) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

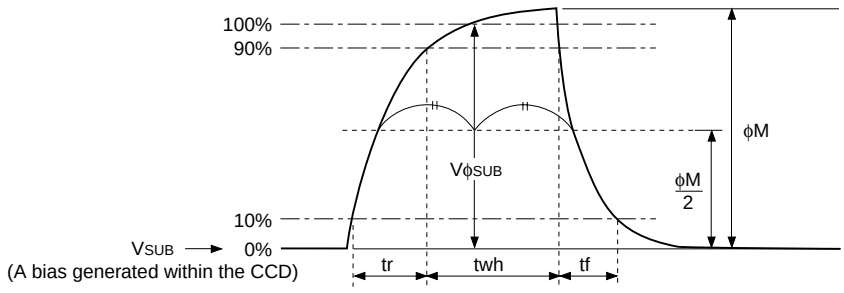
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval with twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform



Clock Switching Characteristics (Horizontal drive frequency: 22.5MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.47	2.67						0.5			0.5		µs	During readout
Vertical transfer clock	Vφ1A, Vφ1B, Vφ1C, Vφ2, Vφ3A, Vφ3B, Vφ3C, Vφ4										15		350	ns	When using CXD3400N
Horizontal transfer clock	Hφ1A, Hφ1B	13	16		13	16			6.5	9.5		6.5	9.5	ns	During imaging, tf ≥ tr – 2ns
	Hφ2A, Hφ2B	13	16		13	16			6.5	9.5		6.5	9.5		
Reset gate clock	φRG	6	8			31			3			3		ns	
Substrate clock	φSUB	2.0	2.58							0.5			0.5	µs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	Hφ1A, Hφ1B, Hφ2A, Hφ2B	11	16		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

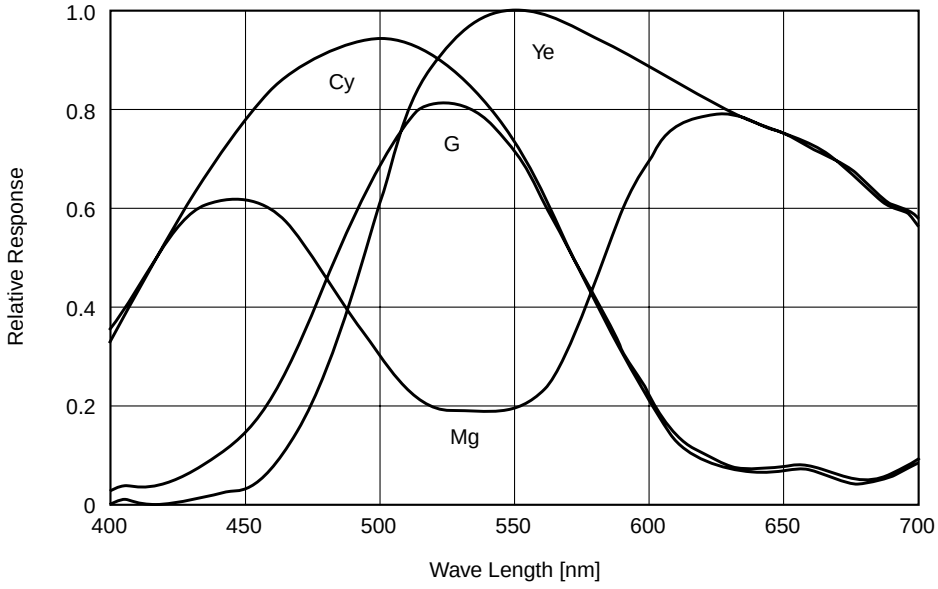


Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks	
Sensitivity	S	264	330		mV	1	1/30s accumulation, no line addition*1, *2	
Sensitivity comparison	R_{MgG}	0.75		1.35		2		
	R_{YeCy}	1.10		1.43				
Saturation signal	Vsat	450			mV	3	Ta = 60°C	No line addition*1
	Vsat2	900						2-line addition*3
Smear	Sm		–92	–84	dB	4	Frame readout mode*4	
			–86	–78			2× speed mode (1)*5	
			–80	–72			8× speed mode	
Video signal shading	SH			20	%	5	Zone 0 and I	
				25			Zone 0 to II'	
Dark signal	Vdt			16	mV	6	Ta = 60°C, 3.75 frame/s	
Dark signal shading	ΔVdt			8	mV	7	Ta = 60°C, 3.75 frame/s, *6	
Lag	Lag			0.5	%	8		

*1 Frame readout mode, 2× speed mode (1), and center scan modes (1), (2), (3) and (4).

*2 When the accumulation time is constant, 2-line addition modes have a sensitivity double that of modes without line addition.

*3 2× speed mode (2), 8× speed mode, and AF mode (1), (2)

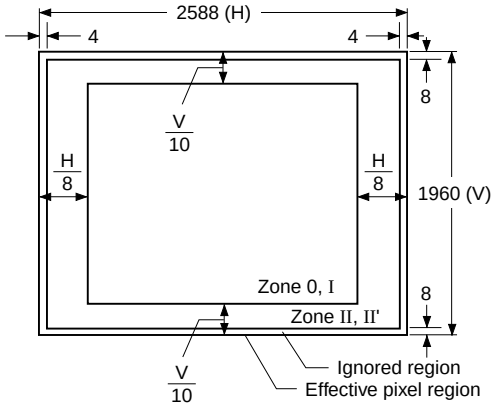
*4 After closing the mechanical shutter, the smear can be reduced to below the detection limit by performing vertical register sweep operation. This is also the same for 2× speed mode (2) and center scan modes (3) and (4).

*5 Smear can be reduced by approximately 30dB to a level of approximately –116dB (typ.) by performing the following sequence.

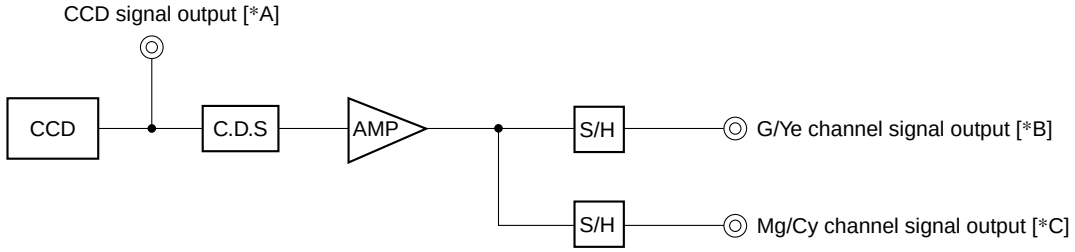
Vertical register high-speed transfer → Readout (SG) → Mechanical shutter closed → Signal output

*6 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

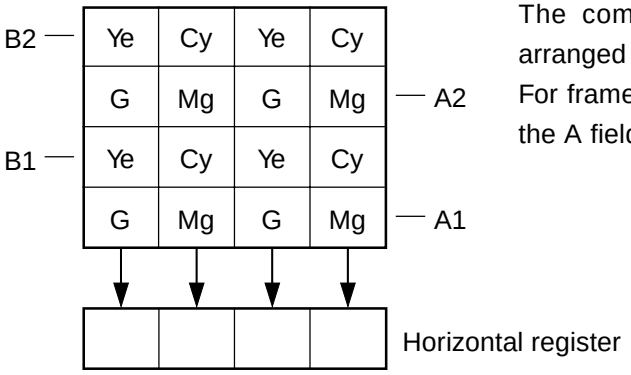
Image Sensor Characteristics Measurement Method

◎ Measurement conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Y signal output or chroma signal output of the measurement system.

◎ Color coding of this image sensor & Composition of luminance (Y) and chroma (color difference) signals



Color Coding Diagram

The complementary color filters of this image sensor are arranged in the layout shown in the figure on the left.
For frame readout, the A1 and A2 lines are output as signals in the A field, and the B1 and B2 lines in the B field.

These signals are processed to form the Y signal and chroma (color difference) signal sa follws.
The approximation:

$$Y = \{G + Mg + Ye + Cy\} \times 1/4$$
$$= 1/4 \{2B + 3G + 2R\}$$

is used for the Y signal, and the approximation:

$$R - Y = \{(Mg + Ye) - (G + Cy\}$$
$$= \{2R - G\}$$
$$B - Y = \{(Mg + Cy) - (G + Ye)\}$$
$$= \{2B - G\}$$

are used for the chroma (color difference) signal.

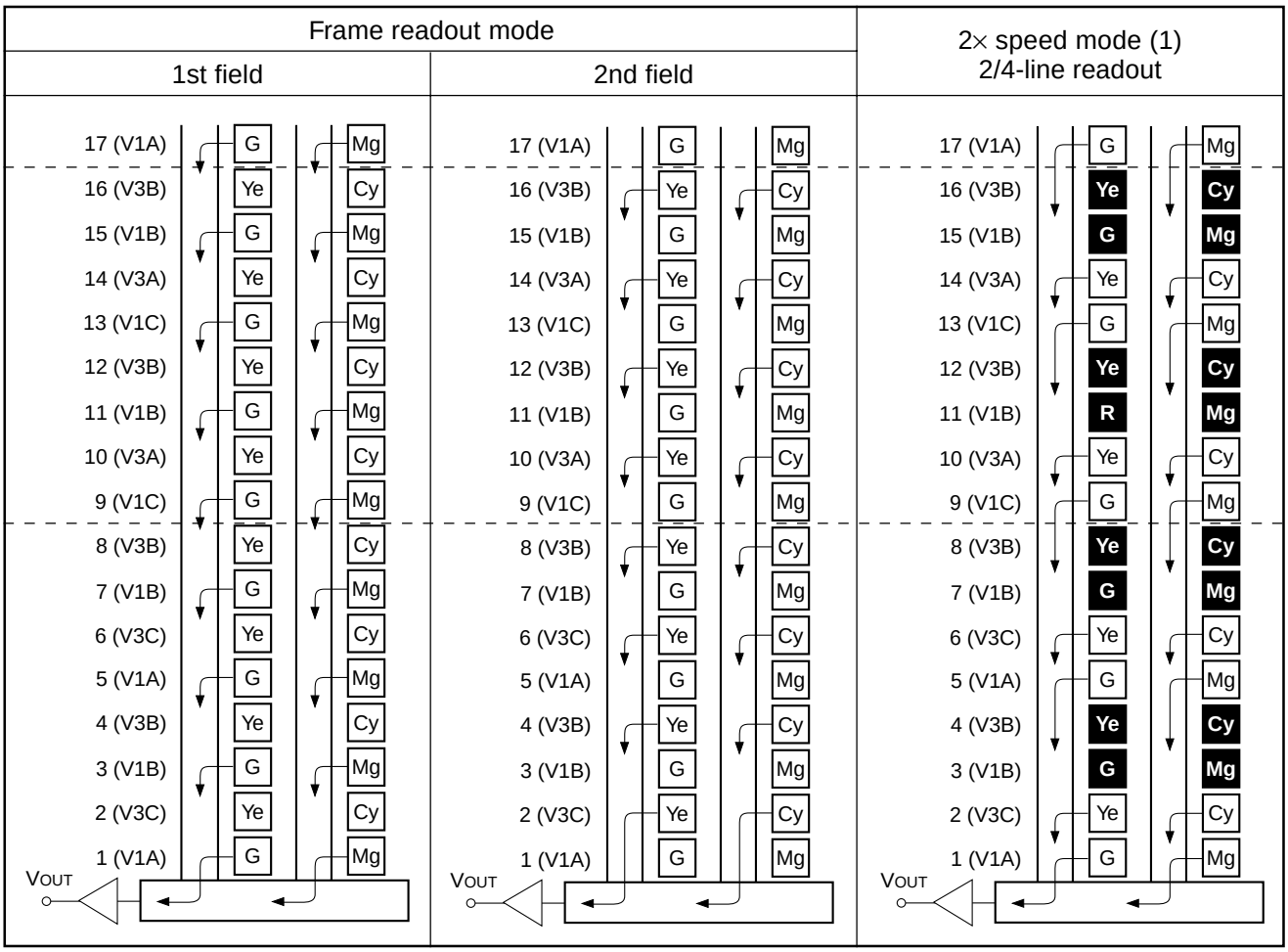
◎ Readout modes list

The readout method, frame rate, number of output lines and other information for each readout mode are shown in the table below.

Mode	Readout method	High-speed sweep for preventing smear	Addition method	Frame rate [frame/s]		Number of output effective image data lines
				NTSC	PAL	
Frame readout	Frame readout	Yes	None	3.75	3.57	1960
2× speed (1)	2/4 lines	Yes	None	7.49	7.14	980
2× speed (2)	Frame readout	Yes	Vertical 2 lines	6.66	6.25	980
8× speed	4/16 lines	None	Vertical 2 lines	29.97	25	245
Center scan (1)	2/4 lines	None	None	14.985	12.5	NTSC: 484, PAL: 587
Center scan (2)	2/4 lines	None	None	26.35		246
Center scan (3)	Frame readout	Yes	None	7.02		968
Center scan (4)	Frame readout	Yes	None	11.988	10	NTSC: 492, PAL: 620
AF (1)	4/16 lines	None	Vertical 2 lines	59.94	50	NTSC: 104, PAL: 128
AF (2)	4/16 lines	None	Vertical 2 lines	119.88	100	NTSC: 34, PAL: 46

◎ Description of frame readout mode

The output methods for the following readout modes are shown below.



Note) Blacked out portions in the diagram indicate pixels which are not read out.

1. Frame readout mode

   In this mode, all pixel signals are divided into two fields and output.

   All pixel signals are read out independently, making this mode suitable for high resolution image capturing.

2. 2× speed mode (1) 2/4-line readout

   All effective area signals are output in half the time of frame readout mode by reading out 2 lines for every 4 lines.

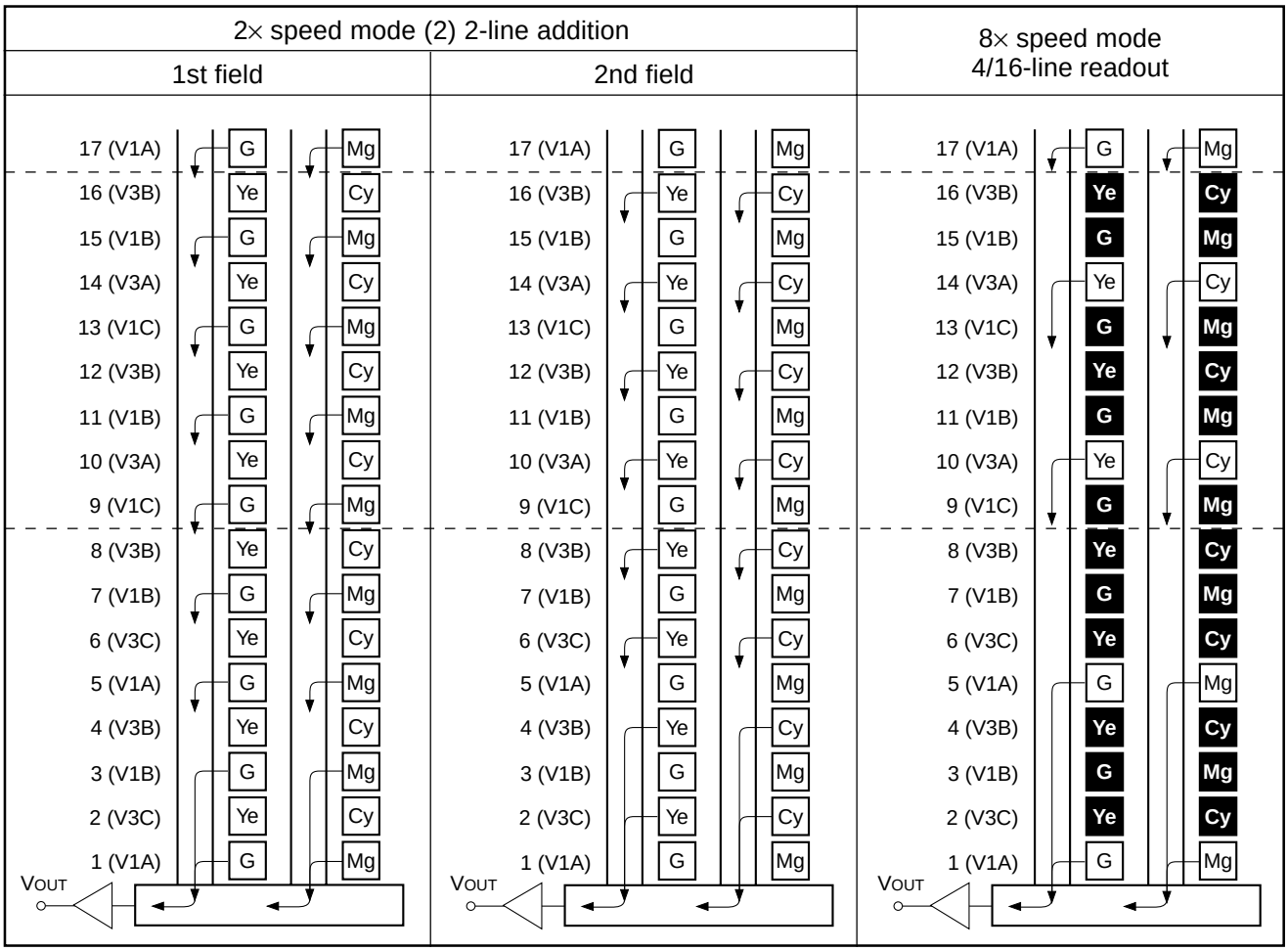
   The number of output lines is halved, but all color signals can be output in a single field, so exposure completed is read out (SG), making high-speed shutter operation possible.

   However, note that the G/Mg and Ye/Cy line readout timings have a time difference of approximately 6.7µs (150clk).

   In addition, using high-speed sweep transfer and the mechanical shutter is recommended to suppress smear.

   Smear is reduced by approximately 30dB by performing the following sequence.

   Vertical register high-speed transfer → Readout (SG) → Mechanical shutter closed → Signal output



Note) Blacked out portions in the diagram indicate pixels which are not read out.

3. 2× speed mode (2) 2-line addition

In this mode, the G/Mg line is read out in the 1st field and the Ye/Cy line in the 2nd field, 2 lines are transferred during the horizontal blanking period, and 2 lines are added in the horizontal register.

All pixel signals are divided into two fields and output in approximately half the time (slightly longer than half) of frame readout mode.

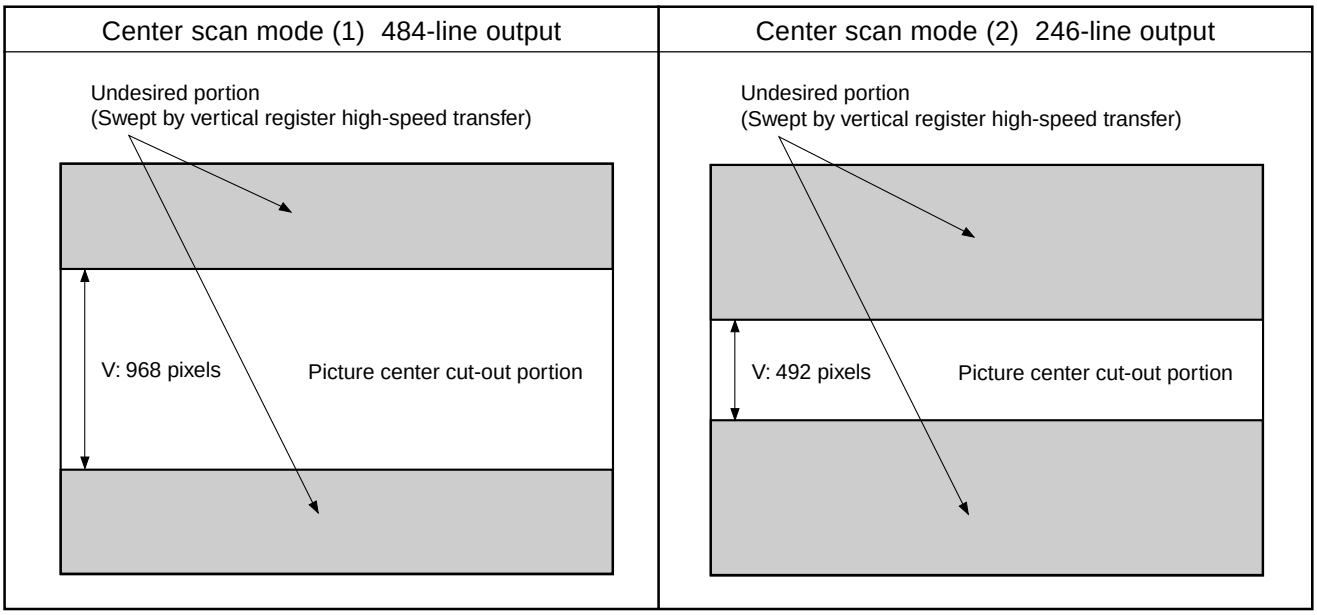
At this time, the sensitivity (for 1/30s accumulation) and saturation signal level are double that during frame readout mode, allowing high sensitivity imaging with a wide dynamic range.

4. 8× speed mode, 4/16-line readout

All effective area signals are output in 1/8 the time of frame readout mode by reading out 4 lines for every 16 lines, transferring 4 lines during the horizontal blanking period, and adding 2 lines in the horizontal register. The number of output lines is 245 lines.

However, note that the G/Mg and Ye/Cy line readout timings have a time difference of approximately 6.7µs (150clk).

This mode emphasizes processing speed over vertical resolution, making it suitable for AE/AF and other control and for image verification on LCD viewfinders.



5. Center scan mode (1) 484-line output

This mode sweeps the undesired portions by vertical register high-speed transfer, and outputs only the vertical 968-pixel region of the picture center by reading out 2 lines for every 4 lines (like 2× speed mode (1)).

The number of output lines is 484 lines.

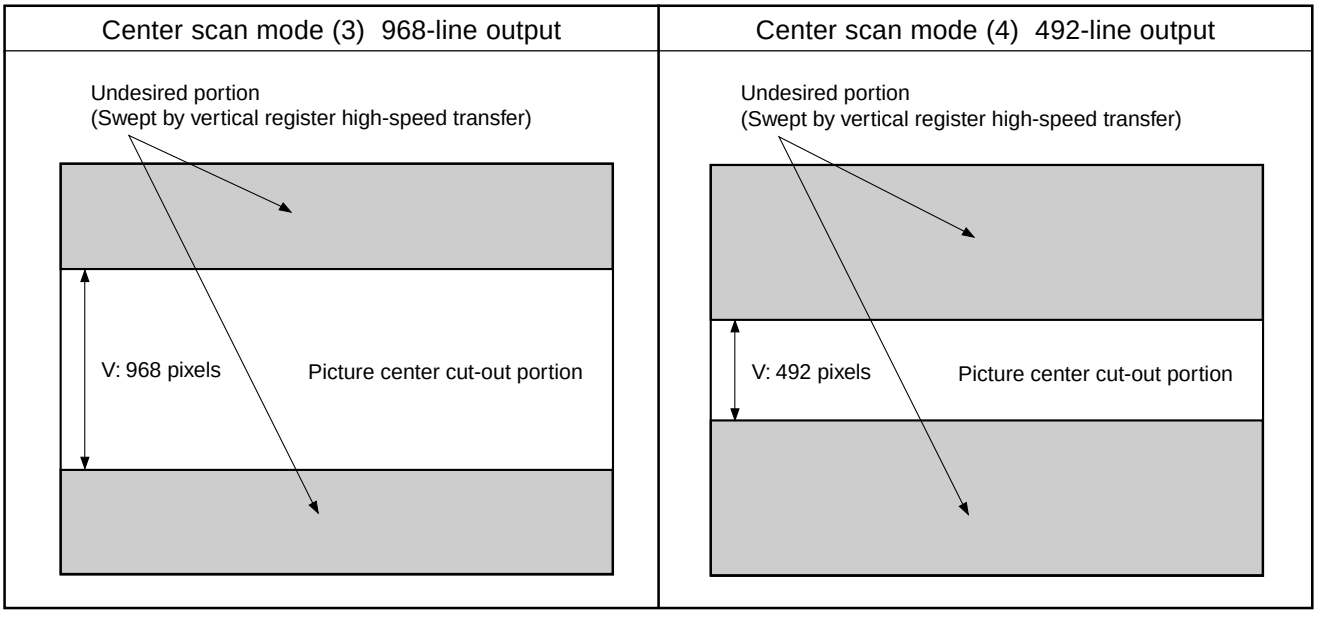
The frame rate is increased (approximately 15 frames/s) by setting the number of vertical output lines to that of VGA mode, making this mode suitable for VGA moving pictures. (However, the angle of view is equivalent to 2× electronic zoom.)

6. Center scan mode (2) 246-line output

This mode sweeps the undesired portions by vertical register high-speed transfer, and outputs only the vertical 492-pixel region of the picture center by reading out 2 lines for every 4 lines (like 2× speed mode (1)).

The number of output lines is 246 lines.

This mode is suitable for enlarged display when verifying image on LCD viewfinders.



7. Center scan mode (3) 968-line output

This mode sweeps the undesired portions by vertical register high-speed transfer, and outputs only the vertical 968-pixel region of the the picture center divided into two fields (like frame readout mode).

The number of output lines is 968 lines.

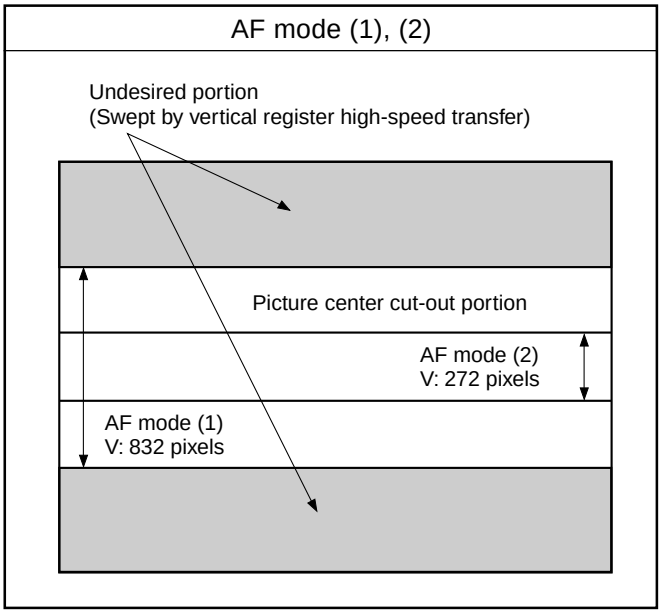
This mode is used to shorten the frame rate when shooting 2× electronic zoom image.

8. Center scan mode (4) 492-line output

This mode sweeps the undesired portions by vertical register high-speed transfer, and outputs only the vertical 492-pixel region of the picture center divided into two fields (like frame readout mode).

The number of output lines is 492 lines.

This mode is used to shorten the frame rate when shooting 4× electronic zoom image.



9. AF modes (1), (2)

The AF modes are used to achieve even higher-speed AF control than 8× speed mode.

AF mode (1) outputs only the vertical 832-pixel (in NTSC mode) region of the picture center at approximately 60 frames/s by reading out 4 lines for every 16 lines (like 8× speed mode).

AF mode (2) outputs only the vertical 272-pixel (in NTSC mode) region of the picture center at approximately 120 frames/s by reading out 4 lines for every 16 lines (like 8× speed mode).

The number of output lines for each mode is shown below.

	AF mode (1)		AF mode (2)	
NTSC mode	60 frame/s	104 lines	120 frame/s	34 lines
PAL mode	50 frame/s	128 lines	100 frame/s	46 lines

◎ Definition of standard imaging conditions

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to the standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_G, V_{Mg}, V_{Ye} and V_{Cy}) at the center of each G, Mg, Ye and Cy channel screen, and substitute the values into the following formulas.

$$V = (V_G + V_{Mg} + V_{Ye} + V_{Cy})/4$$

$$S = V \times \frac{100}{30} \text{ [mV]}$$

2. Saturation comparison
Set to the standard imaging condition II: Adjust the luminous intensity so that the average value of the G/Mg/Ye/Cy channel signal output is 150mV, and then measure the Mg signal output (S_{Mg} [mV]) and G signal output (S_G [mV]), and the Ye signal output (S_{Ye} [mV]) and Cy signal output (S_{Cy} [mV]) at the center of the screen. Substitute the values into the following formulas.

$$R_{MgG} = S_{Mg}/S_G$$
$$R_{YeCy} = S_{Ye}/S_{Cy}$$

3. Satutation signal
Set to standaed imageing condition II. After adjusting the luminous intensity to 10 times the intsnsity with the avarage value of the G/Mg/Ye/Cy channel signal output, 150mV, measure the minimum values of the G, Mg, Ye and Cy signal outputs.

4. Smear
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of the G/Mg/Ye/Cy channel signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (V_{Sm} [mV]) independent of the G, Mg, Ye and Cy signal outputs, and substitute the values into the following formula.
The smear for modes other than frame readout mode is calculated from the storage time and signal addition method. As a result, 2× speed mode (2) is the same, 2× speed mode (1) is double, and 8× speed mode is 4 times that for frame readout mode.

$$Sm = 20 \times \log \left(\frac{V_{Sm}}{150} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB] (1/10V method conversion value)}$$

5. Video signal shading

Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the G/Mg/Ye/Cy channel signal output is 200mV. Then measure the maximum value (Vmax [mV]) and minimum value (Vmin [mV]) of the G/Mg/Ye/Cy channel signal output and substitute the values into the following formula.

$$SH = (Vmax - Vmin)/150 \times 100\ [\%]$$

6. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading

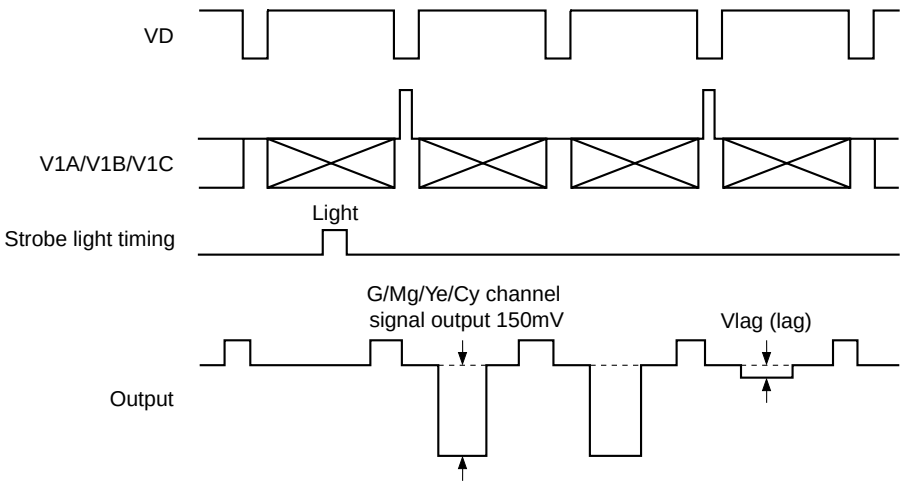
After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta Vdt = Vdmax - Vdmin\ [mV]$$

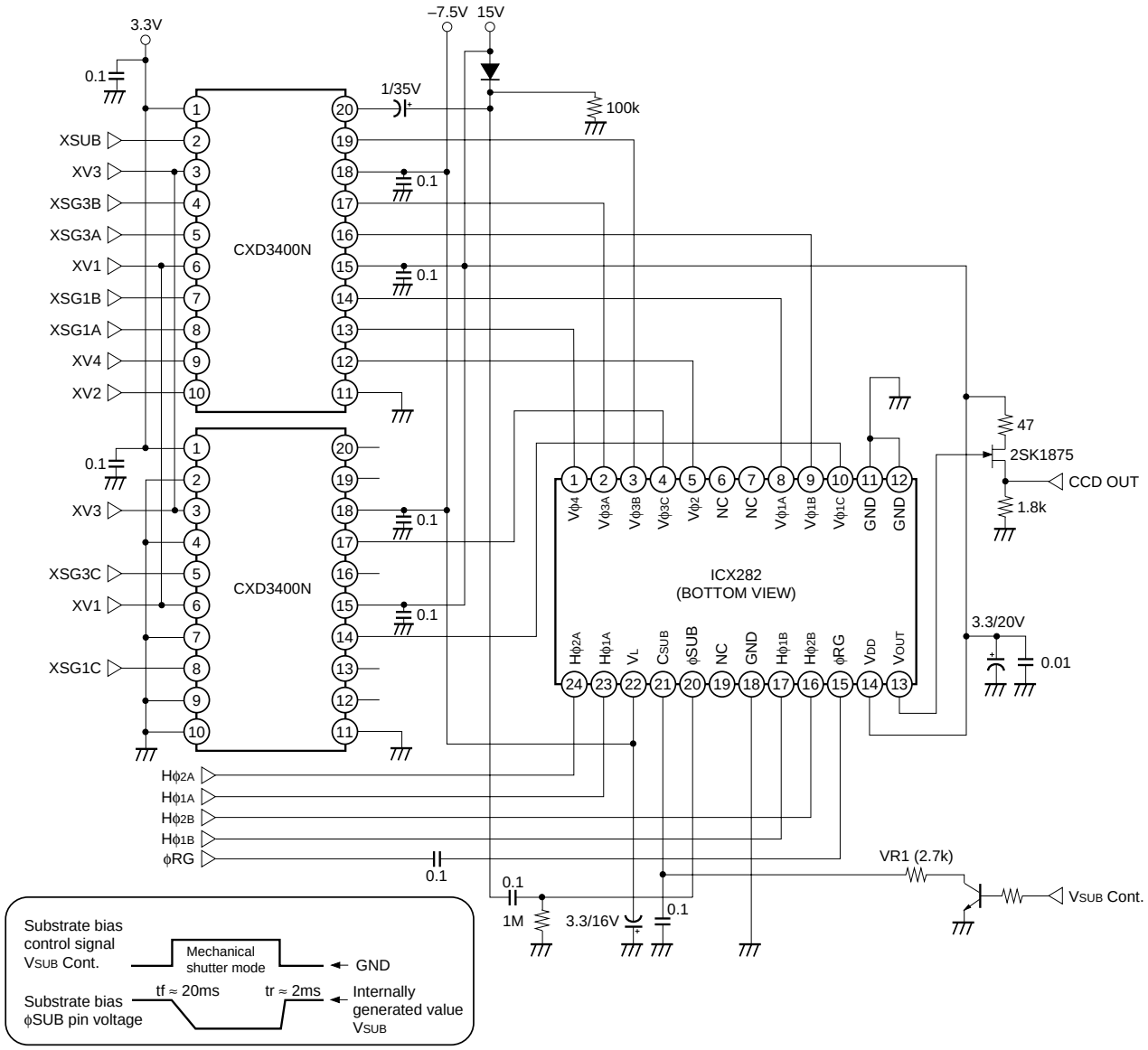
8. Lag

Adjust the G/Mg/Ye/Cy channel output generated by the strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

$$Lag = (Vlag/150) \times 100\ [\%]$$



Drive Circuit



Notes)

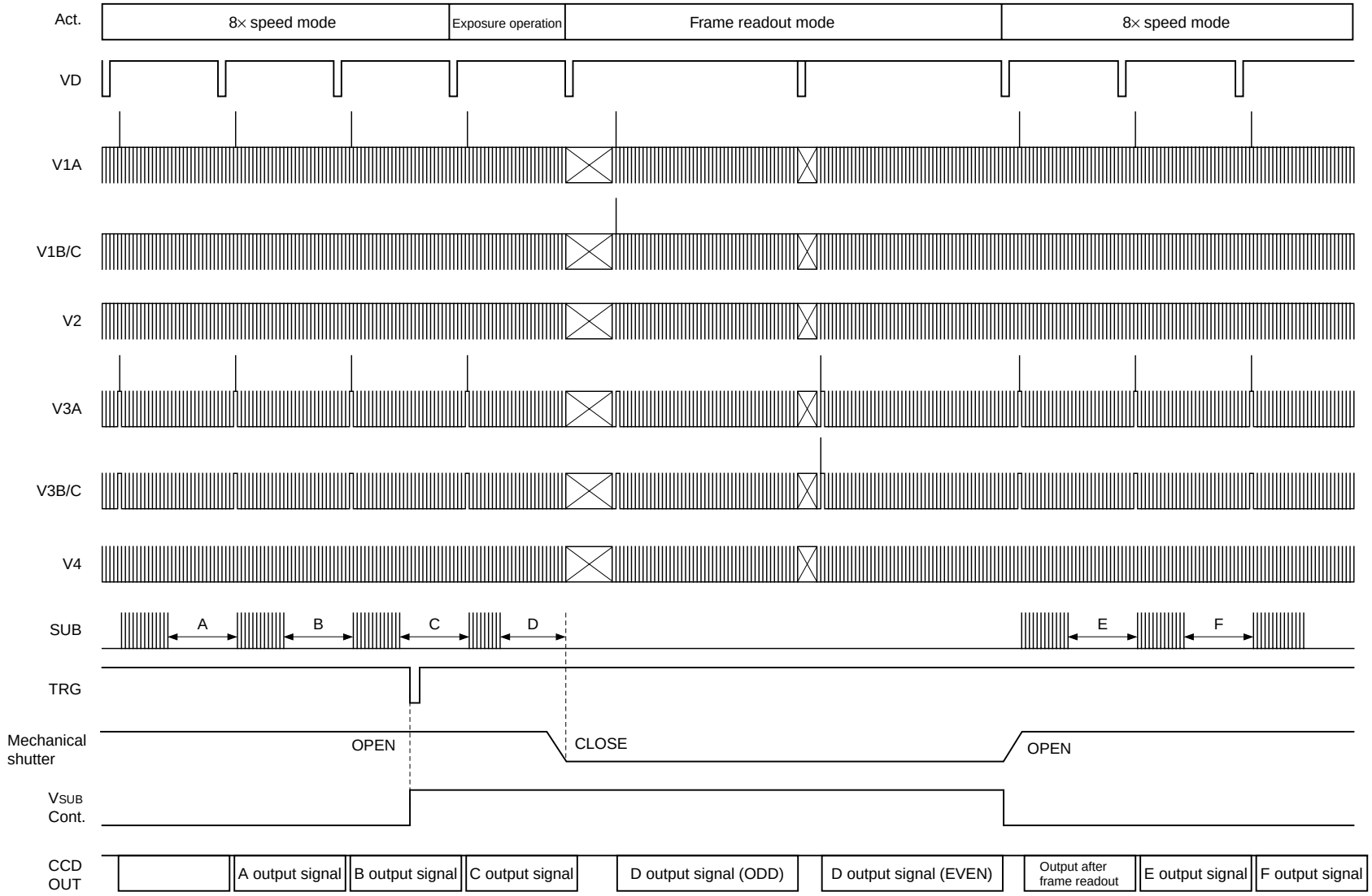
Substrate bias control

1. The saturation signal level decreases when exposure is performed using the mechanical shutter, so control the substrate bias.
2. A saturation signal level equivalent to that for continuous exposure can be assured by connecting a 2.7kΩ grounding registor to the CCD C_{SUB} pin.

Drive timing precautions

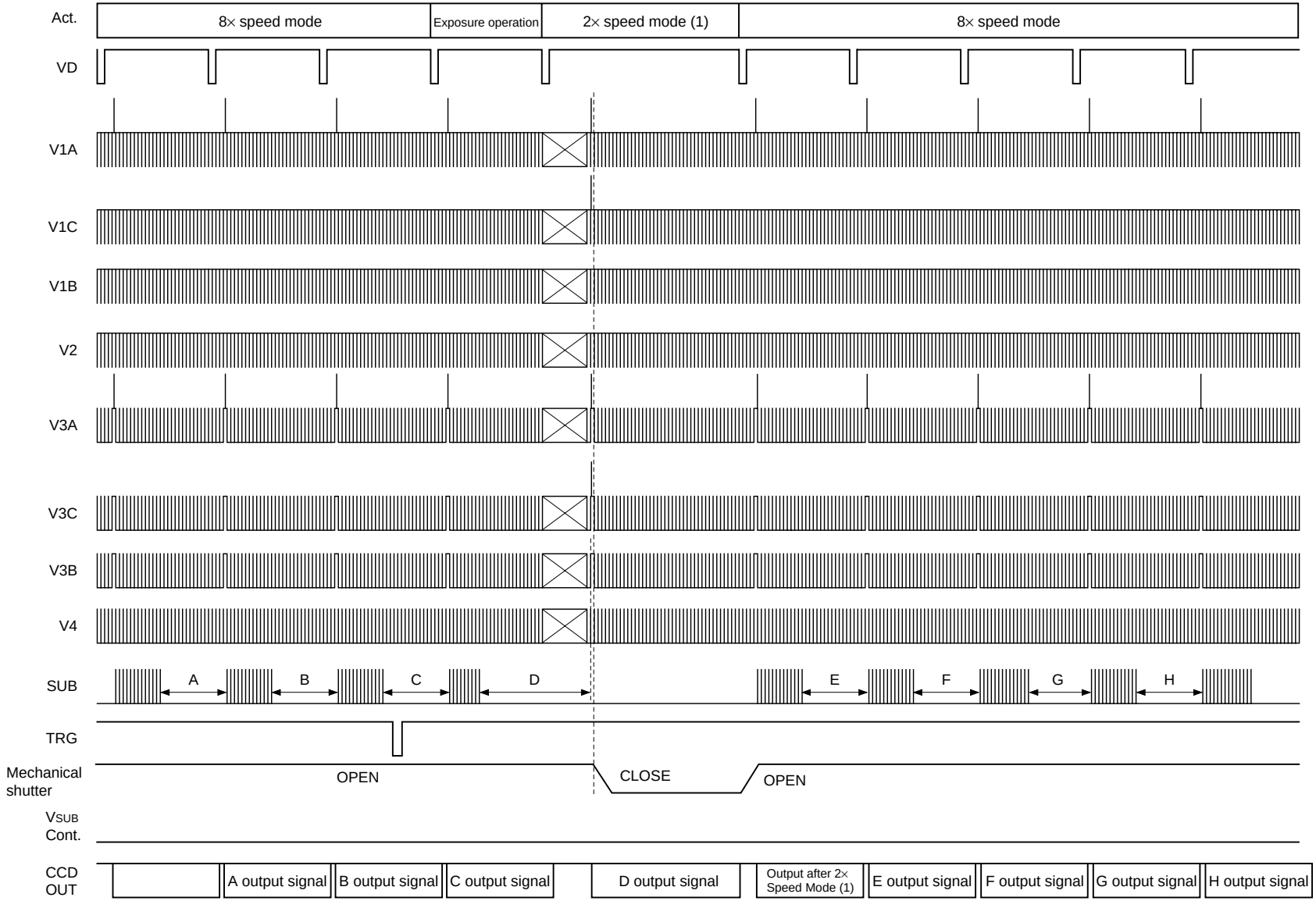
1. Blooming occurs in modes (2× speed (1), 8× speed, etc.) where exposure is not completed by closing the mechanical shutter, so do not ground the connected 2.7kΩ resistor.
2. tf is slow, so the internally generated voltage V_{SUB} may not drop to a sufficiently low level if the substrate bias control signal is not set to high level 30ms before entering the exposure period and the 2.7kΩ resistor connected to the C_{SUB} pin is not grounded.
3. The blooming signal generated during exposure in mechanical shutter mode is swept by providing one field or more (two fields is recommended) of idle transfer through vertical register high-speed sweep transfer from the time the mechanical shutter closes until sensor readout is performed. However, note that the V_L potential and the φSUB pin DC voltage sag at this time.
4. When exposure time is several seconds or more, we recommend the sequence that the substrate bias control is performed just before the completion of exposure (Mechanical shutter is closed.), not before the start of exposure.

Drive Timing Chart (Vertical Sequence) 8× Speed Mode → Frame Readout Mode (or 2× Speed Mode (1)) / Electronic Shutter Normal Operation



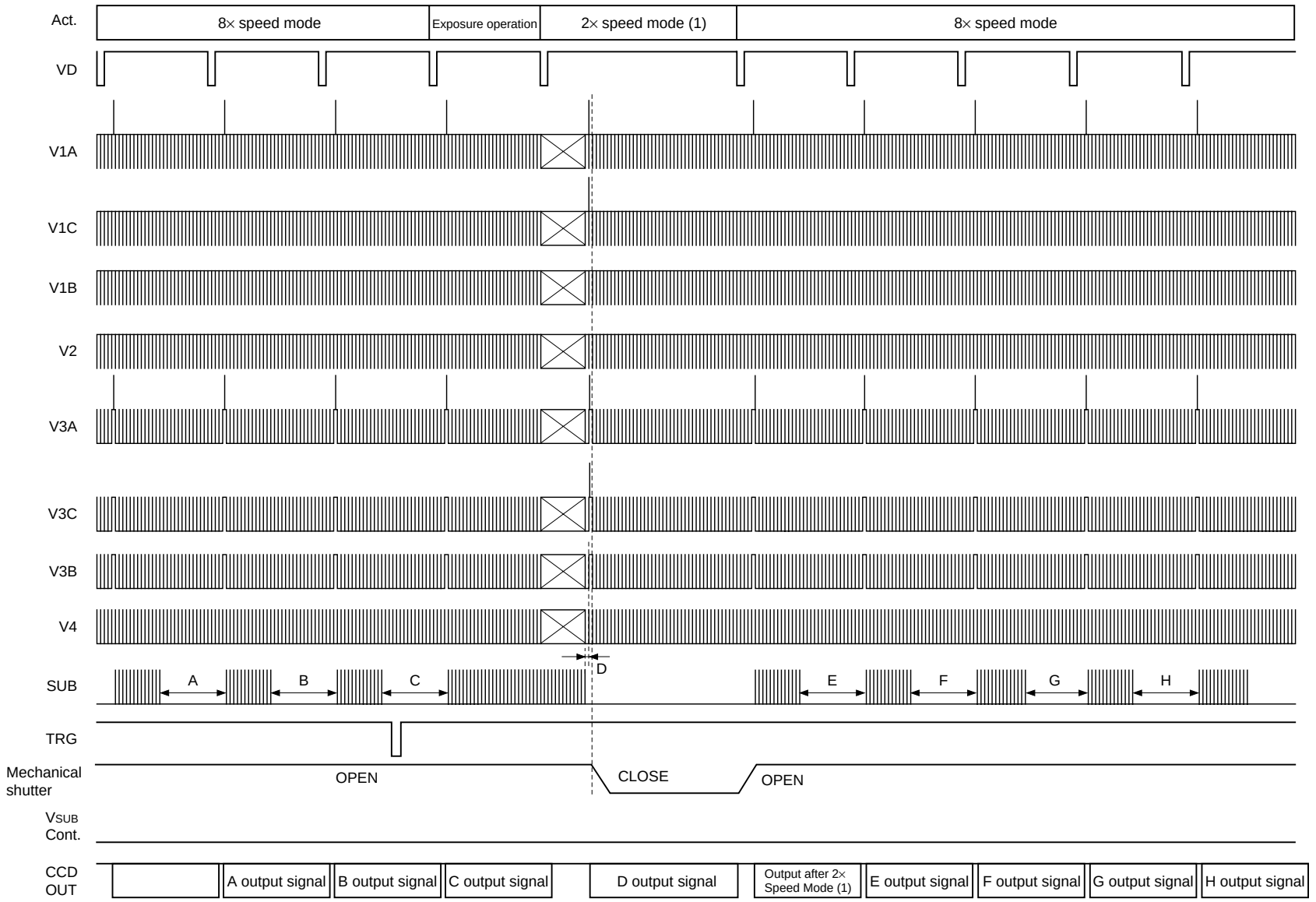
* The B and C output signals contain a blooming component and should therefore not be used.
* Apply 20 or more electronic shutter pulses at the start of exposure for the recording image. If less than 20 pulses are applied, the electronic shutter may occur a discharge error.

Drive Timing Chart (Vertical Sequence) 8× Speed Mode → 2× Speed Mode (1) / Electronic Shutter Normal Operation



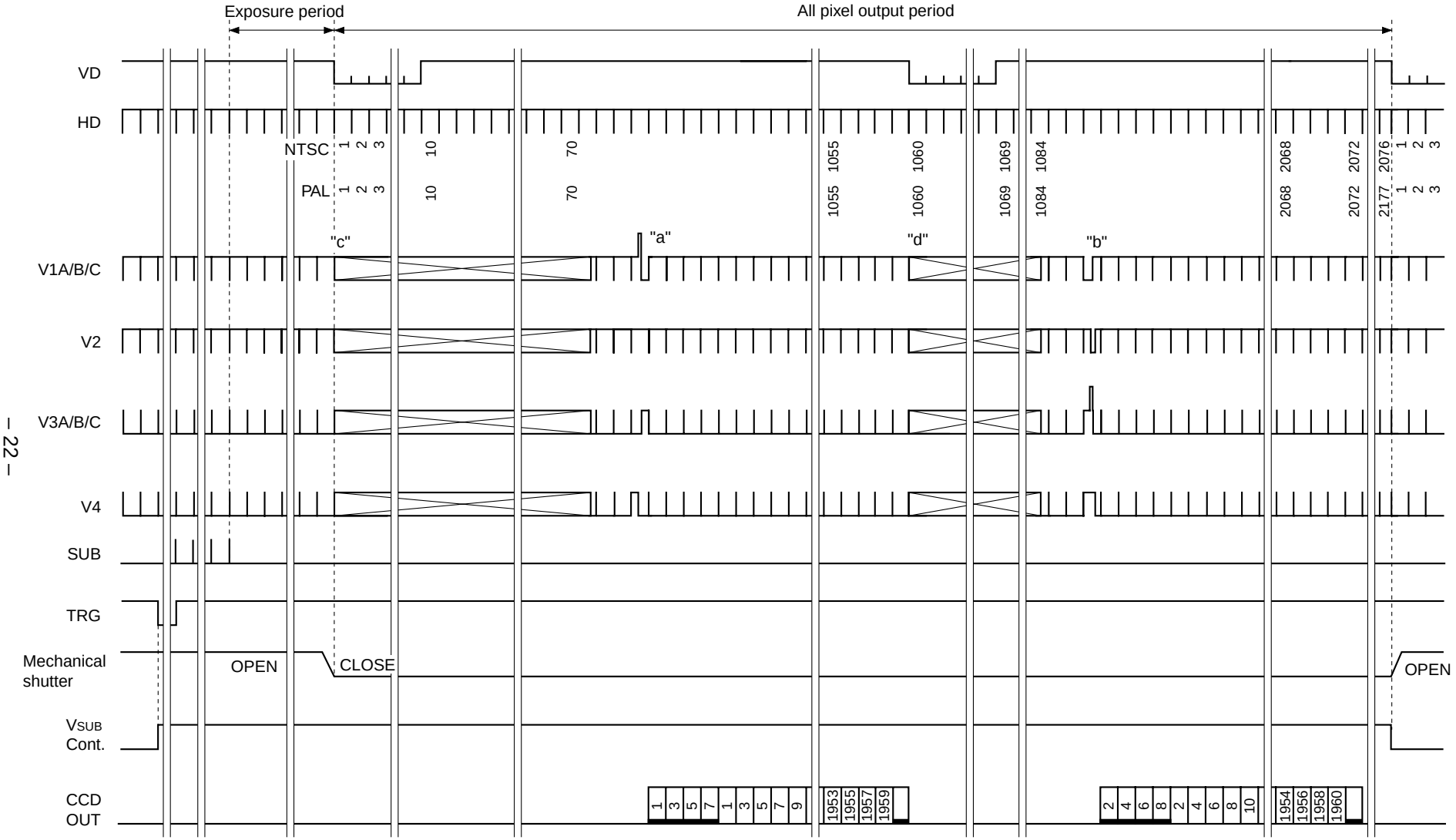
* The substrate bias control signal (V_{SUB} Cont.) should not be used in the above sequence.
* Apply 20 or more electronic shutter pulses at the start of exposure for the recording image. If less than 20 pulses are applied, the electronic shutter may occur a discharge error.

Drive Timing Chart (Vertical Sequence) 8× Speed Mode → 2× Speed Mode (1) / High-speed Shutter Operation



* The substrate bias control signal (V_{SUB} Cont.) should not be used in the above sequence.
* Apply 20 or more electronic shutter pulses at the start of exposure for the recording image. If less than 20 pulses are applied, the electronic shutter may occur a discharge error.

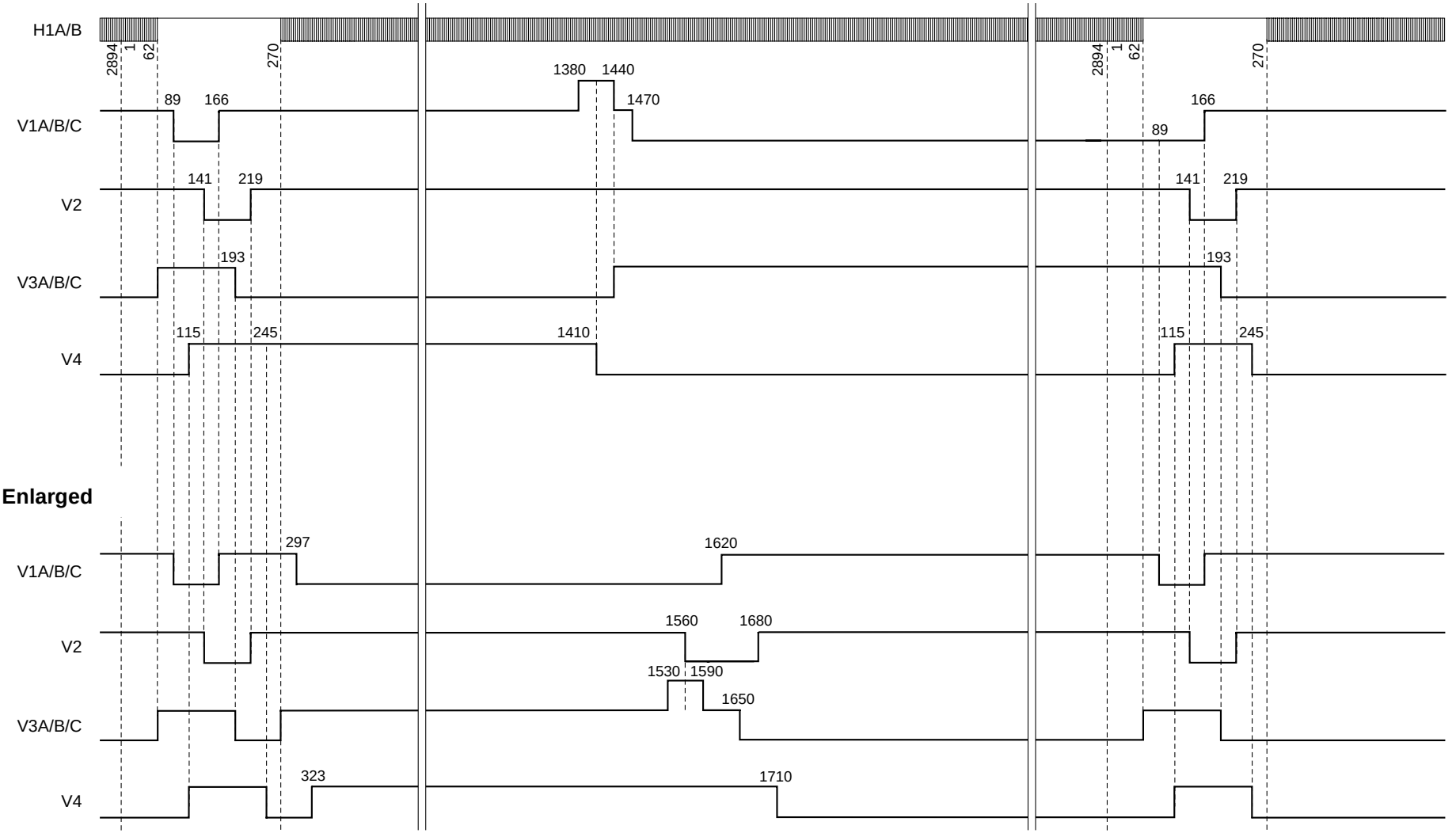
Drive Timing Chart (Vertical Sync) NTSC/PAL Frame Readout Mode



* 2894fH. However, 2076H in NTSC mode is 950 clk, and 2177H in PAL mode is 2656 clk.
Also, the number of high-speed sweep transfer stages and the transfer speed differ for the 1st field and 2nd field sides, so the fields should not be reversed.

Drive Timing Chart (Vertical Sync) **Frame Readout Mode**
Center Scan Mode (3) 968-line output
Center Scan Mode (4) 492-line output

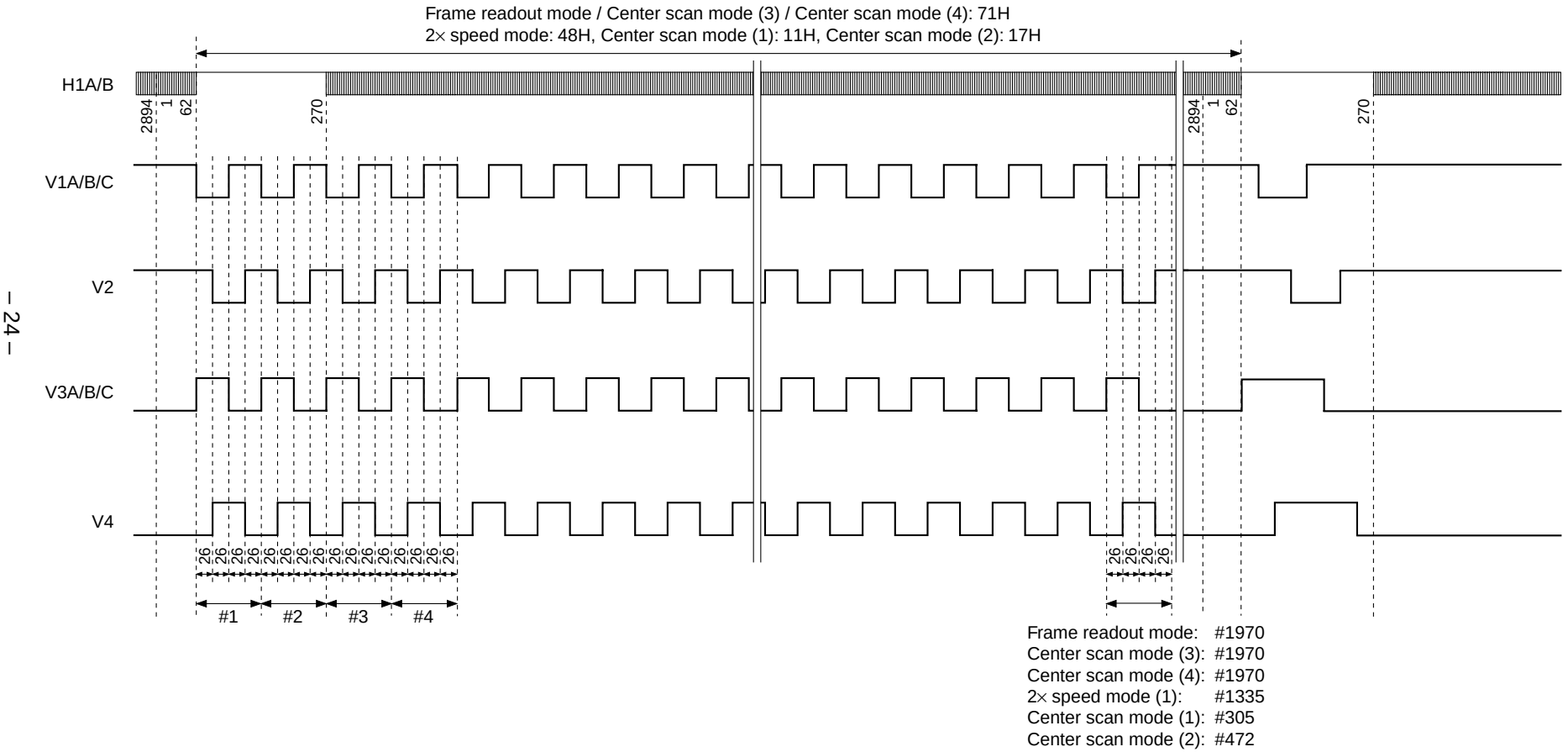
"a" Enlarged



"b" Enlarged

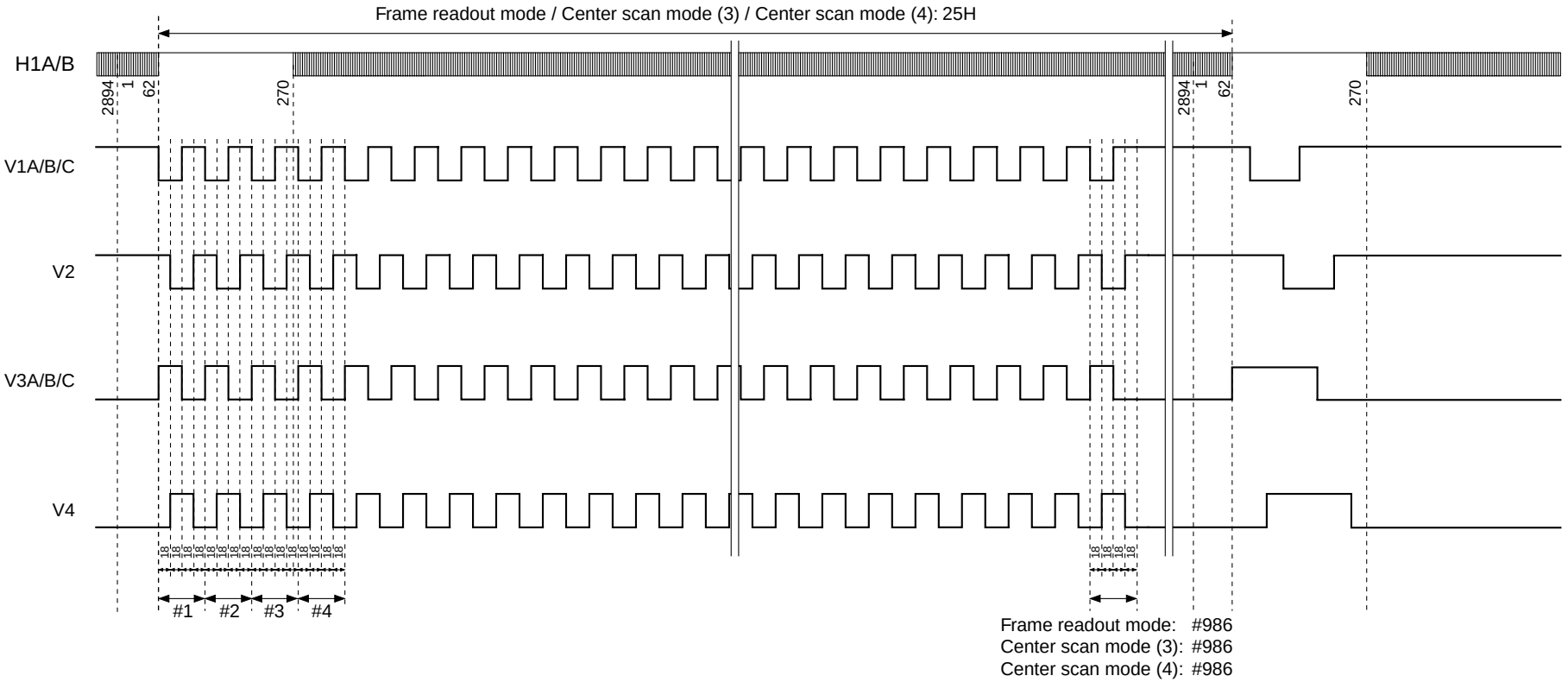
Drive Timing Chart (Vertical Sync) **Frame Readout Mode / Center Scan Mode (3) / Center Scan Mode (4)**
2× Speed Mode (1)
Center Scan Mode (1)
Center Scan Mode (2)

"c" Enlarged



Drive Timing Chart (Vertical Sync) Frame Readout Mode / Center Scan Mode (3) / Center Scan Mode (4)

"d" Enlarged



Drive Timing Chart (Horizontal Sync) **Frame readout mode**

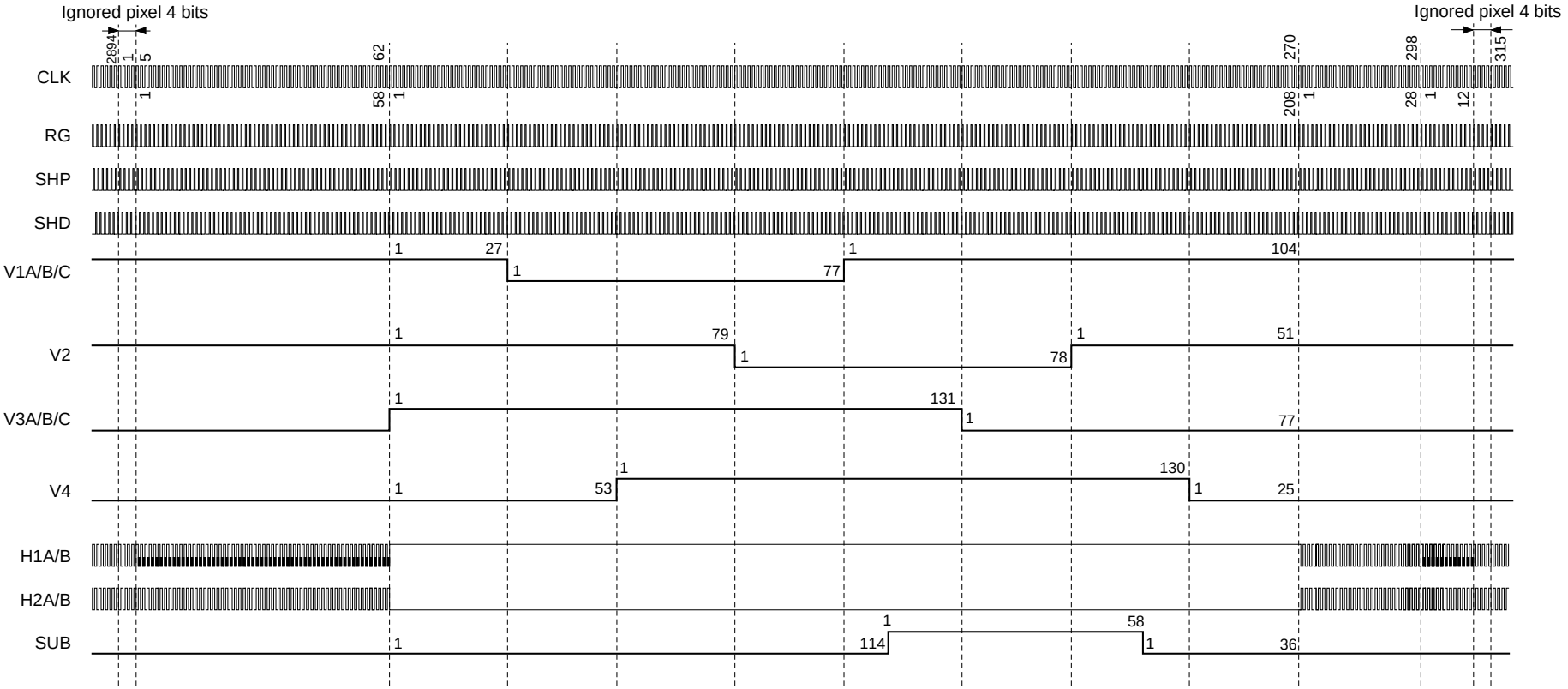
2× speed mode (1) 2/4-line readout

Center scan mode (1) 484-line output

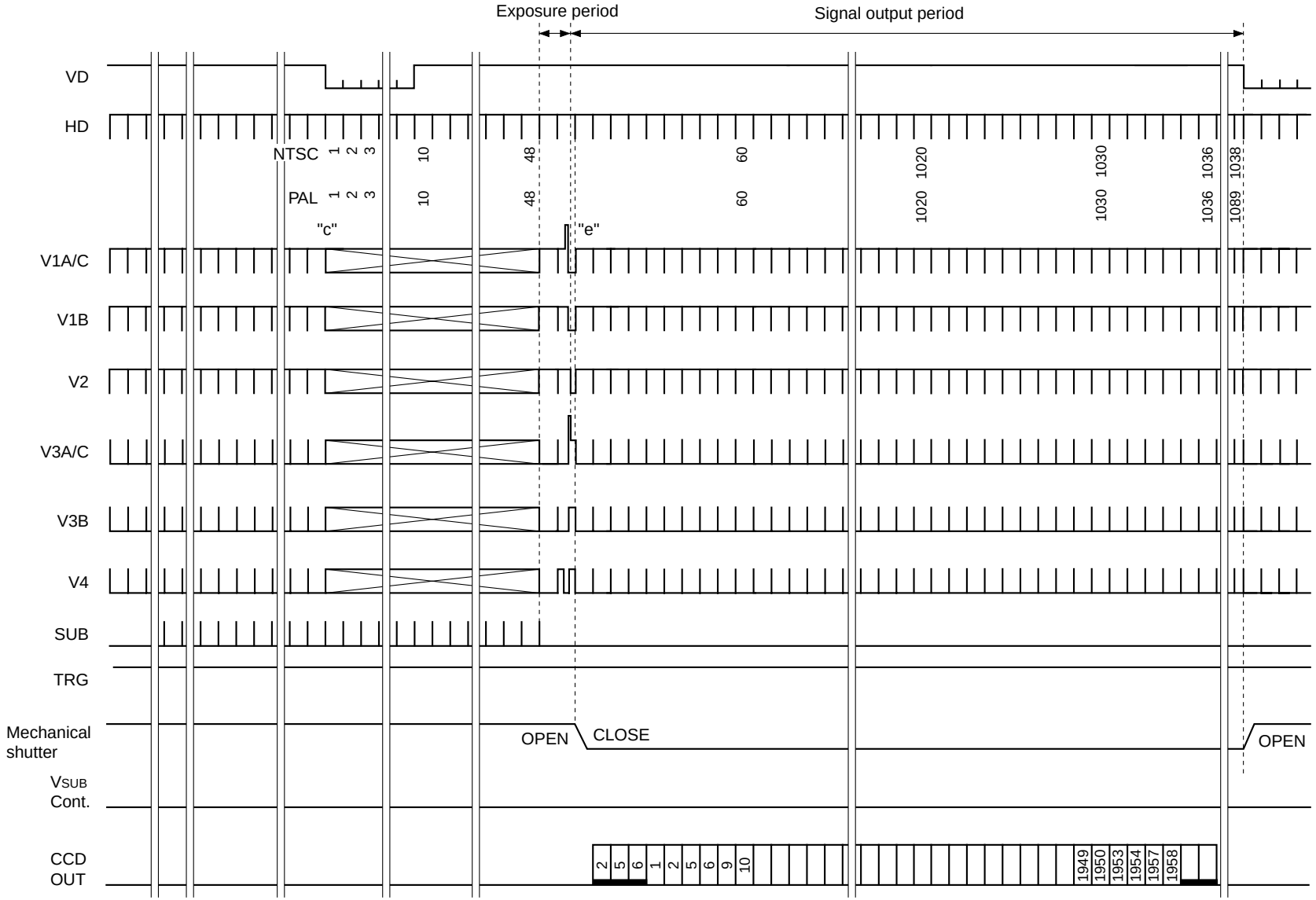
Center scan mode (2) 246-line output

Center scan mode (3) 968-line output

Center scan mode (4) 492-line output



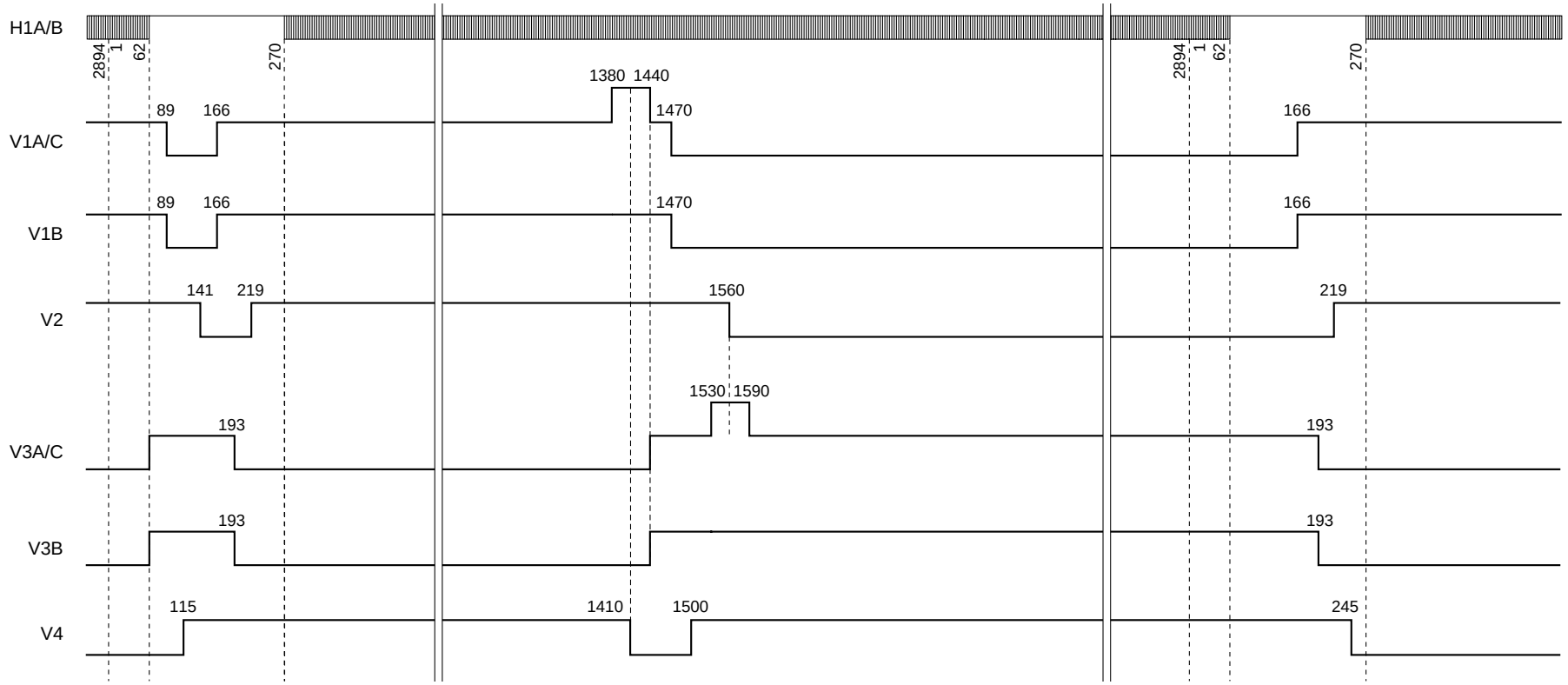
Drive Timing Chart (Vertical Sync) NTSC/PAL 2× Speed Mode (1) 2/4-line readout



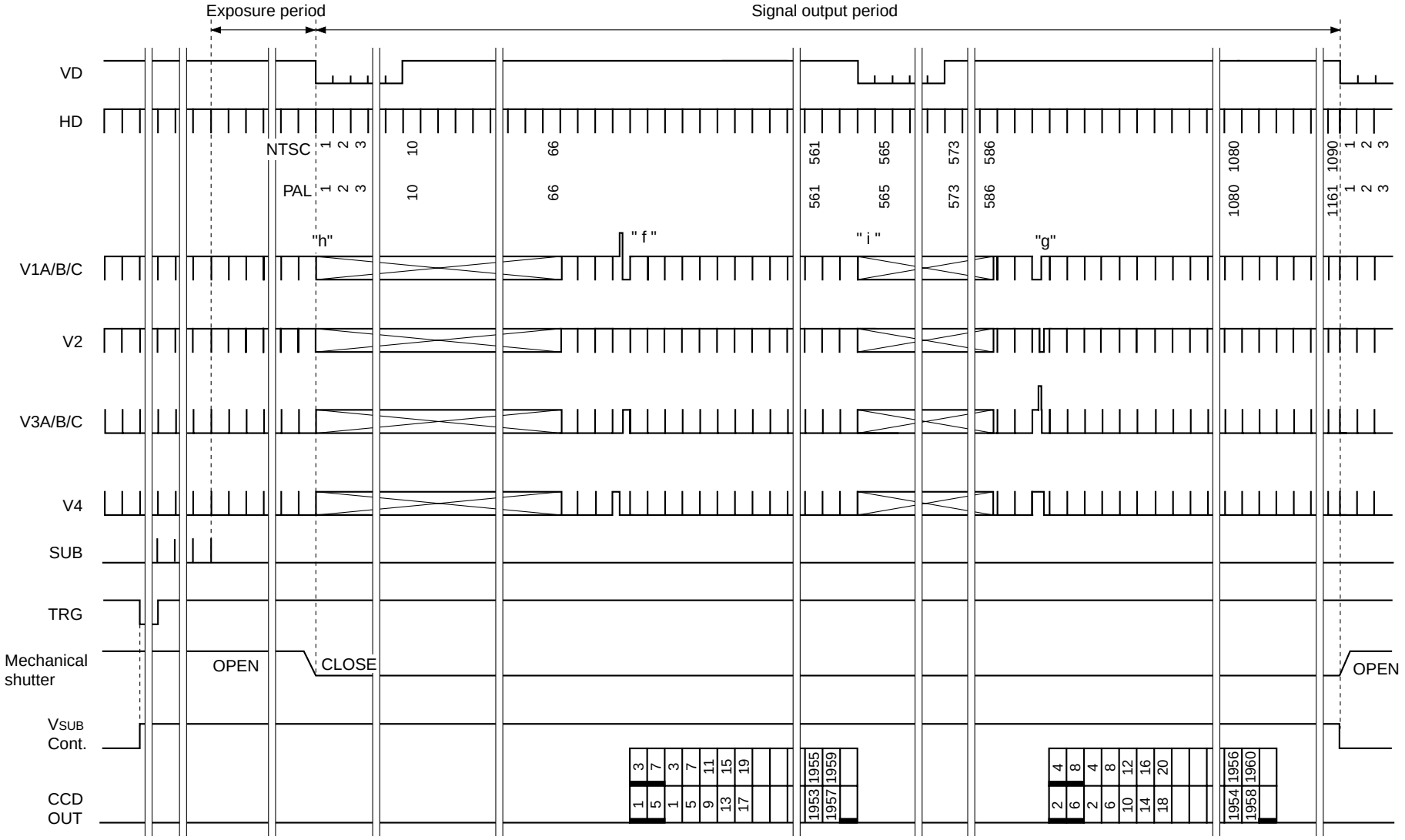
* 2894fH. However, 1038H in NTSC mode is 1922 clk, and 1089H in PAL mode is 1328 clk.

Drive Timing Chart (Vertical Sync) **2× Speed Mode (1) 2/4-line readout**
Center Scan Mode (1) 484-line output
Center Scan Mode (2) 246-line output

"e" Enlarged



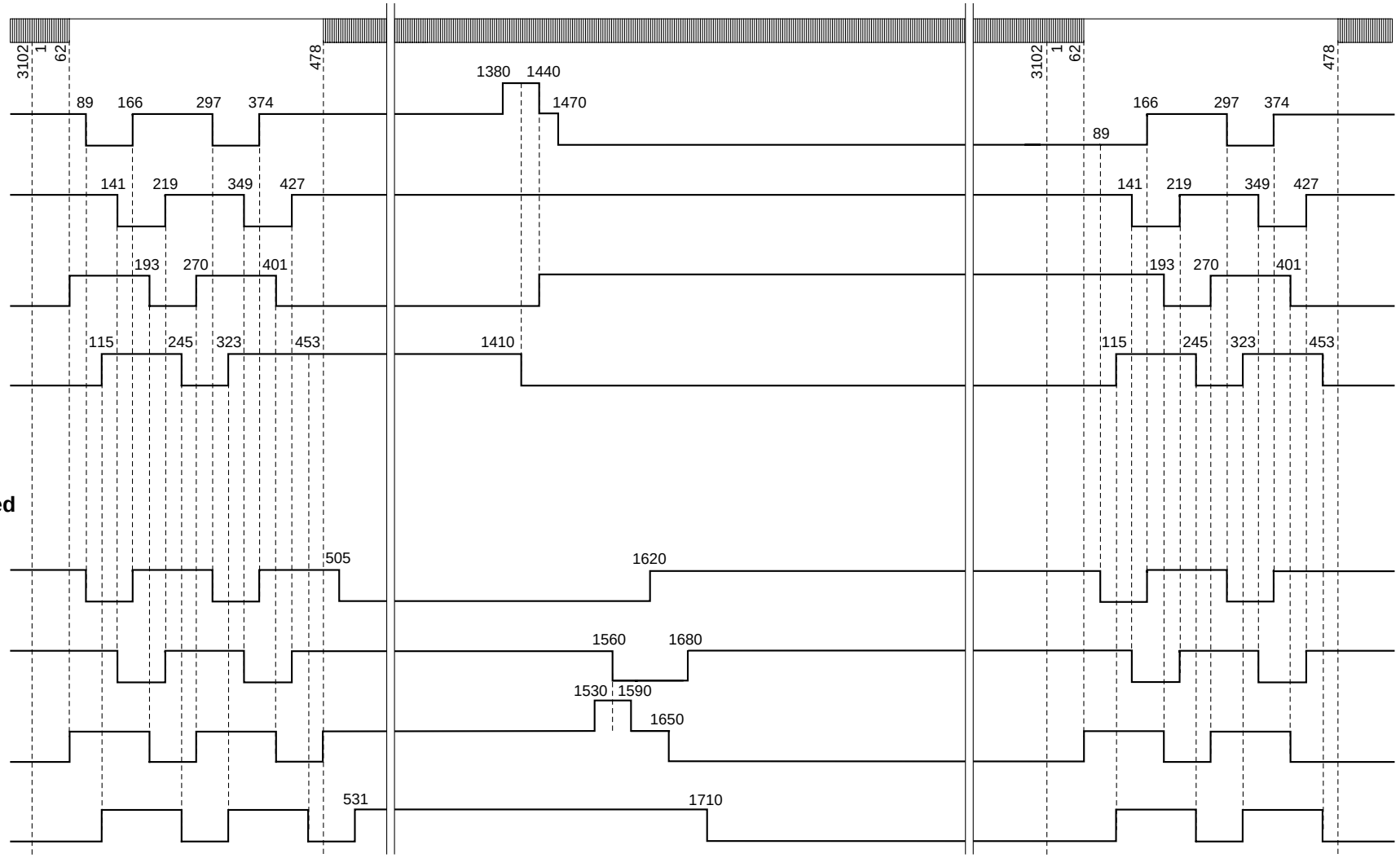
Drive Timing Chart (Vertical Sync) NTSC/PAL 2× Speed Mode (2) 2-line addition



* 3102fH. However, 1089H and 1090H in NTSC mode are 1700 clk and 1699 clk, respectively, and 1161H in PAL mode is 1680 clk.
Also, the number of high-speed sweep transfer stages and the transfer speed differ for the 1st field and 2nd field sides, so the fields should not be reversed.

Drive Timing Chart (Vertical Sync) 2× Speed Mode (2) 2-line addition

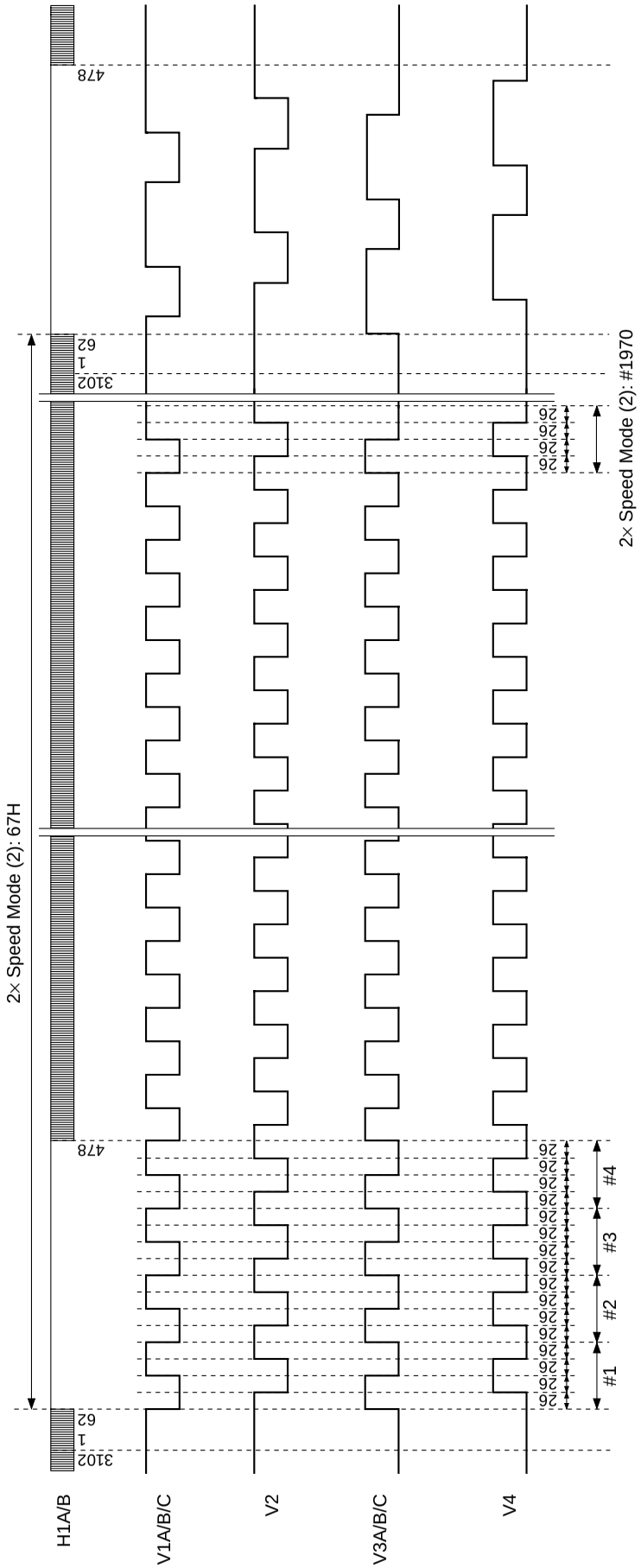
" f " Enlarged



"g" Enlarged

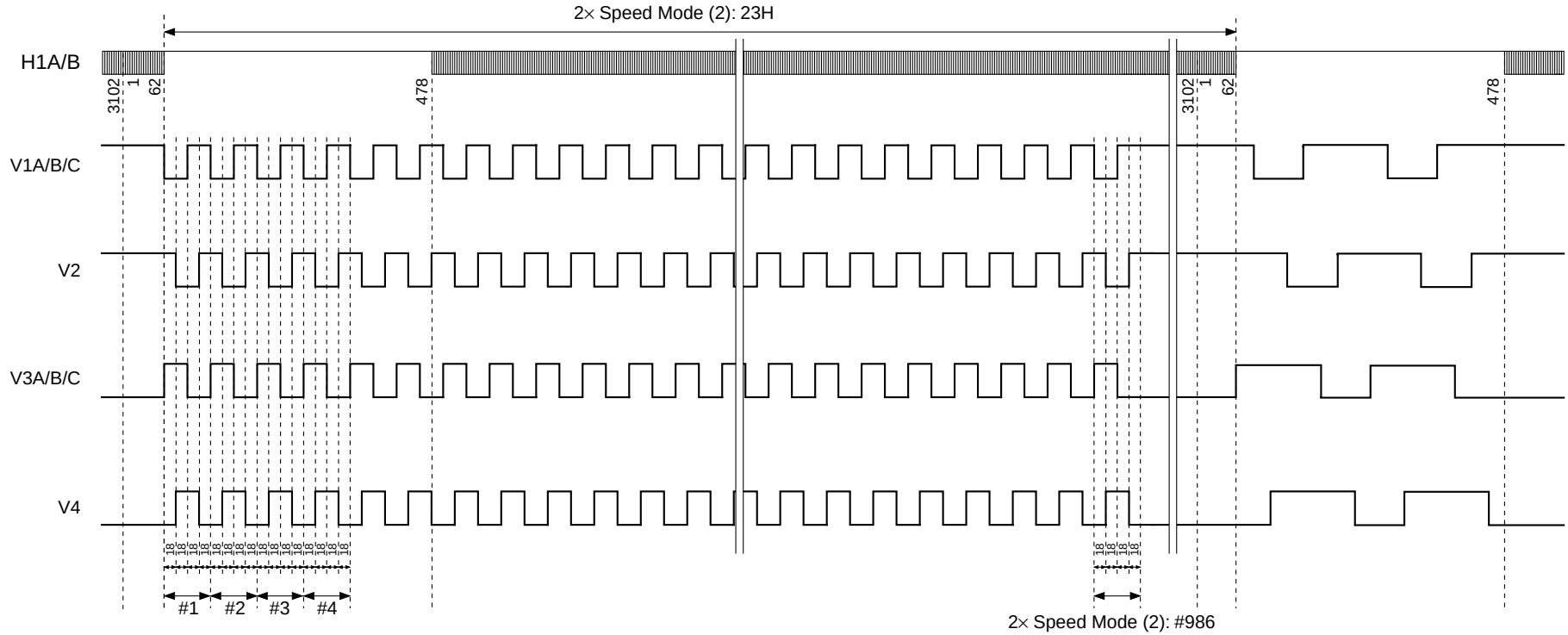
Drive Timing Chart (Vertical Sync) 2x Speed Mode (2) 2-line addition

"h" Enlarged

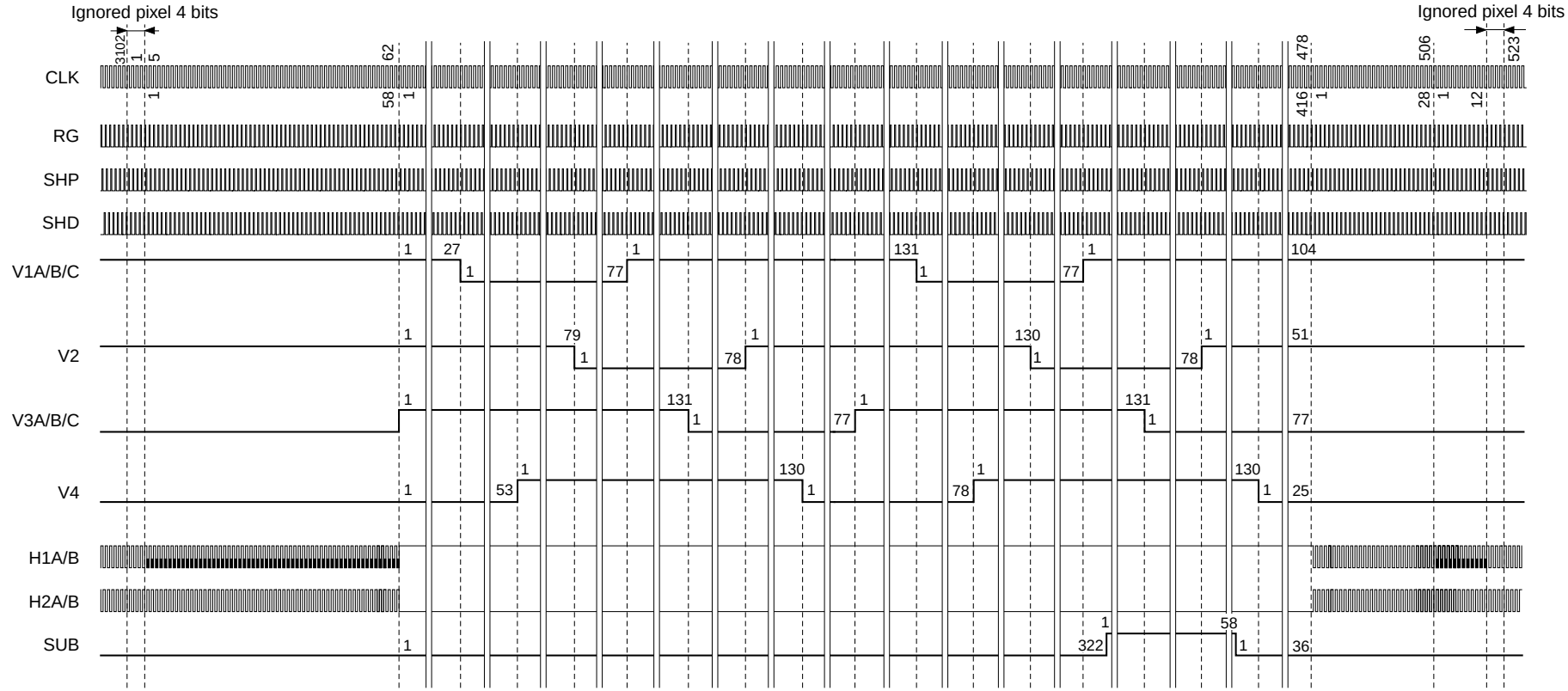


Drive Timing Chart (Vertical Sync) 2× Speed Mode (2) 2-line addition

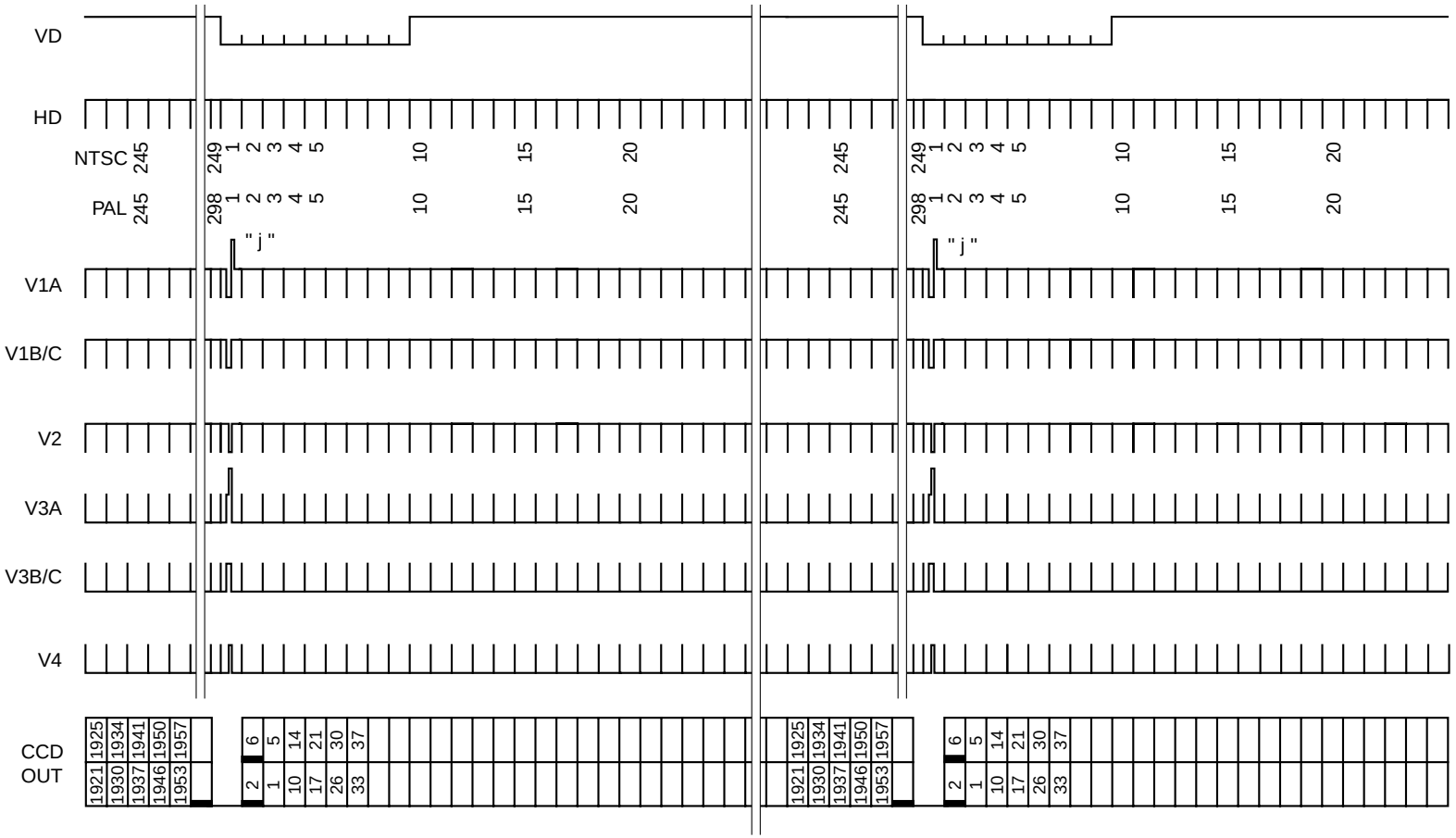
" i " Enlarged



Drive Timing Chart (Horizontal Sync) 2× Speed Mode (2) 2-line addition



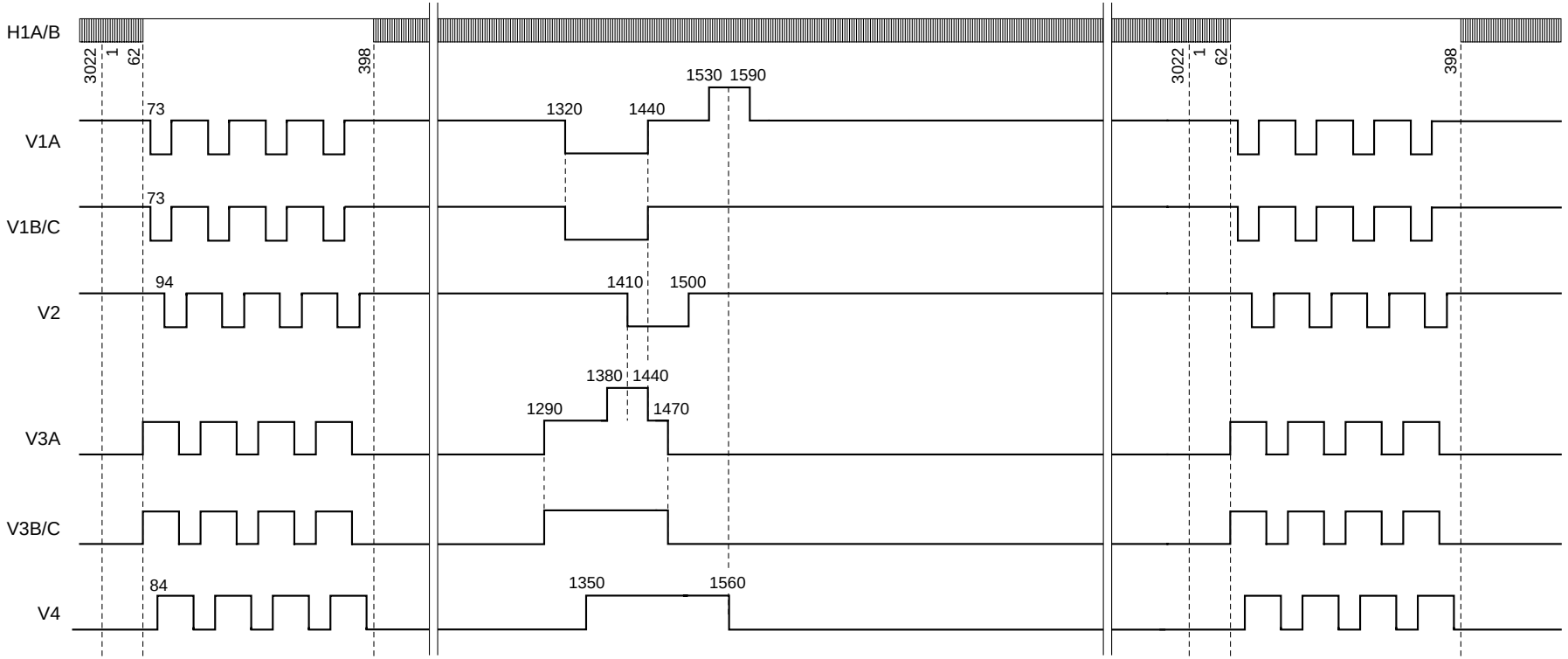
Drive Timing Chart (Vertical Sync) NTSC/PAL 8× Speed Mode



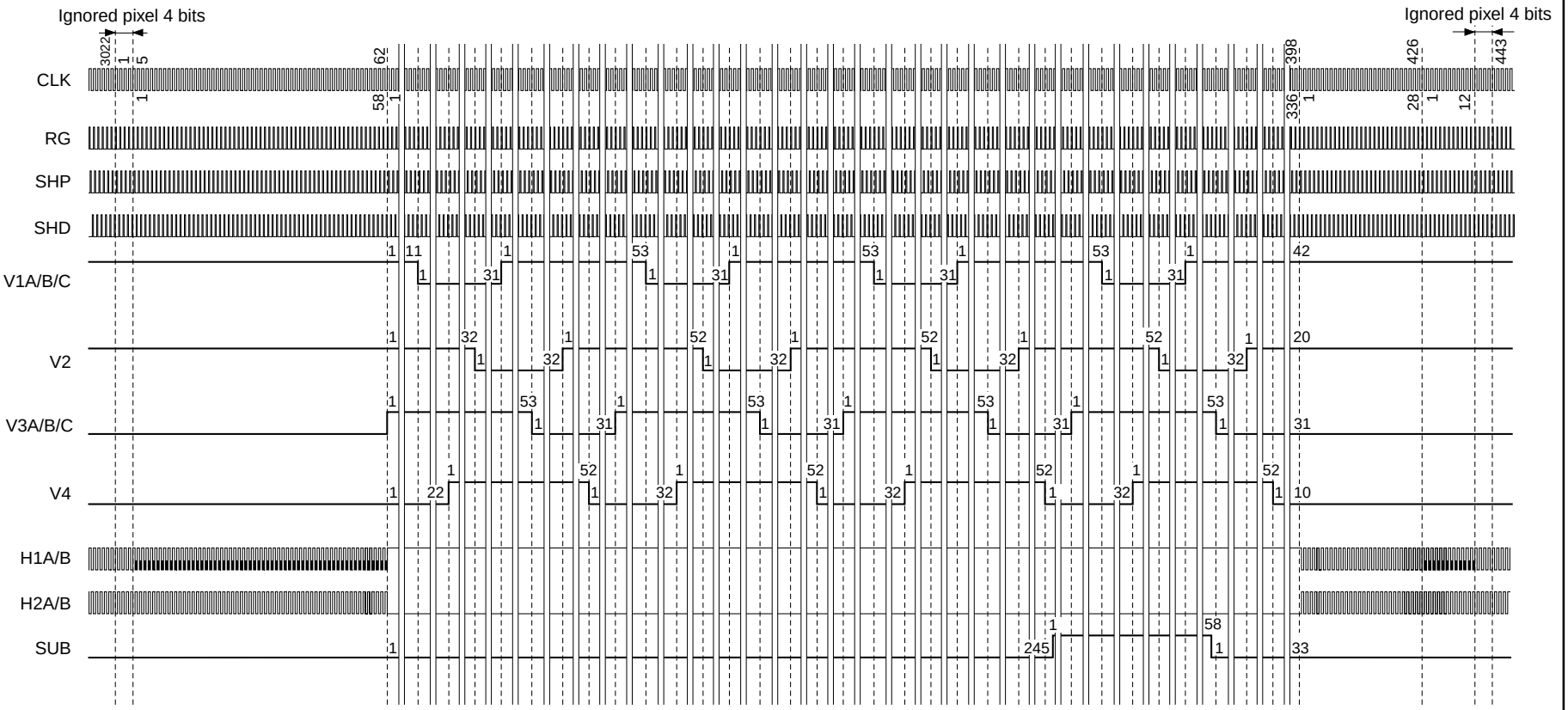
* 3022fH. However, 249H in NTSC mode is 1294 clk, and 298H in PAL mode is 2466 clk.

Drive Timing Chart (Vertical Sync) **8× Speed Mode**
AF Mode (1)
AF Mode (2)

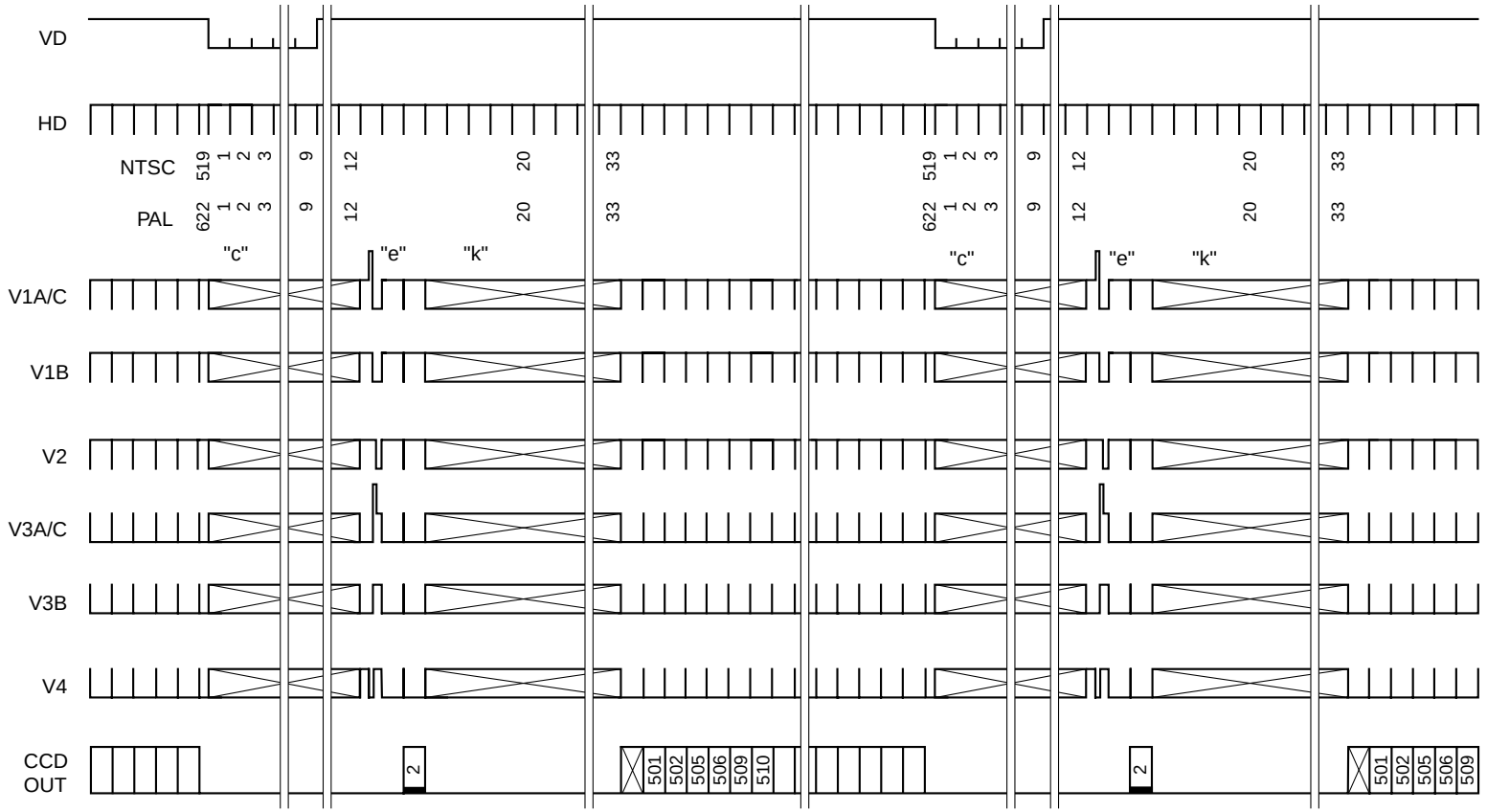
" j " Enlarged



Drive Timing Chart (Horizontal Sync) 8× Speed Mode
AF Mode (1)
AF Mode (2)



Drive Timing Chart (Vertical Sync) NTSC/PAL Center Scan Mode (1) 484-line output (in NTSC mode)

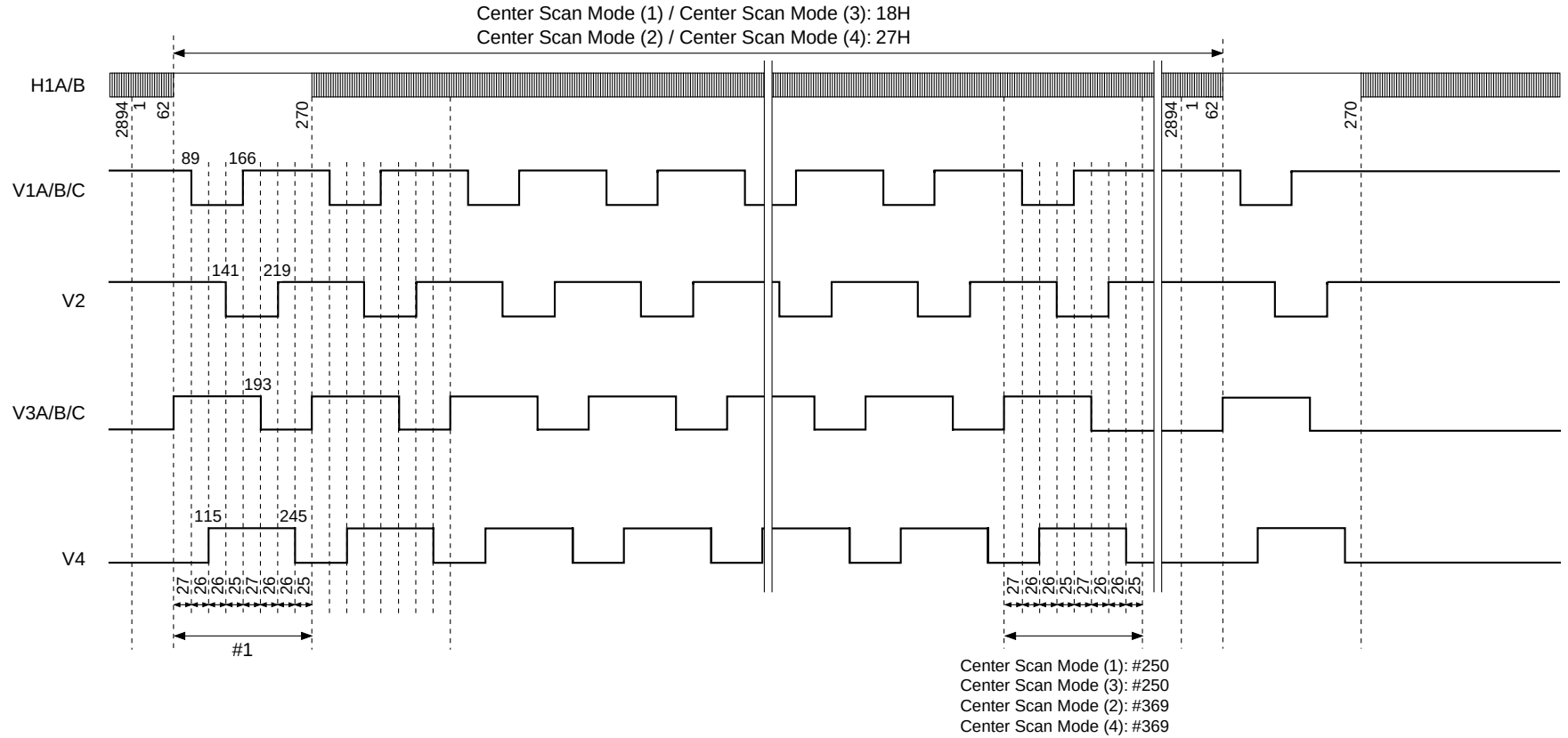


* 2894fH. However, 519H in NTSC mode is 2408 clk, and 622H in PAL mode is 2826 clk.

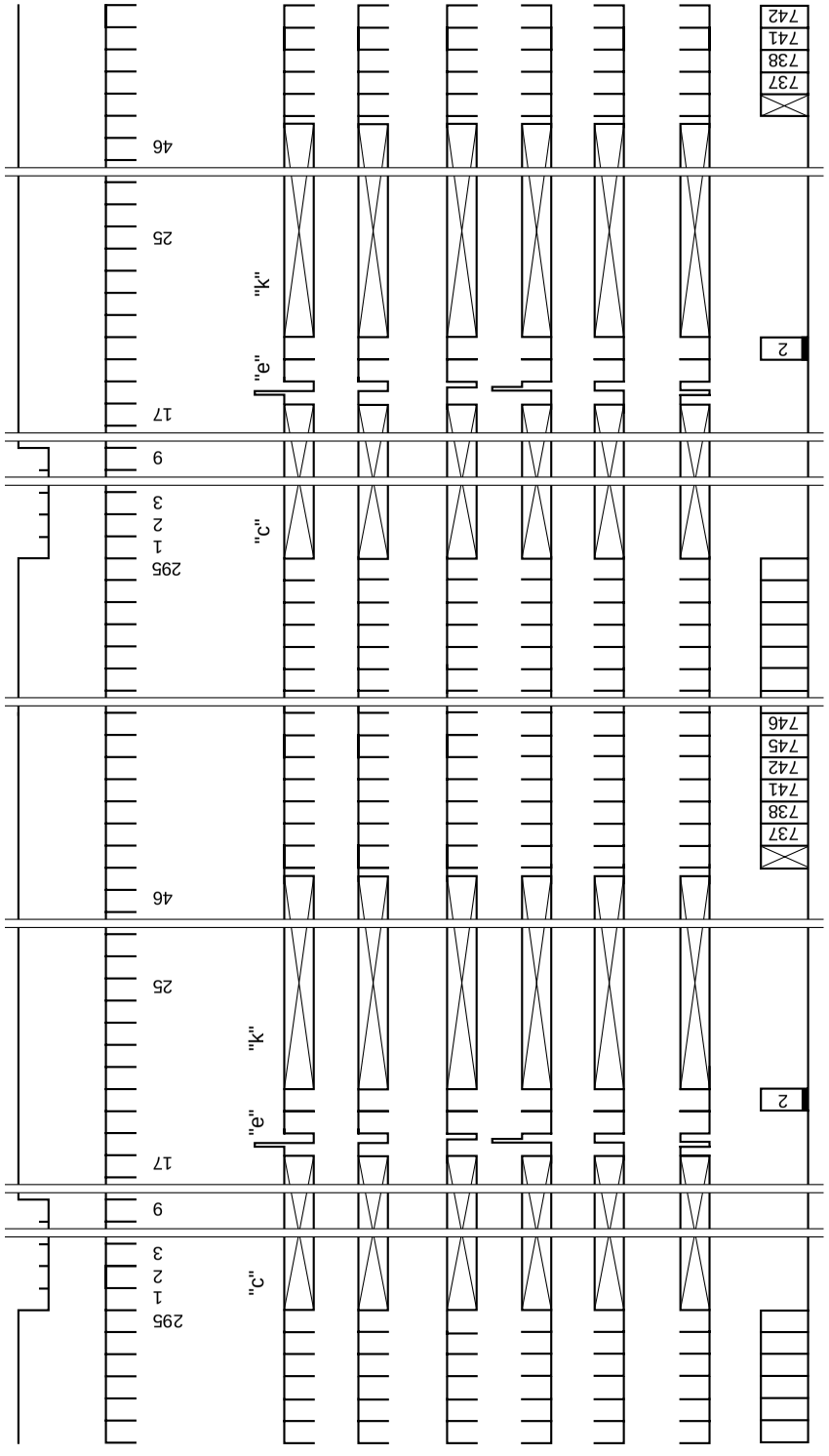
Drive Timing Chart (Vertical Sync)

Center Scan Mode (1) / Center Scan Mode (3)
Center Scan Mode (2) / Center Scan Mode (4)

"k" Enlarged

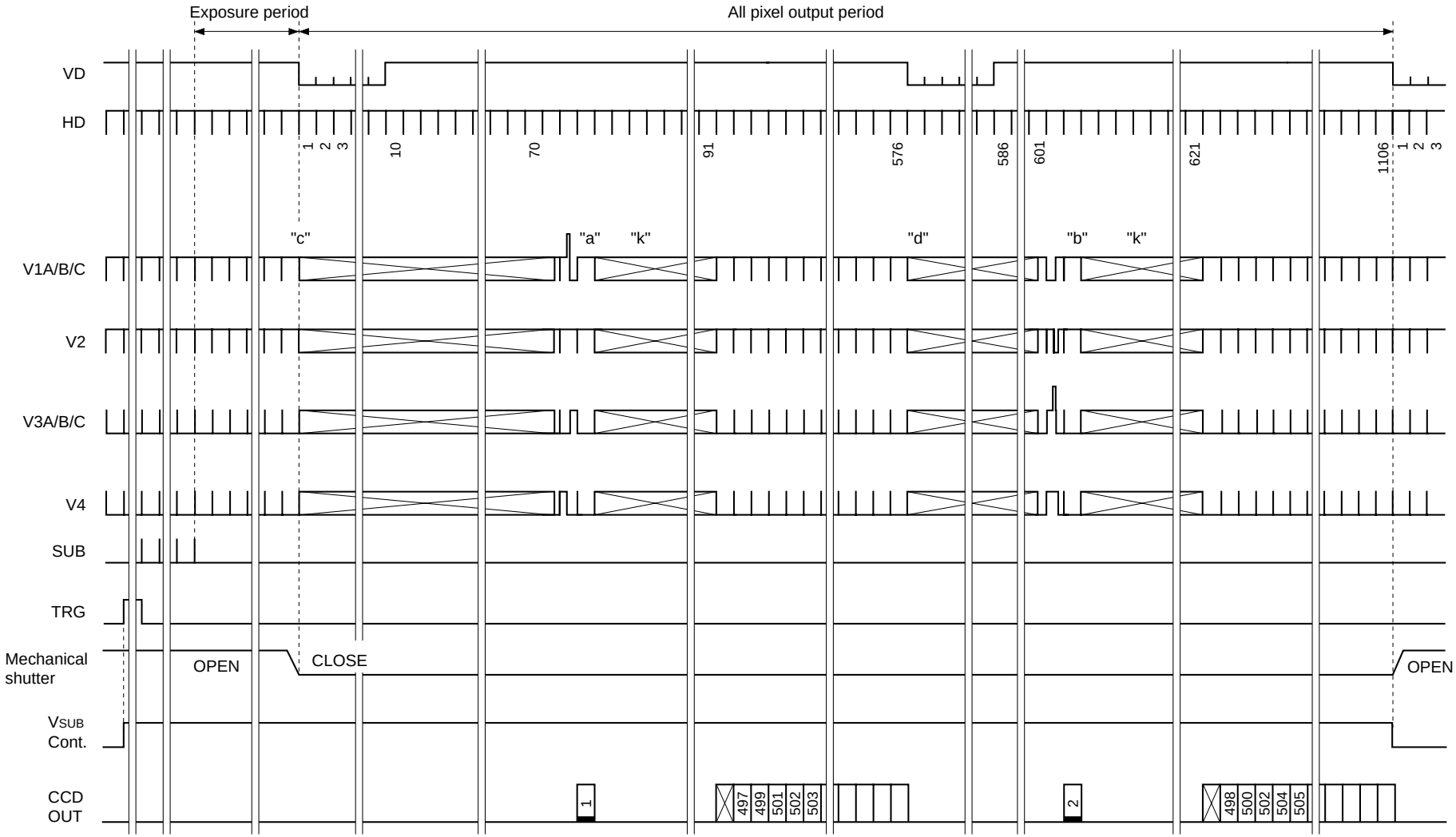


Drive Timing Chart (Vertical Sync) Center Scan Mode (2) 246-line output



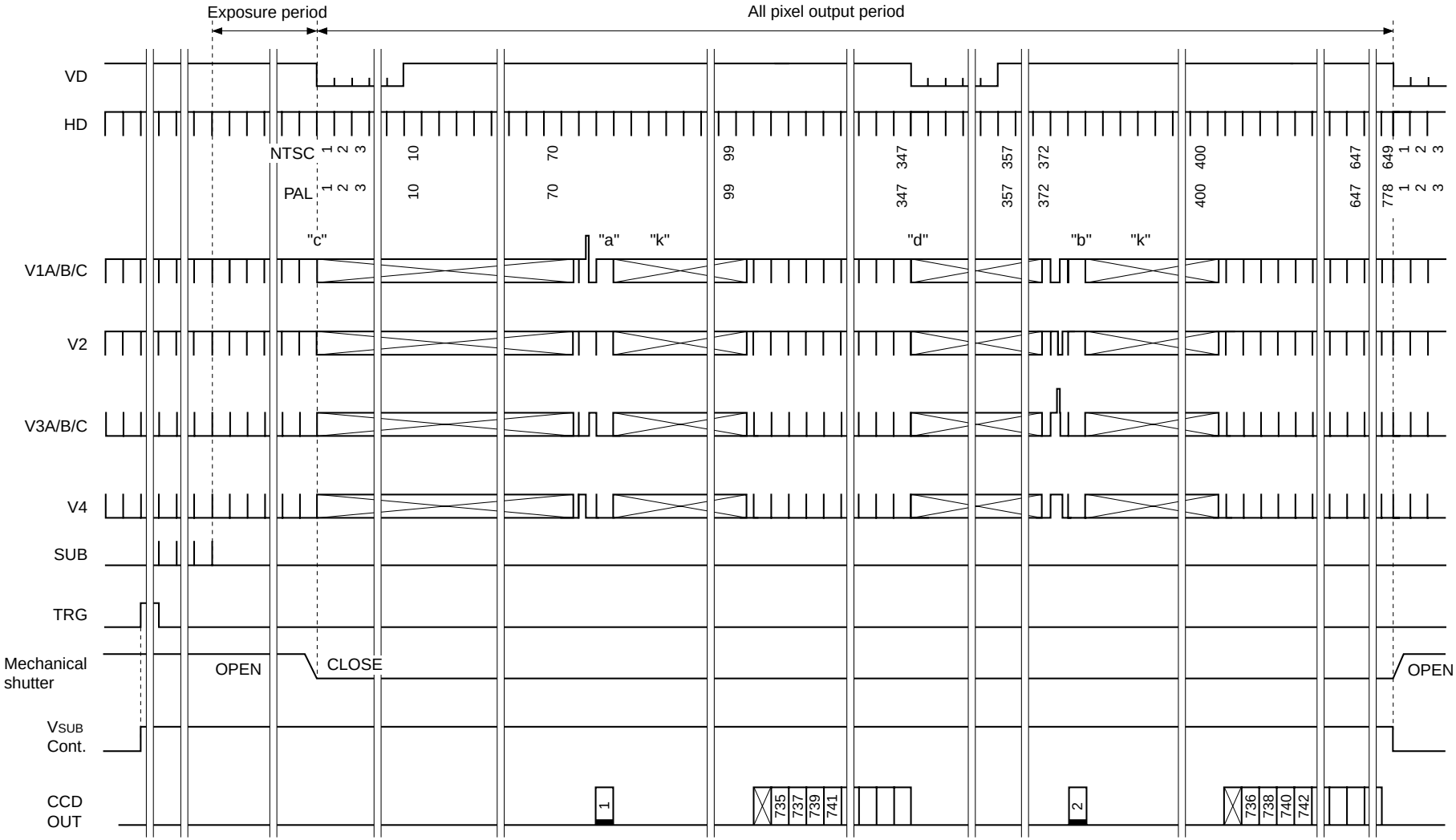
* 2894fH.

Drive Timing Chart (Vertical Sync) Center Scan Mode (3) 968-line output



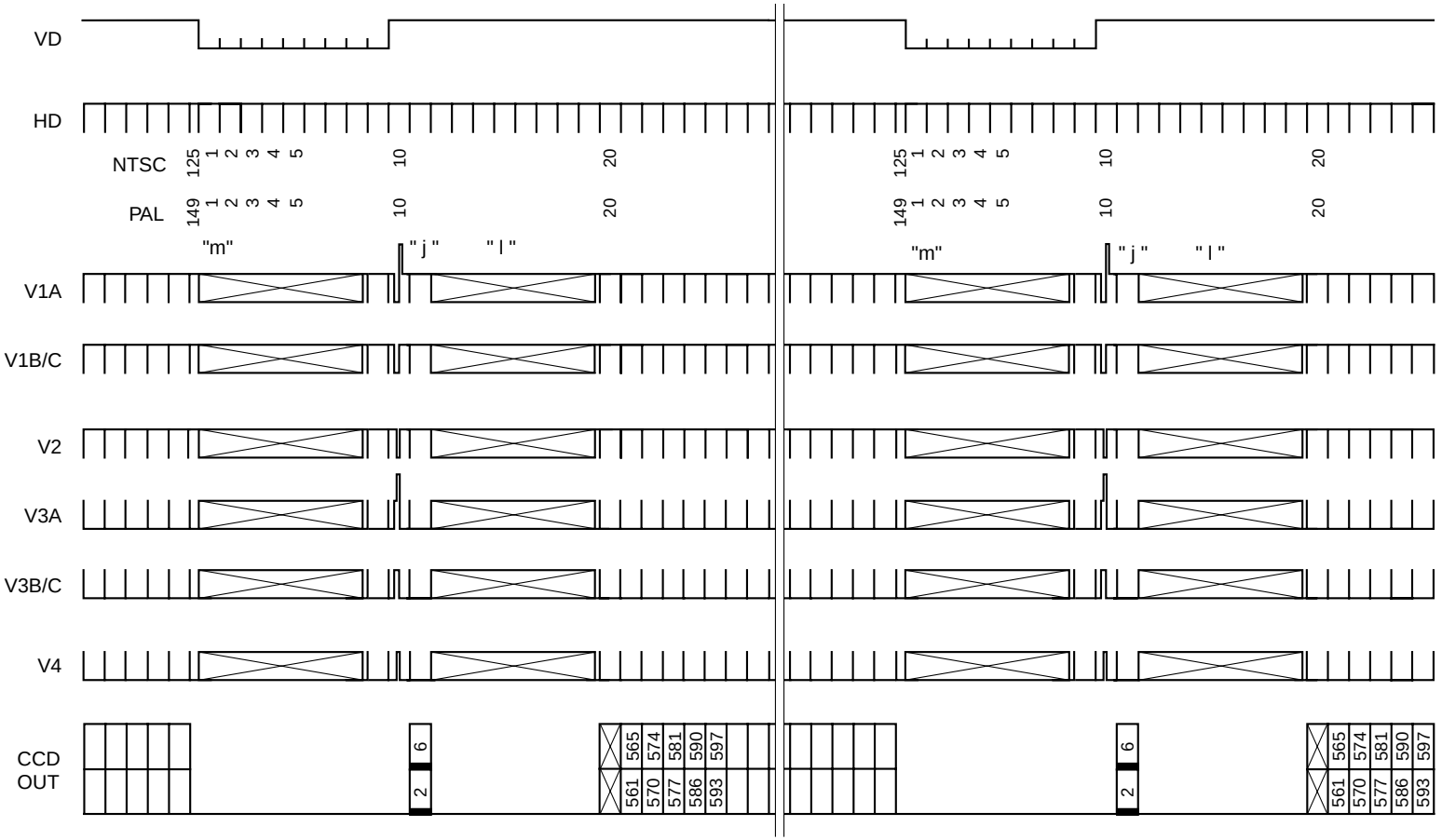
* 2894fH.
Also, the number of high-speed sweep transfer stages and the transfer speed differ for the 1st field and 2nd field sides, so the fields should not be reversed.

Drive Timing Chart (Vertical Sync) NTSC/PAL Center Scan Mode (4) 492-line output (in NTSC mode)



* 2894fH. However, 649H in NTSC mode is 1563 clk, and 778H in PAL mode is 1362 clk.
Also, the number of high-speed sweep transfer stages and the transfer speed differ for the 1st field and 2nd field sides, so the fields should not be reversed.

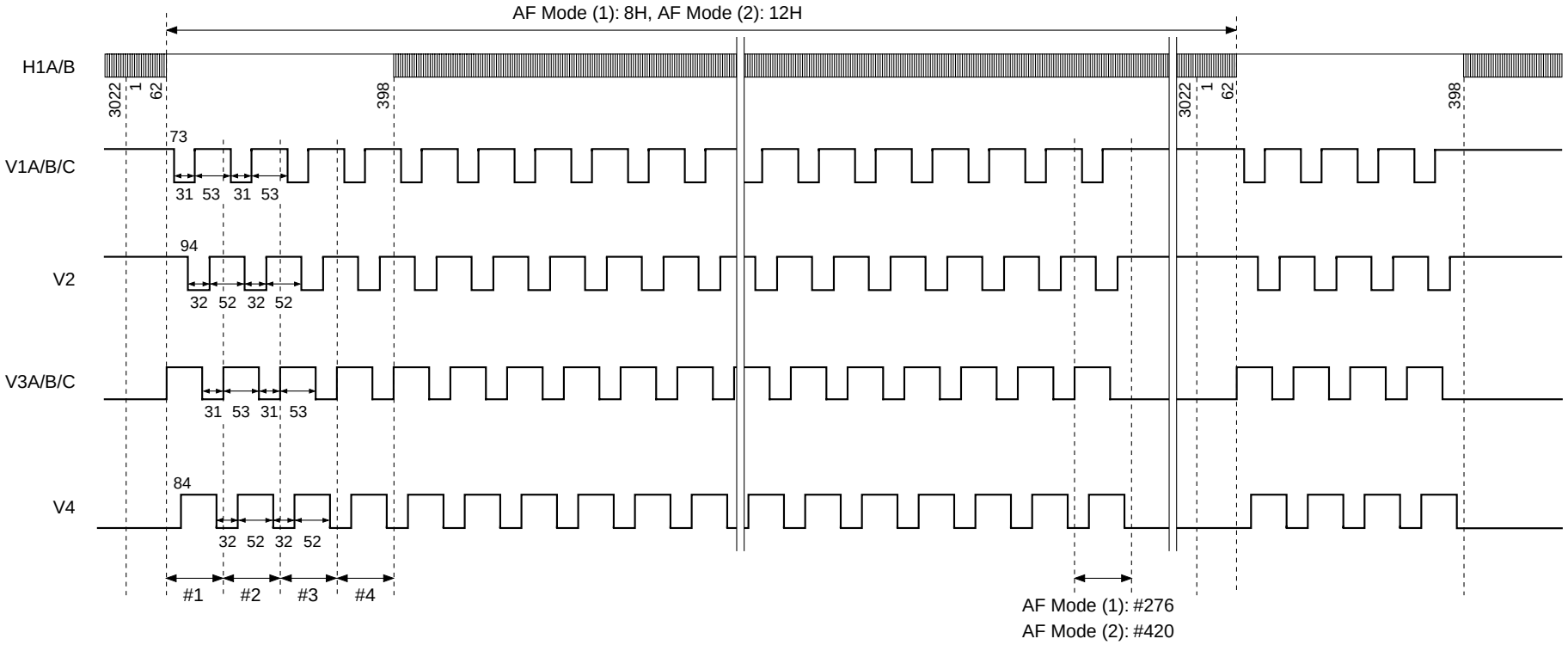
Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (1)



* 3022fH. However, 125H in NTSC mode is 647 clk, and 149H in PAL mode is 2744 clk.

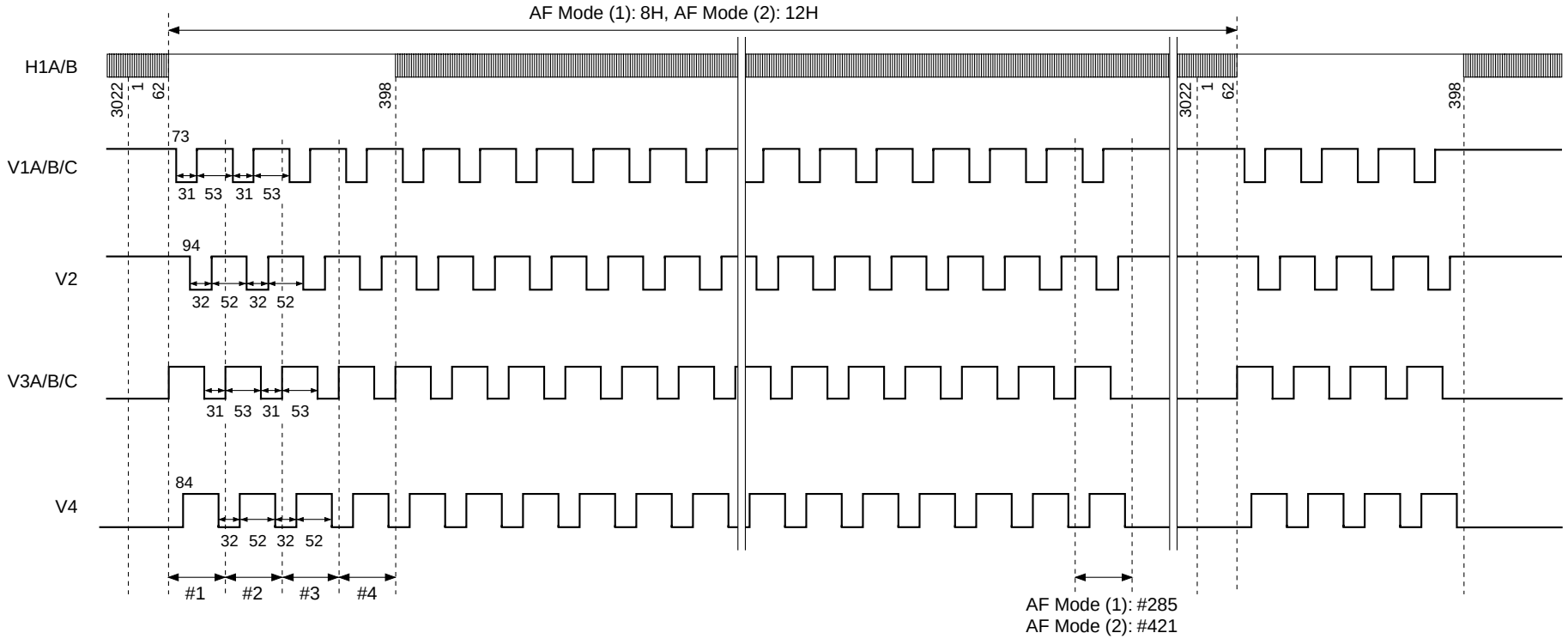
Drive Timing Chart (Vertical Sync) **AF Mode (1)**
AF Mode (2)

" I " Enlarged

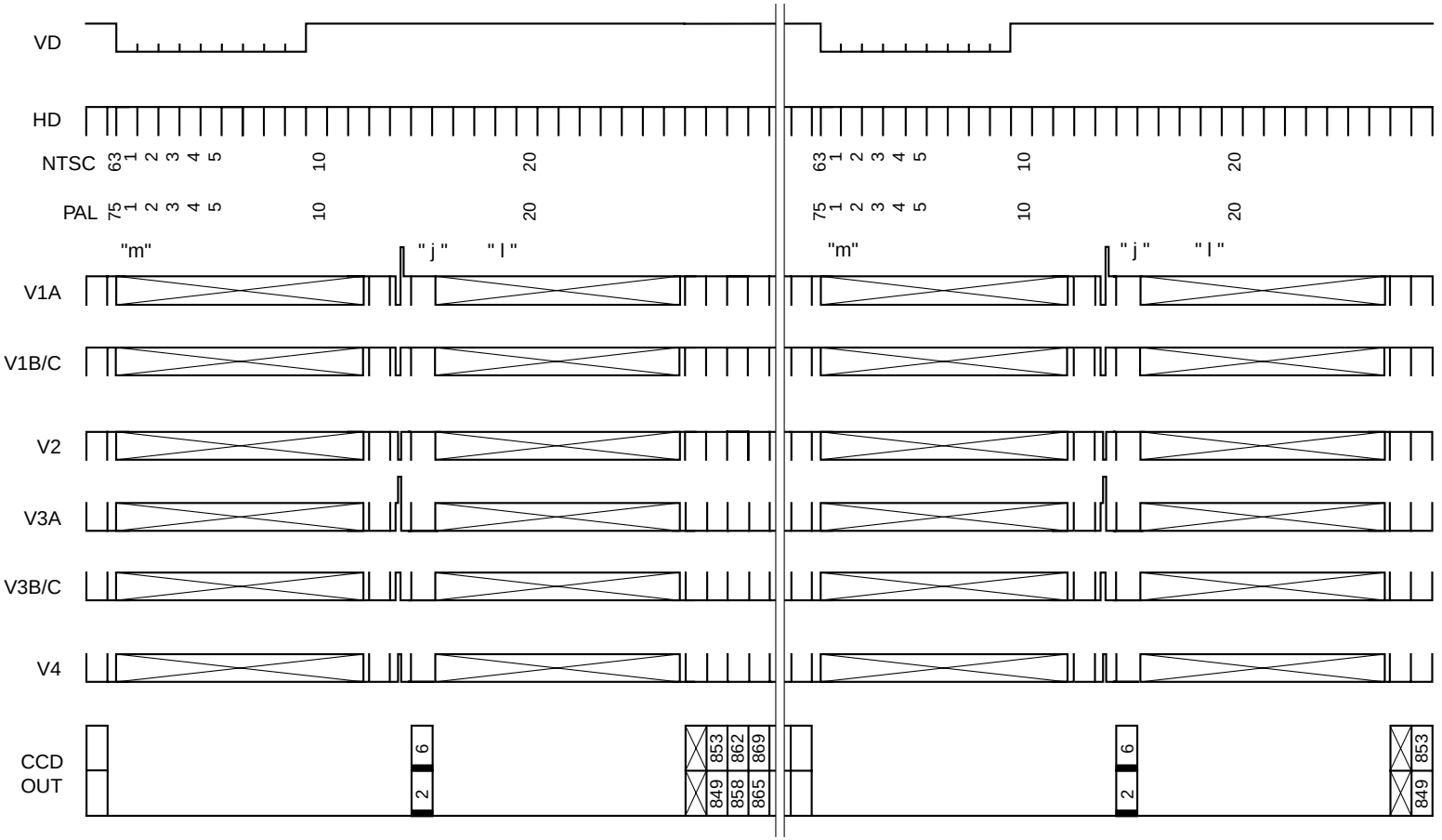


Drive Timing Chart (Vertical Sync) **AF Mode (1)**
AF Mode (2)

"m" Enlarged



Drive Timing Chart (Vertical Sync) NTSC/PAL AF Mode (2)



* 3022fH. However, 63H in NTSC mode is 324 clk, and 75H in PAL mode is 1372 clk.

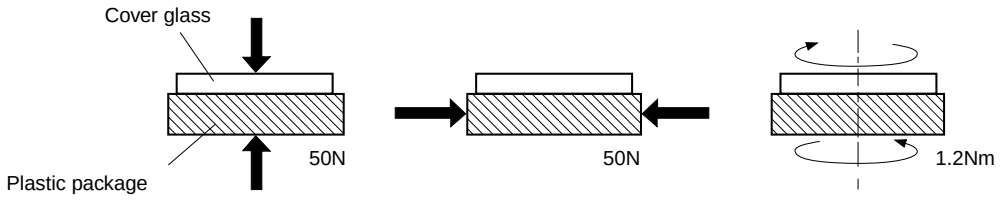
Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
   a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

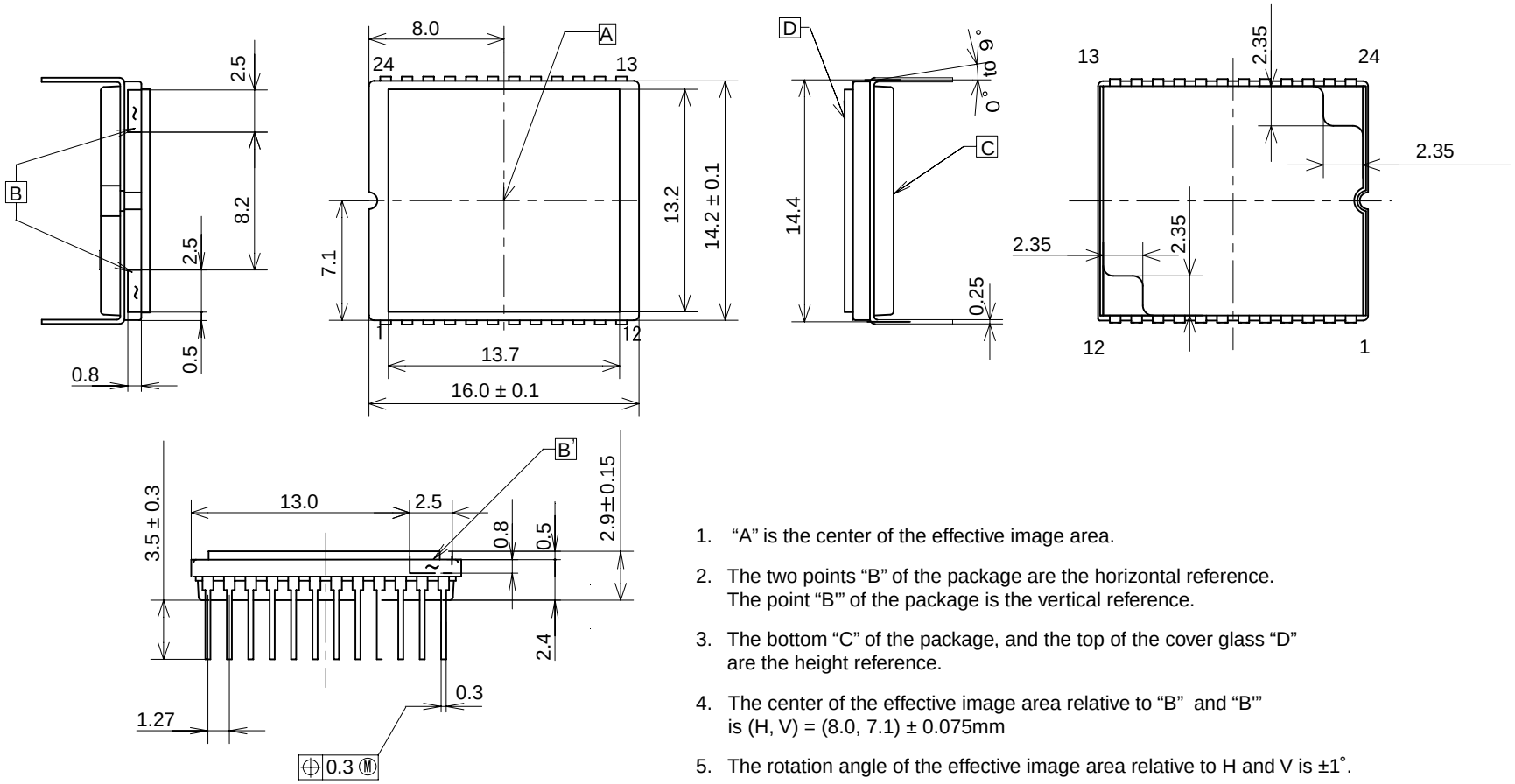
   b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others
a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline Unit: mm

24 pin DIP



PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.23g
DRAWING NUMBER	AS-A9-02(E)

1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference. The point "B'" of the package is the vertical reference.
3. The bottom "C" of the package, and the top of the cover glass "D" are the height reference.
4. The center of the effective image area relative to "B" and "B'" is (H, V) = (8.0, 7.1) ± 0.075mm
5. The rotation angle of the effective image area relative to H and V is ±1°.
6. The height from the bottom "C" to the effective image area is 1.41 ± 0.10mm. The height from the top of the cover glass "D" to the effective image area is 1.49 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom "C" is less than 50µm. The tilt of the effective image area relative to the top "D" of the cover glass is less than 50µm
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.