PRELIMINARY

MX8350

2 in 1 RAMBUS CLOCK GENERATOR

FEATURES

- Clock generator for Rambus™ Channel
- Provide output frequency select pin
- Provide a Rambus™ interface level output frequency which is 17 times of input frequency
- Provide a TTL interface level output frequency which is one fourth of input frequency
- Provide a TTL interface level output frequency which is 14/5 or 17/5 times of input frequency
- Provide a chip reset pin ($\overline{\text{RESET}}$) for external control
- 3.3 V power supply
- Package 14-pin SOP

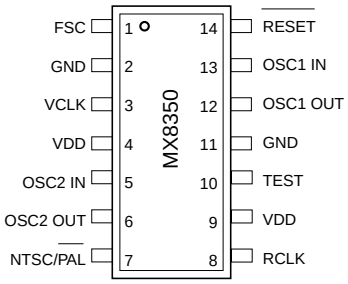
GENERAL DESCRIPTION

The product is a clock synthesizer chip for Rambus™ channel. It uses advanced phase lock loop technology to generate three desired clock. The reference clocks are supplied by two external crystals. (X'tal1 and X'tal2) The X'tal1 frequency is 14.31818MHz in NTSC case, 17.734475MHz in PAL case and 14.302446MHz in MPAL case. With X'tal1 input frequency, the TTL-interface-level output clock set (VCLK and FSC) is (48.681812MHz, 3.579545MHz), (49.65653MHz, 4.433619MHz) and (48.628318MHz, 3.5756115MHz) in the three cases respectively. The Rambus™-interface-level clock (RCLK) is 250MHz which is 17 times of the X'tal2 frequency. i.e.14.705882MHz.

The product is 3.3 V operation, and the package type is 14-pin SOP.

PIN CONFIGURATIONS

14-PIN SOP



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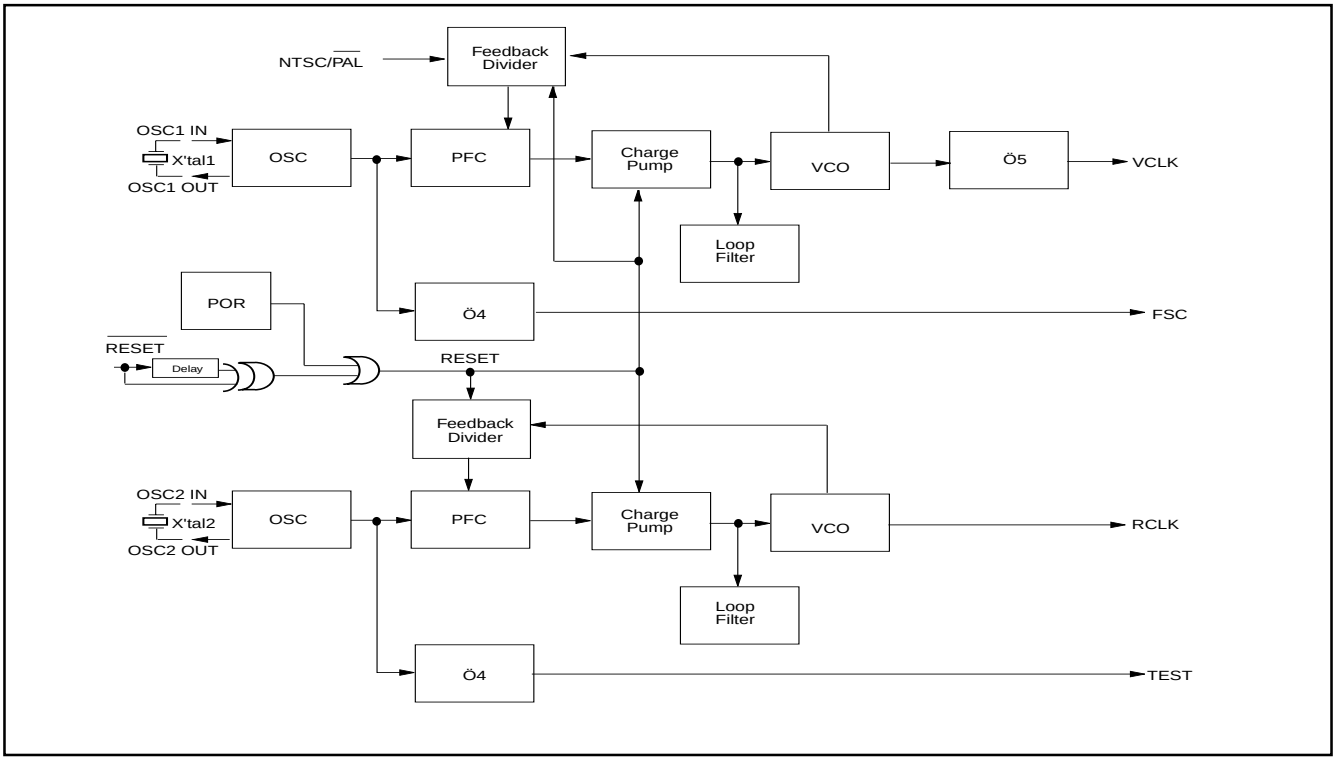
PIN DESCRIPTION

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
FSC	O	1	Clock output. 1/4 of OSC1 frequency.
GND	-	2	Circuit ground
VCLK	O	3	Video data transfer clock output.
VDD	-	4	+3.3V power supply.
OSC2 IN	I	5	OSC2 (14.705882MHz) crystal pin.
OSC2 OUT	O	6	OSC2 (14.705882MHz) crystal pin.
NTSC/$\overline{\text{PAL}}$	I	7	OSC1 frequency select pin. High; VCLK=17/5 times of input frequency. Low; VCLK=14/5 times of input frequency.
RCLK	O	8	Rambus clock output.
VDD	-	9	+3.3V power supply.
TEST	O	10	OSC2 test pin. 1/4 of OSC2 frequency.
GND	-	11	Circuit ground.
OSC1 OUT	O	12	OSC1 crystal pin.
OSC1 IN	I	13	OSC1 (NTSC; 14.31818MHz, PAL; 17.734475MHz, MPAL; 14.302446MHz) crystal pin.
$\overline{\text{RESET}}$	I	14	System reset input. Reset the chip when any transition edge is tetected.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The Rambus clock generator is an integrated circuit of phase locked loop frequency synthesizer. It provides three clock output frequencies. The first clock output (FSC) is the crystal 1 frequency divided by 4 clock. The second clock output frequency (VCLK) is 14/5 or 17/5 times of crystal1 frequency. It can be selected by NTSC/$\overline{\text{PAL}}$ pin. When NTSC/$\overline{\text{PAL}}$ pin is high, VCLK is 17/5 times of crystal 1 frequency. When NTSC/$\overline{\text{PAL}}$ pin is low, VCLK is 14/5 times of crystal 1 frequency. FSC and VCLK are TTL-interface-level outputs. The third clock output (RCLK) which is 17 times of crystal2 frequency is Rambus-interface-level signal.

As shown in the block diagram, two phase locked loops which consist of feedback divider, phase frequency comparator (PFC), charge pump, voltage controlled oscillator (VCO) and loop filter are used. All components for PLL are integrated inside the chip.

FREQUENCY TABLE(in MHz)

	CRYSTAL 1	NTSC/$\overline{\text{PAL}}$	VCLK	FSC
NTSC	14.31818	H	48.681812	3.579545
PAL	17.734475	L	49.65653	4.433619
MPAL	14.302446	H	48.628318	3.575612

CRYSTAL2	RCLK
14.705882	250

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Storage Temperature	-55°C to 150°C
Applied Input Voltage	-0.5V to VDD + 0.5V
Applied Output Voltage	-0.5V to VDD + 0.5V
Supply Voltage	-0.5V to 5V
Operating Temperature	0 to 70°C
Power Dissipation	0.5Watts

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VDD = 3.15V to 3.6V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VIL	Input Low Voltage			0.8	V	
VIH	Input High Voltage	2.4			V	
IIL	Input Low Current			-5	uA	
IIH	Input High Current			5	uA	
IVDD	VDD Current		TBD		mA	
VOL	Output Low Voltage			0.4	V	IOL=8mA, VCLK output
VOH	Output High Voltage	2.4			V	IOH=-4mA, VCLK output
CI	Input Capacitance			10	pF	
RL	Line Impedence	20	50	75	Ohm	Rambus Level
VLT	Line Termination Voltage	2.2		2.7	V	Rambus Level
IOH	Output High Current	-10		10	uA	RCLK output
IOL	Output Low Current	40	50	75	mA	VOL=0.4V, RCLK output
Ro	Output Resistance	5.3	8	10	Ohm	RCLK output
Ro (PMOS)	Output Resistance		TBD		Ohm	IOH=-600uA, FSC output
Ro (NMOS)	Output Resistance		TBD		Ohm	IOL=600uA, FSC output

AC CHARACTERISTICS TA = 0°C to 80°C, VDD = 3.15V to 3.6V

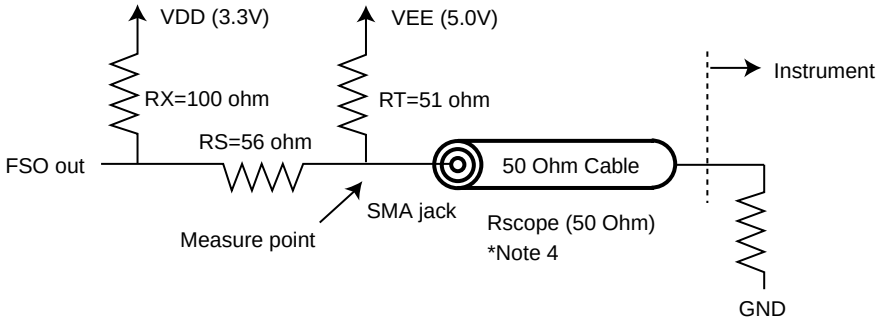
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Dt_1	Duty Cycle	45		55	%	RCLK, FSC *Note 1
Dt_2	Duty Cycle	55	60	65	%	VCLK *Note 2
J	Jitter,short term			150	ps	*Note 1
Tr/Tf	Rise/Fall Time	0.3		0.7	ns	Rambus level, RCLK output *Note 1
Tr/Tf	Rise/Fall Time	2	3.5	5	ns	VCLK output, 30pF load *Note 2
Tup	Power up Time		1	5	ms	1. After power is stable 2.Frequency from 0 to 250MHz *Note3

*Note 1: We measured FSC output with 20pF load to GND. Considering with probe loading, the total loading on FSC is 28pF. The test fixture to measure RCLK output is shown as Fig. 1. The measured duty cycle, jitter and Rise/Fall time are based on the test fixture. The reference voltage as measureing duty cycle is 50%. Short tern jitter means jitter measured at 11th rising edge after trigger point. Rise/Fall time is measured from 20% to 80%.

*Note 2: VCLK output is measured with 22pF external capacitance loading. Considering with probe loading, the total loading on VCLK is 30pF.
The reference voltage to measure duty cycle of VCLK is VDD/2. Rise/Fall time is measured from 20% to 80%.

*Note 3: It's guaranteed by design.

APPENDIX



*Note 4: Rscope is the internal equivalent resistance of instrument.

Fig. 1

ORDERING INFORMATION

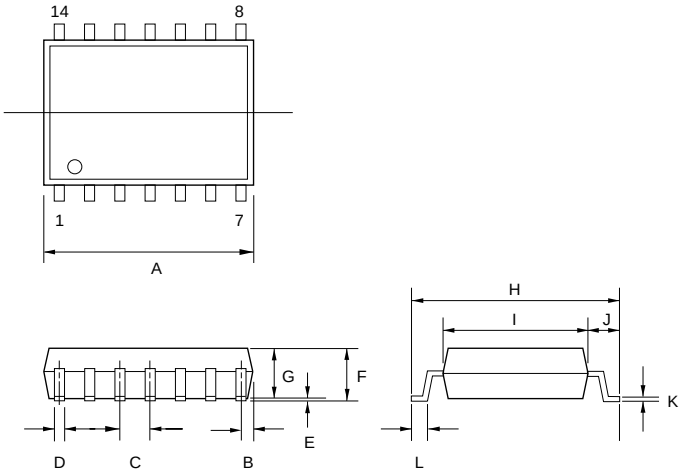
PART NO.	PACKAGE
MX8350	14-PIN SOP

PACKAGE INFORMATION

14-PIN PLASTIC SOP (150 mil)

ITEM	MILLIMETER	INCHES
A	8.66 MAX.	.341 MAX.
B	.53 [REF]	.021 [REF]
C	1.27 [TP]	.050 [TP]
D	.41 [TYP.]	.016 [TYP.]
E	.10 MIN.	.004 MIN.
F	1.73 MAX.	.068 MAX.
G	1.45 ± .13	.057 ± .005
H	5.99 ± .25	.236 ± .010
I	3.91 ± .13	.154 ± .005
J	1.04	.041
K	.20 [TYP.]	.008 [TYP.]
L	.67	.026

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

Revision	Description	Date
1.1	P 4: Add Note 1-3 P 5: Add Apendix	JUL. 23, 1998

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