

OKI Semiconductor

MSM63188A

4-Bit Microcontroller with Built-in 1024-Dot Matrix LCD Drivers and Melody Circuit, Operating at 0.9 V (Min.)

GENERAL DESCRIPTION

The MSM63188A is an enhanced version of the MSM63188 in which supply currents have been improved.

The MSM63188A is a CMOS 4-bit microcontroller with built-in 1024-dot matrix LCD drivers and operates at 0.9 V (min.). The MSM63188A is suitable for applications such as games, toys, watches, etc. which are provided with an LCD display.

The MSM63188A is an M6318x series mask ROM-version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.

The MSM63P180 is the one-time-programmable ROM version of MSM63188/A, having one-time PROM (OTP) as internal program memory.

The MSM63P180 is used to evaluate the software development.

FEATURES

- Rich instruction set
 - 439 instructions
 - Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, branch, conditional branch, call/return, control.
- Rich selection of addressing modes
 - Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
 - Data memory bank internal direct addressing mode.
- Processing speed
 - Two clocks per machine cycle, with most instructions executed in one machine cycle.
 - Minimum instruction execution time : 61 μ s (@ 32.768 kHz system clock)
 - 1 μ s (@ 2 MHz system clock)
- Clock generation circuit
 - Low-speed clock : 32.768 kHz crystal oscillator
 - High-speed clock : 2 MHz (Max.) RC or ceramic oscillator select
- Program memory space
 - 16K words
 - Basic instruction length is 16 bits/1 word
- Data memory space
 - 3584 nibbles
- External data memory space
 - 64 Kbytes (expandable by using an I/O port)

- Stack level
 - Call stack level : 16 levels
 - Register stack level : 16 levels
- I/O ports
 - Input ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
 - Output ports: Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
 - Input-output ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
 - Can be interfaced with external peripherals that use a different power supply than this device uses.
 - Number of ports:
 - Input port : 2 ports × 4 bits
 - Output port : 6 ports × 4 bits
 - Input-output port : 6 ports × 4 bits
- Melody output function
 - Melody sound frequency : 529 to 2979 Hz
 - Tone length : 63 types
 - Tempo : 15 types
 - Note data : Resides in the program memory
 - Buzzer drive signal output : 4 kHz
- LCD driver
 - Number of segments : 1024 Max. (64 SEG × 16 COM)
 - 1/1 to 1/16 duty
 - 1/4 or 1/5 bias (regulator built-in)
 - Selectable as all-on mode/all-off mode/power down mode/normal display mode
 - Adjustable contrast
- Multiplier/divider circuits
 - Multiplier : (8 bits) × (8 bits) → Product (16 bits)
 - Divider : (16 bits) ÷ (8 bits) → Quotient (16 bits), Remainder (8 bits)
- Reset function
 - Reset through RESET pin
 - Power-on reset
 - Reset by low-speed oscillation halt
- Battery check
 - Low-voltage supply check
 - Criterion voltage : Can be selected as 1.05 ±0.10 V, 1.30 ±0.15 V, 2.20 ±0.20 V or 2.80 ±0.30 V
- Power supply backup
 - Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

- Timers and counter
 - 8-bit timer × 4
 Selectable as auto-reload mode/capture mode/clock frequency measurement mode
 - Watchdog timer × 1
 Overflows in 2 sec.
 - 100 Hz timer × 1
 Measurable in steps of 1/100 sec.
 - 15-bit time base counter × 1
 1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read

- Serial port
 - Mode : UART mode, synchronous mode
 - UART communication speed : 1200 bps, 2400 bps, 4800 bps, 9600 bps
 - Clock frequency in synchronous mode : 32.768 kHz (internal clock mode), external clock frequency
 - Data length : 5 to 8 bits

- Interrupt sources
 - External interrupt : 4
 - Internal interrupt : 13 (watchdog timer interrupt is a nonmaskable interrupt)

- Operating voltage
 - When backup used : 0.9 to 2.7 V
 (Low-speed clock operating)
 1.2 to 2.7 V
 (Operating frequency: 300 to 500 kHz)
 1.5 to 2.7 V
 (Operating frequency: 200 kHz to 1 MHz)
 - When backup not used : 1.8 to 5.5 V
 (Operating frequency: 300 to 500 kHz)
 2.2 to 5.5 V
 (Operating frequency: 300 kHz to 1 MHz)
 2.7 to 5.5 V
 (Operating frequency: 200 kHz to 2 MHz)



- Package:
 - 176-pin plastic LQFP (LQFP176-P-2424-0.50-BK) : (Product name: MSM63188A-xxxGS-BK)
 - Chip : (Product name: MSM63188A-xxx)
 xxx indicates a code number.

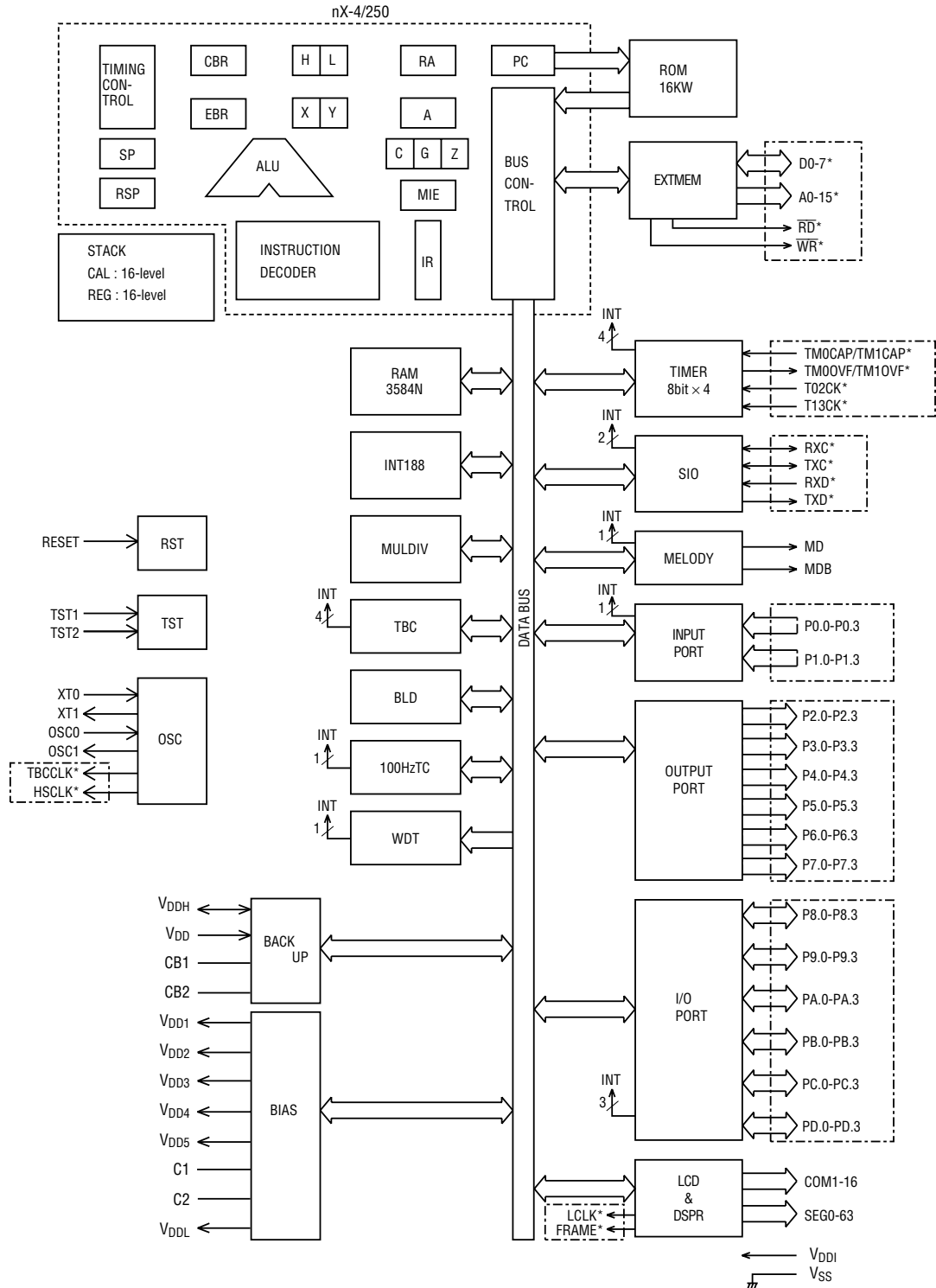
Differences Between the MSM63188 and the MSM63188A

The MSM63188A has the following improved characteristics.

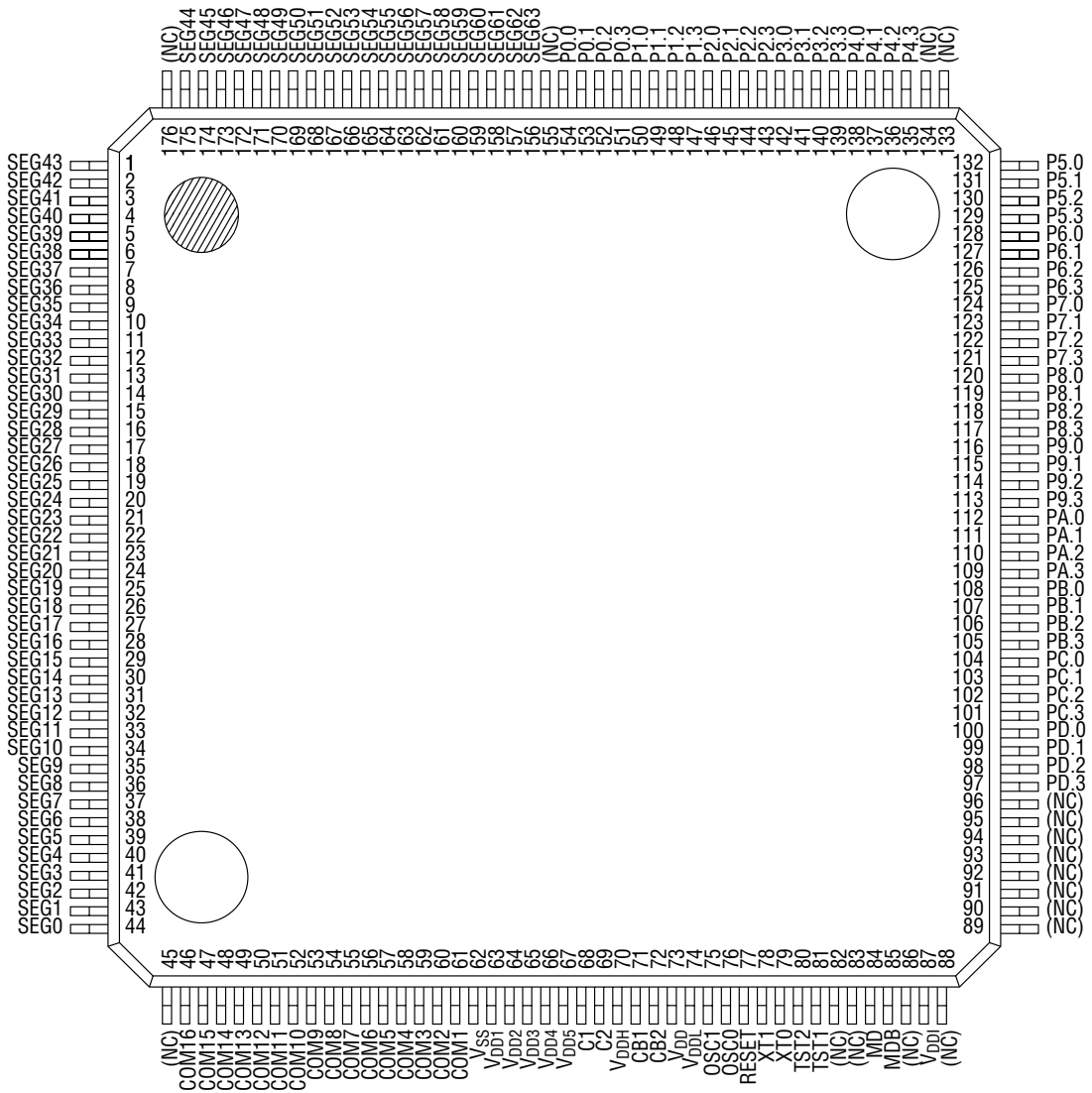
- Supply currents (I_{DD1} , I_{DD2} , I_{DD3}) in DC characteristics
- The V_{DDL} voltage during a halt of high-speed clock oscillation

BLOCK DIAGRAM

An asterisk (*) indicates the port secondary function.  indicates that the power is supplied to the circuits corresponding to the signal names inside  from V_{DDI} (power supply for interface).



PIN CONFIGURATION (TOP VIEW)

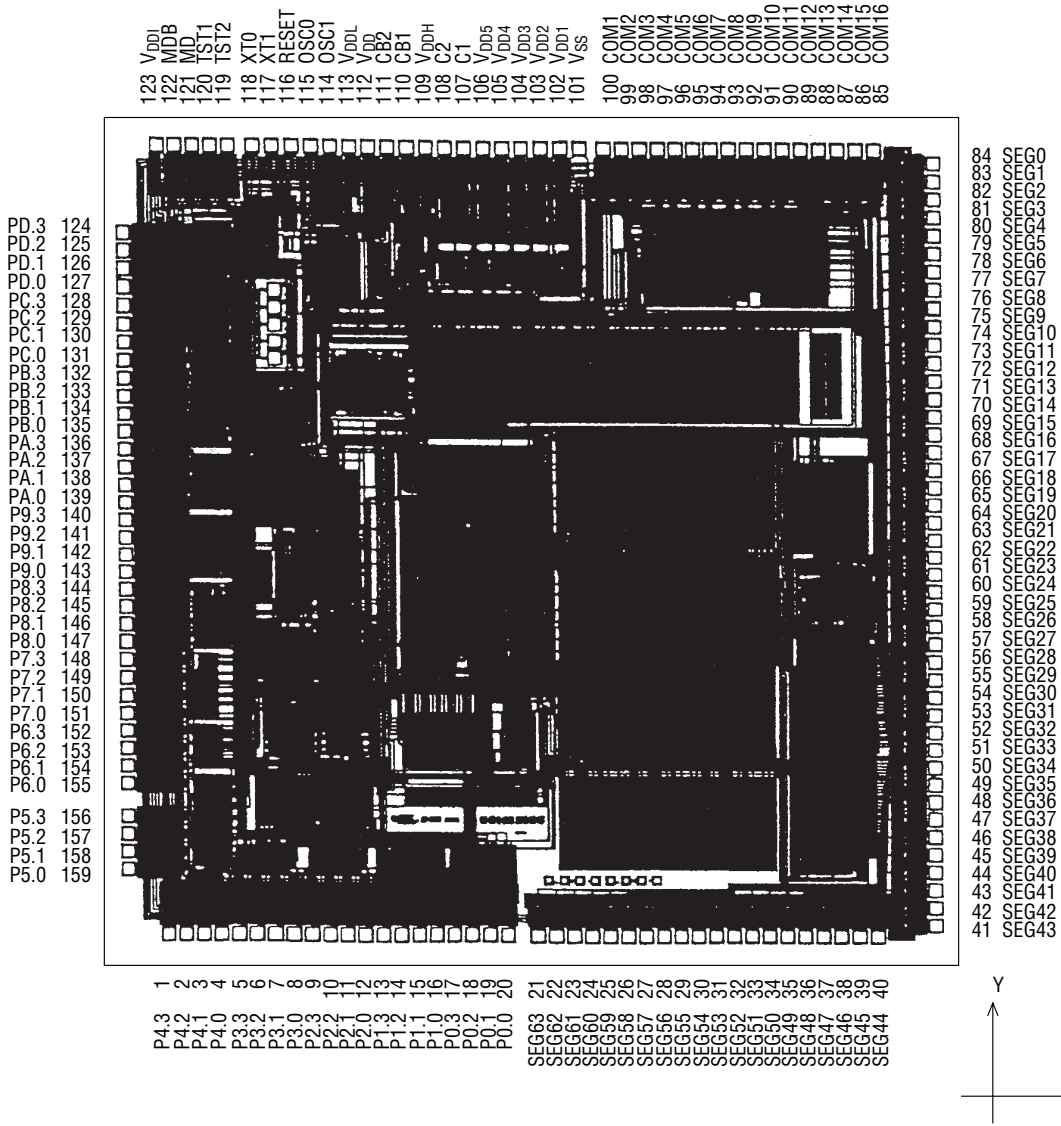


176-Pin Plastic LQFP

Note: Pins marked as (NC) are no-connection pins which are left open.

PAD CONFIGURATION

Pad Layout



Chip Size : 6.60 mm × 6.60 mm
 Chip Thickness : 350 μm (typ.)
 Coordinate Origin : Chip center
 Pad Hole Size : 100 μm × 100 μm
 Pad Size : 110 μm × 110 μm
 Minimum Pad Pitch : 140 μm

Note: The chip substrate voltage is V_{SS}.

Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	P4.3	-2837	-3105	42	SEG42	3155	-2870	83	SEG1	3155	2870
2	P4.2	-2697	-3105	43	SEG41	3155	-2730	84	SEG0	3155	3010
3	P4.1	-2557	-3105	44	SEG40	3155	-2590	85	COM16	2705	3105
4	P4.0	-2417	-3105	45	SEG39	3155	-2450	86	COM15	2565	3105
5	P3.3	-2277	-3105	46	SEG38	3155	-2310	87	COM14	2425	3105
6	P3.2	-2137	-3105	47	SEG37	3155	-2170	88	COM13	2285	3105
7	P3.1	-1997	-3105	48	SEG36	3155	-2030	89	COM12	2145	3105
8	P3.0	-1857	-3105	49	SEG35	3155	-1890	90	COM11	2005	3105
9	P2.3	-1717	-3105	50	SEG34	3155	-1750	91	COM10	1865	3105
10	P2.2	-1577	-3105	51	SEG33	3155	-1610	92	COM9	1725	3105
11	P2.1	-1437	-3105	52	SEG32	3155	-1470	93	COM8	1585	3105
12	P2.0	-1297	-3105	53	SEG31	3155	-1330	94	COM7	1445	3105
13	P1.3	-1157	-3105	54	SEG30	3155	-1190	95	COM6	1305	3105
14	P1.2	-1017	-3105	55	SEG29	3155	-1050	96	COM5	1165	3105
15	P1.1	-877	-3105	56	SEG28	3155	-910	97	COM4	1025	3105
16	P1.0	-737	-3105	57	SEG27	3155	-770	98	COM3	885	3105
17	P0.3	-597	-3105	58	SEG26	3155	-630	99	COM2	745	3105
18	P0.2	-457	-3105	59	SEG25	3155	-490	100	COM1	605	3105
19	P0.1	-317	-3105	60	SEG24	3155	-350	101	V _{SS}	420	3105
20	P0.0	-177	-3105	61	SEG23	3155	-210	102	V _{DD1}	270	3105
21	SEG63	54	-3105	62	SEG22	3155	-70	103	V _{DD2}	120	3105
22	SEG62	194	-3105	63	SEG21	3155	70	104	V _{DD3}	-30	3105
23	SEG61	334	-3105	64	SEG20	3155	210	105	V _{DD4}	-179	3105
24	SEG60	474	-3105	65	SEG19	3155	350	106	V _{DD5}	-329	3105
25	SEG59	614	-3105	66	SEG18	3155	490	107	C1	-479	3105
26	SEG58	754	-3105	67	SEG17	3155	630	108	C2	-629	3105
27	SEG57	894	-3105	68	SEG16	3155	770	109	V _{DDH}	-779	3105
28	SEG56	1034	-3105	69	SEG15	3155	910	110	CB1	-929	3105
29	SEG55	1174	-3105	70	SEG14	3155	1050	111	CB2	-1079	3105
30	SEG54	1314	-3105	71	SEG13	3155	1190	112	V _{DD}	-1229	3105
31	SEG53	1454	-3105	72	SEG12	3155	1330	113	V _{DDL}	-1379	3105
32	SEG52	1594	-3105	73	SEG11	3155	1470	114	OSC1	-1529	3105
33	SEG51	1734	-3105	74	SEG10	3155	1610	115	OSC0	-1679	3105
34	SEG50	1874	-3105	75	SEG9	3155	1750	116	RESET	-1829	3105
35	SEG49	2014	-3105	76	SEG8	3155	1890	117	XT1	-1979	3105
36	SEG48	2154	-3105	77	SEG7	3155	2030	118	XT0	-2129	3105
37	SEG47	2294	-3105	78	SEG6	3155	2170	119	TST2	-2324	3105
38	SEG46	2434	-3105	79	SEG5	3155	2310	120	TST1	-2464	3105
39	SEG45	2574	-3105	80	SEG4	3155	2450	121	MD	-2604	3105
40	SEG44	2714	-3105	81	SEG3	3155	2590	122	MDB	-2744	3105
41	SEG43	3155	-3010	82	SEG2	3155	2730	123	V _{DDI}	-2884	3105

Pad Coordinates (continued)

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
124	PD.3	-3155	2428	136	PA.3	-3155	748	148	P7.3	-3155	-932
125	PD.2	-3155	2288	137	PA.2	-3155	608	149	P7.2	-3155	-1072
126	PD.1	-3155	2148	138	PA.1	-3155	468	150	P7.1	-3155	-1212
127	PD.0	-3155	2008	139	PA.0	-3155	328	151	P7.0	-3155	-1352
128	PC.3	-3155	1868	140	P9.3	-3155	188	152	P6.3	-3155	-1492
129	PC.2	-3155	1728	141	P9.2	-3155	48	153	P6.2	-3155	-1632
130	PC.1	-3155	1588	142	P9.1	-3155	-92	154	P6.1	-3155	-1772
131	PC.0	-3155	1448	143	P9.0	-3155	-232	155	P6.0	-3155	-1912
132	PB.3	-3155	1308	144	P8.3	-3155	-372	156	P5.3	-3155	-2172
133	PB.2	-3155	1168	145	P8.2	-3155	-512	157	P5.2	-3155	-2312
134	PB.1	-3155	1028	146	P8.1	-3155	-652	158	P5.1	-3155	-2452
135	PB.0	-3155	888	147	P8.0	-3155	-792	159	P5.0	-3155	-2592

PIN DESCRIPTIONS

The basic functions of each pin of the MSM63188A are described in Table 1.

A symbol with a slash (/) denotes a pin that has a secondary function.

Refer to Table 2 for secondary functions.

For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

Table 1 Pin Descriptions (Basic Functions)

Function	Symbol	Pin	Type	Description
Power Supply	V _{DD}	73	—	Positive power supply
	V _{SS}	62	—	Negative power supply
	V _{DD1}	63	—	Power supply pins for LCD bias (internally generated). Capacitors (0.1 μF) should be connected between these pins and V _{SS} .
	V _{DD2}	64		
	V _{DD3}	65		
	V _{DD4}	66		
	V _{DD5}	67		
	C1	68		
	C2	69	—	A capacitor (0.1 μF) should be connected between C1 and C2.
	V _{DDI}	87	—	Positive power supply pin for external interface (power supply for input, output, and input-output ports)
	V _{DDL}	74	—	Positive power supply pin for internal logic (internally generated). A capacitor (0.1 μF) should be connected between this pin and V _{SS} .
	V _{DDH}	70	—	Voltage multiplier pin for power supply backup (internally generated). A capacitor (1.0 μF) should be connected between this pin and V _{SS} .
	CB1	71	—	Pins to connect a capacitor for voltage multiplier.
CB2	72	—	A capacitor (1.0 μF) should be connected between CB1 and CB2.	
Oscillation	XT0	79	I	Low-speed clock oscillation pins.
	XT1	78	O	A 32.768 kHz crystal should be connected between XT0 and XT1, and C _G (5 to 25 pF) should be connected between XT0 and V _{SS} .
	OSC0	76	I	High-speed clock oscillation pins.
	OSC1	75	O	A ceramic resonator and capacitors (C _{L0} , C _{L1}) or external oscillation resistor (R _{OS}) should be connected to these pins.
Test	TST1	81	I	Input pins for testing.
	TST2	80	I	A pull-down resistor is internally connected to these pins. The user cannot use these pins.
Reset	RESET	77	I	Reset input pin. Setting this pin to "H" level puts this device into a reset state. Then, setting this pin to "L" level starts executing an instruction from address 0000H. A pull-down resistor is internally connected to this pin.
Melody	MD	84	O	Melody output pin (non-inverted output)
	MDB	85	O	Melody output pin (inverted output)

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin	Type	Description
Port	P0.0/INT5	154	I	4-bit input ports. Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P0.1/INT5	153		
	P0.2/INT5	152		
	P0.3/INT5	151		
	P1.0/INT5	150	I	
	P1.1/INT5	149		
	P1.2/INT5	148		
	P1.3/INT5	147		
	P2.0	146	O	4-bit output ports. P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P2.1	145		
	P2.2	144		
	P2.3	143		
	P3.0	142	O	
	P3.1	141		
	P3.2	140		
	P3.3	139		
	P4.0/A0	138	O	
	P4.1/A1	137		
	P4.2/A2	136		
	P4.3/A3	135		
	P5.0/A4	132	O	
	P5.1/A5	131		
	P5.2/A6	130		
	P5.3/A7	129		
	P6.0/A8	128	O	
	P6.1/A9	127		
	P6.2/A10	126		
	P6.3/A11	125		
P7.0/A12	124	O		
P7.1/A13	123			
P7.2/A14	122			
P7.3/A15	121			

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin	Type	Description
Port	P8.0/ \overline{RD}	120	I/O	4-bit input-output ports. In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P8.1/ \overline{WR}	119		
	P8.2	118		
	P8.3/INT4	117		
	P9.0/D0	116	I/O	In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P9.1/D1	115		
	P9.2/D2	114		
	P9.3/D3	113		
	PA.0/D4	112	I/O	
	PA.1/D5	111		
	PA.2/D6	110		
	PA.3/D7	109		
	PB.0/INT0/ TMOCAP/ TMOVF	108	I/O	
	PB.1/INT0/ TM1CAP/ TM1OVF	107		
	PB.2/INT0/T02CK	106		
	PB.3/INT0/T13CK	105		
	PC.0/INT1/RXD	104	I/O	
	PC.1/INT1/TXC	103		
	PC.2/INT1/RXC	102		
	PC.3/INT1/TXD	101		
PD.0/FRAME	100	I/O		
PD.1/LCLK	99			
PD.2/TBCCLK	98			
PD.3/HSCLK	97			

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin	Type	Description
LCD	COM1	61	0	LCD common signal output pins
	COM2	60		
	COM3	59		
	COM4	58		
	COM5	57		
	COM6	56		
	COM7	55		
	COM8	54		
	COM9	53		
	COM10	52		
	COM11	51		
	COM12	50		
	COM13	49		
	COM14	48		
	COM15	47		
	COM16	46		
	SEG0	44	0	LCD segment signal output pins
	SEG1	43		
	SEG2	42		
	SEG3	41		
	SEG4	40		
	SEG5	39		
	SEG6	38		
	SEG7	37		
	SEG8	36		
	SEG9	35		
	SEG10	34		
	SEG11	33		
	SEG12	32		
	SEG13	31		
	SEG14	30		
	SEG15	29		
SEG16	28			
SEG17	27			
SEG18	26			
SEG19	25			
SEG20	24			
SEG21	23			
SEG22	22			
SEG23	21			
SEG24	20			

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin	Type	Description
LCD	SEG25	19	0	LCD segment signal output pins
	SEG26	18		
	SEG27	17		
	SEG28	16		
	SEG29	15		
	SEG30	14		
	SEG31	13		
	SEG32	12		
	SEG33	11		
	SEG34	10		
	SEG35	9		
	SEG36	8		
	SEG37	7		
	SEG38	6		
	SEG39	5		
	SEG40	4		
	SEG41	3		
	SEG42	2		
	SEG43	1		
	SEG44	175		
	SEG45	174		
	SEG46	173		
	SEG47	172		
	SEG48	171		
	SEG49	170		
	SEG50	169		
	SEG51	168		
	SEG52	167		
	SEG53	166		
	SEG54	165		
	SEG55	164		
	SEG56	163		
	SEG57	162		
SEG58	161			
SEG59	160			
SEG60	159			
SEG61	158			
SEG62	157			
SEG63	156			

Table 2 shows the secondary functions of each pin of the MSM63188A.

Table 2 Pin Descriptions (Secondary Functions)

Function	Symbol	Pin	Type	Description
External Interrupt	PB.0/INT0	108	I	External 0 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit.
	PB.1/INT0	107		
	PB.2/INT0	106		
	PB.3/INT0	105		
	PC.0/INT1	104	I	External 1 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port C Interrupt Enable register (PCIE) enables or disables an interrupt for each bit.
	PC.1/INT1	103		
	PC.2/INT1	102		
	PC.3/INT1	101		
	P8.3/INT4	117	I	External 4 interrupt input pins. The change of input signal level causes an interrupt to occur.
	P0.0/INT5	154	I	External 5 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port 0 Interrupt Enable register (P0IE) and Port 1 Interrupt Enable register (P1IE) enable or disable an interrupt for each bit.
	P0.1/INT5	153		
	P0.2/INT5	152		
	P0.3/INT5	151		
	P1.0/INT5	150		
	P1.1/INT5	149		
	P1.2/INT5	148		
P1.3/INT5	147			

Table 2 Pin Descriptions (Secondary Functions) (continued)

Function	Symbol	Pin	Type	Description
Capture	PB.0/TM0CAP	108	I	Timer 0 capture input pin.
	PB.1/TM1CAP	107	I	Timer 1 capture input pin.
Timer	PB.0/TM0OVF	108	O	Timer 0 overflow flag output pin.
	PB.1/TM1OVF	107	O	Timer 1 overflow flag output pin.
	PB.2/T02CK	106	I	External clock input pin for timer 0 and timer 2.
	PB.3/T13CK	105	I	External clock input pin for timer 1 and timer 3.
LCD External Expansion	PD.0/FRAME	100	O	Frame output pin for LCD driver expansion
	PD.1/LCLK	99	O	Clock output pin for LCD driver expansion
Oscillation Output	PD.2/TBCCLK	98	O	Low-speed oscillation clock output pin
	PD.3/HSCLK	97	O	High-speed oscillation clock output pin
Serial Port	PC.0/RXD	104	I	Serial port receive data input pin
	PC.1/TXC	103	I/O	Sync serial port clock input-output pin.
				Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.
	PC.2/RXC	102	I/O	Sync serial port clock input-output pin.
Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.				
PC.3/TXD	101	O	Serial port transmit data output pin.	

Table 2 Pin Descriptions (Secondary Functions) (continued)

Function	Symbol	Pin	Type	Description
External Memory	P4.0/A0	138	0	Address output bus for external memory
	P4.1/A1	137		
	P4.2/A2	136		
	P4.3/A3	135		
	P5.0/A4	132		
	P5.1/A5	131		
	P5.2/A6	130		
	P5.3/A7	129		
	P6.0/A8	128		
	P6.1/A9	127		
	P6.2/A10	126		
	P6.3/A11	125		
	P7.0/A12	124		
	P7.1/A13	123		
	P7.2/A14	122		
P7.3/A15	121			
	P9.0/D0	116	I/O	Data bus for external memory
	P9.1/D1	115		
	P9.2/D2	114		
	P9.3/D3	113		
	PA.0/D4	112		
	PA.1/D5	111		
	PA.2/D6	110		
	PA.3/D7	109		
	P8.0/ \overline{RD}	120	0	Read signal output pin for external memory (negative logic)
	P8.1/ \overline{WR}	119	0	Write signal output pin for external memory (negative logic)

ABSOLUTE MAXIMUM RATINGS(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V _{DD1}	Ta = 25°C	-0.3 to +1.6	V
Power Supply Voltage 2	V _{DD2}	Ta = 25°C	-0.3 to +2.9	V
Power Supply Voltage 3	V _{DD3}	Ta = 25°C	-0.3 to +4.2	V
Power Supply Voltage 4	V _{DD4}	Ta = 25°C	-0.3 to +5.5	V
Power Supply Voltage 5	V _{DD5}	Ta = 25°C	-0.3 to +6.8	V
Power Supply Voltage 6	V _{DD}	Ta = 25°C	-0.3 to +6.0	V
Power Supply Voltage 7	V _{DDI}	Ta = 25°C	-0.3 to +6.0	V
Power Supply Voltage 8	V _{DDH}	Ta = 25°C	-0.3 to +6.0	V
Power Supply Voltage 9	V _{DDL}	Ta = 25°C	-0.3 to +6.0	V
Input Voltage 1	V _{IN1}	V _{DD} Input, Ta = 25°C	-0.3 to V _{DD} + 0.3	V
Input Voltage 2	V _{IN2}	V _{DDI} Input, Ta = 25°C	-0.3 to V _{DDI} + 0.3	V
Output Voltage 1	V _{OUT1}	V _{DD1} Output, Ta = 25°C	-0.3 to V _{DD1} + 0.3	V
Output Voltage 2	V _{OUT2}	V _{DD2} Output, Ta = 25°C	-0.3 to V _{DD2} + 0.3	V
Output Voltage 3	V _{OUT3}	V _{DD3} Output, Ta = 25°C	-0.3 to V _{DD3} + 0.3	V
Output Voltage 4	V _{OUT4}	V _{DD4} Output, Ta = 25°C	-0.3 to V _{DD4} + 0.3	V
Output Voltage 5	V _{OUT5}	V _{DD5} Output, Ta = 25°C	-0.3 to V _{DD5} + 0.3	V
Output Voltage 6	V _{OUT6}	V _{DD} Output, Ta = 25°C	-0.3 to V _{DD} + 0.3	V
Output Voltage 7	V _{OUT7}	V _{DDI} Output, Ta = 25°C	-0.3 to V _{DDI} + 0.3	V
Output Voltage 8	V _{OUT8}	V _{DDH} Output, Ta = 25°C	-0.3 to V _{DDH} + 0.3	V
Storage Temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

- When backup is used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	-20 to +70	°C
Operating Voltage	V _{DD}	—	0.9 to 2.7	V
	V _{DDI}	—	0.9 to 5.5	V
Crystal Oscillation Frequency	f _{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f _{CM}	V _{DD} = 1.2 to 2.7 V	300k to 500k	Hz
		V _{DD} = 1.5 to 2.7 V	200k to 1M	
External RC Oscillator Resistance	R _{OS}	V _{DD} = 1.2 to 2.7 V	100 to 300	kΩ
		V _{DD} = 1.5 to 2.7 V	50 to 300	

- When backup is not used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	-20 to +70	°C
Operating Voltage	V _{DD}	—	1.8 to 5.5	V
	V _{DDI}	—	1.8 to 5.5	V
Crystal Oscillation Frequency	f _{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f _{CM}	V _{DD} = 1.8 to 5.5 V	300k to 500k	Hz
		V _{DD} = 2.2 to 5.5 V	300k to 1M	
		V _{DD} = 2.7 to 5.5 V	200k to 2M	
External RC Oscillator Resistance	R _{OS}	V _{DD} = 1.8 to 5.5 V	100 to 300	kΩ
		V _{DD} = 2.2 to 5.5 V	50 to 300	
		V _{DD} = 2.7 to 5.5 V	30 to 300	

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD} = V_{DD1} = 0.9$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to $+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD2} Voltage	V_{DD2}	1/5 bias, 1/4 bias ($T_a = 25^\circ\text{C}$)	1.7	1.8	1.9	V	1
V_{DD2} Voltage Temperature Deviation	ΔV_{DD2}	—	—	-4	—	mV/ $^\circ\text{C}$	
V_{DD1} Voltage	V_{DD1}	1/5 bias, 1/4 bias	Typ.- 0.2	$1/2 \times V_{DD2}$	Typ.+ 0.2	V	
V_{DD3} Voltage	V_{DD3}	1/5 bias	Typ.- 0.3	$3/2 \times V_{DD2}$	Typ.+ 0.3	V	
		1/4 bias (connect V_{DD3} and V_{DD2})	Typ.- 0.2	V_{DD2}	Typ.+ 0.2		
V_{DD4} Voltage	V_{DD4}	1/5 bias	Typ.- 0.4	$2 \times V_{DD2}$	Typ.+ 0.4	V	
		1/4 bias	Typ.- 0.3	$3/2 \times V_{DD2}$	Typ.+ 0.3		
V_{DD5} Voltage	V_{DD5}	1/5 bias	Typ.- 0.5	$5/2 \times V_{DD2}$	Typ.+ 0.5	V	
		1/4 bias	Typ.- 0.4	$2 \times V_{DD2}$	Typ.+ 0.4		
V_{DDH} Voltage (Backup used)	V_{DDH}	High-speed clock oscillation stopped $V_{DD} = 1.5$ V	2.8	—	3.0	V	
		High-speed clock oscillation (Ceramic oscillation, 1 MHz) $V_{DD} = 1.5$ V	2.0	—	2.7	V	
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillation stopped	0.8	1.3	1.8	V	
		High-speed clock oscillation ($V_{DD} = 1.2$ to 5.5 V)	1.2	—	5.5	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	1.0	—	—	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	Backup	0.9	—	—	V	
		Backup not used	1.7	—	—	V	
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External Crystal Oscillator Capacitance	C_G	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C_D	—	20	25	30	pF	
External Ceramic Oscillator Capacitance	$C_{L0, 1}$	CSA2.00MG (Murata MFG.-make) used $V_{DD} = 3.0$ V	—	30	—	pF	
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16	pF	
POR Voltage	V_{POR1}	$V_{DD} = 1.5$ V	0.0	—	0.4	V	
		$V_{DD} = 3.0$ V	0.0	—	0.7	V	
Non-POR Voltage	V_{POR2}	$V_{DD} = 1.5$ V	1.2	—	1.5	V	
		$V_{DD} = 3.0$ V	2.0	—	3.0	V	

Notes: 1. " T_{STOP} " indicates that if the crystal oscillator stops over the value of T_{STOP} , the system reset occurs.

2. "POR" denotes Power On Reset.

3. " V_{POR1} " indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD} .

4. " V_{POR2} " indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD} .

DC Characteristics (continued)

- When backup is used

($V_{DD} = V_{DD1} = 1.5\text{ V}$, $V_{SS} = 0\text{ V}$, 1/5 bias, $T_a = -20\text{ to }+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	$T_a = -20\text{ to }+50^\circ\text{C}$	—	5.6	7.0	μA	1
			$T_a = -20\text{ to }+70^\circ\text{C}$	—	5.6	8.5		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	$T_a = -20\text{ to }+50^\circ\text{C}$	—	4.5	5.5	μA	
			$T_a = -20\text{ to }+70^\circ\text{C}$	—	4.5	7.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	—	18	22	μA		
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation, $f = \text{approx. } 720\text{ kHz}$, $R_{OS} = 51\text{ k}\Omega$)	—	700	900	μA		
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)	—	800	1000	μA		

- When backup is not used

($V_{DD} = V_{DD1} = 3.0\text{ V}$, $V_{SS} = 0\text{ V}$, 1/5 bias, $T_a = -20\text{ to }+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	$T_a = -20\text{ to }+50^\circ\text{C}$	—	2.7	3.0	μA	1
			$T_a = -20\text{ to }+70^\circ\text{C}$	—	2.7	3.5		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	$T_a = -20\text{ to }+50^\circ\text{C}$	—	2.1	2.4	μA	
			$T_a = -20\text{ to }+70^\circ\text{C}$	—	2.1	3.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	—	8.5	10.5	μA		
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation)	$f = \text{approx. } 800\text{ kHz}$, $R_{OS} = 51\text{ k}\Omega$	—	550	800	μA	
			$f = \text{approx. } 500\text{ kHz}$, $R_{OS} = 100\text{ k}\Omega$	—	390	450		
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)	—	1000	1500	μA		

DC Characteristics (continued)

($V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$, $V_{SS} = 0\text{ V}$, $V_{DD1} = 1.1\text{ V}$, $V_{DD2} = 2.2\text{ V}$, $V_{DD3} = 3.3\text{ V}$, $V_{DD4} = 4.4\text{ V}$, $V_{DD5} = 5.5\text{ V}$, $T_a = -20\text{ to }+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Output Current 1 (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) ⋮ (PC.0 to PC.3) (PD.0 to PD.3)	I_{OH1}	$V_{OH1} = V_{DD1} - 0.5\text{ V}$	$V_{DD1} = 1.5\text{ V}$	-2.0	-1.2	-0.2	mA	2
			$V_{DD1} = 3.0\text{ V}$	-5.0	-3.0	-1.0	mA	
			$V_{DD1} = 5.0\text{ V}$	-8.0	-4.0	-1.5	mA	
	I_{OL1}	$V_{OL1} = 0.5\text{ V}$	$V_{DD1} = 1.5\text{ V}$	0.2	1.2	2.0	mA	
			$V_{DD1} = 3.0\text{ V}$	1.0	3.0	5.0	mA	
			$V_{DD1} = 5.0\text{ V}$	1.5	4.0	8.0	mA	
Output Current 2 (MD, MDB)	I_{OH2}	$V_{OH2} = V_{DD} - 0.7\text{ V}$	$V_{DD} = 1.5\text{ V}$	-2.5	-1.3	-0.4	mA	
			$V_{DD} = 3.0\text{ V}$	-6.0	-4.0	-2.0	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-9.0	-5.5	-3.0	mA	
	I_{OL2}	$V_{OL2} = 0.7\text{ V}$	$V_{DD} = 1.5\text{ V}$	0.4	1.3	2.5	mA	
			$V_{DD} = 3.0\text{ V}$	2.0	4.0	6.0	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	3.0	5.5	9.0	mA	
Output Current 3 (SEG0 to SEG63) (COM1 to COM16)	I_{OH3}	$V_{OH3} = V_{DD5} - 0.2\text{ V}$ (V_{DD5} level)	—	—	-4	μA		
	I_{OHM3}	$V_{OHM3} = V_{DD4} + 0.2\text{ V}$ (V_{DD4} level)	4	—	—	μA		
	I_{OHM3S}	$V_{OHM3S} = V_{DD4} - 0.2\text{ V}$ (V_{DD4} level)	—	—	-4	μA		
	I_{OMH3}	$V_{OMH3} = V_{DD3} + 0.2\text{ V}$ (V_{DD3} level)	4	—	—	μA		
	I_{OMH3S}	$V_{OMH3S} = V_{DD3} - 0.2\text{ V}$ (V_{DD3} level)	—	—	-4	μA		
	I_{OML3}	$V_{OML3} = V_{DD2} + 0.2\text{ V}$ (V_{DD2} level)	4	—	—	μA		
	I_{OML3S}	$V_{OML3S} = V_{DD2} - 0.2\text{ V}$ (V_{DD2} level)	—	—	-4	μA		
	I_{OLM3}	$V_{OLM3} = V_{DD1} + 0.2\text{ V}$ (V_{DD1} level)	4	—	—	μA		
	I_{OLM3S}	$V_{OLM3S} = V_{DD1} - 0.2\text{ V}$ (V_{DD1} level)	—	—	-4	μA		
	I_{OL3}	$V_{OL3} = V_{SS} + 0.2\text{ V}$ (V_{SS} level)	4	—	—	μA		
Output Current 4 (OSC1)	I_{OH4R}	$V_{OH4R} = V_{DDH} - 0.5\text{ V}$ (RC oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-2.5	-1.5	-0.75	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-3.5	-2.0	-1.0	mA	
	I_{OL4R}	$V_{OL4R} = 0.5\text{ V}$ (RC oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	0.75	1.5	2.5	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	1.0	2.0	3.5	mA	
	I_{OH4C}	$V_{OH4C} = V_{DDH} - 0.5\text{ V}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-300	-180	-60	μA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-450	-280	-100	μA	
	I_{OL4C}	$V_{OL4C} = 0.5\text{ V}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	60	120	300	μA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	100	200	450	μA	
Output Leakage (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) ⋮ (PD.0 to PD.3)	I_{OOH}	$V_{OH} = V_{DD1}$	—	—	0.3	μA		
	I_{OOL}	$V_{OL} = V_{SS}$	-0.3	—	—	μA		

DC Characteristics (continued)

($V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$, $V_{SS} = 0\text{ V}$, $V_{DD1} = 1.1\text{ V}$, $V_{DD2} = 2.2\text{ V}$, $V_{DD3} = 3.3\text{ V}$, $V_{DD4} = 4.4\text{ V}$, $V_{DD5} = 5.5\text{ V}$, $T_a = -20\text{ to }+70^\circ\text{C}$ unless otherwise specified)

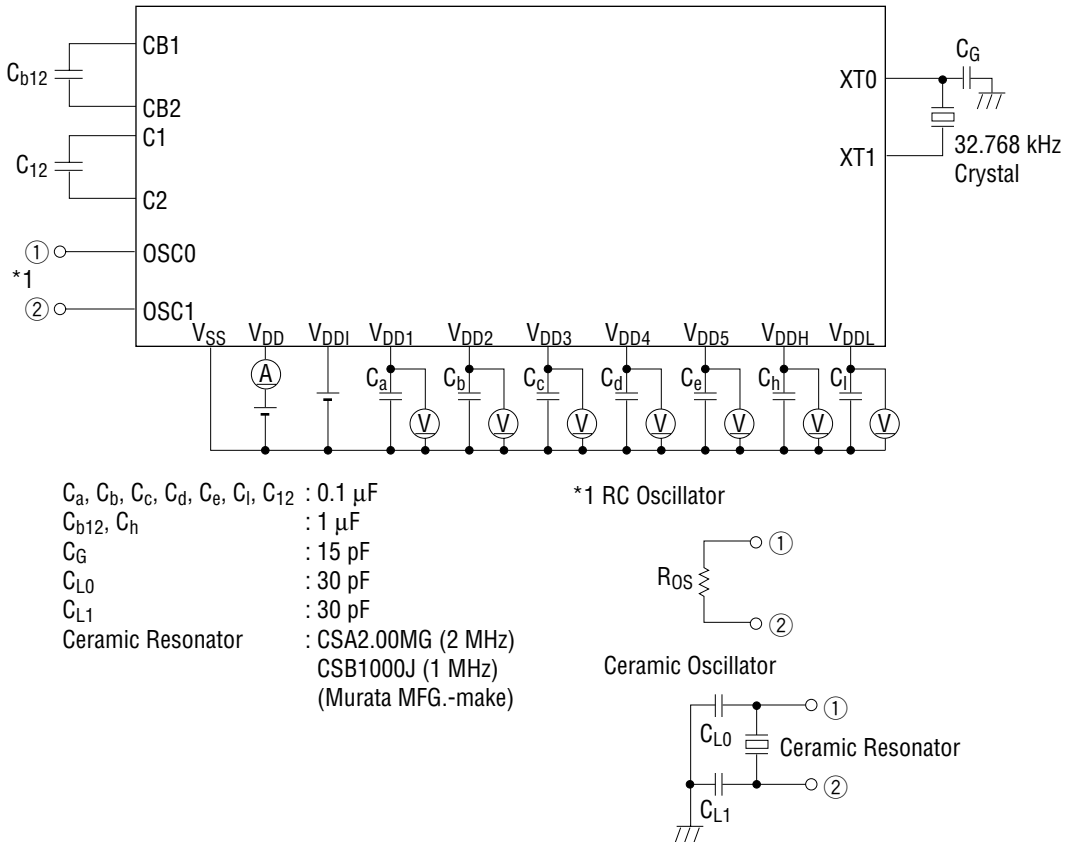
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PD.0 to PD.3)	I_{IH1}	$V_{IH1} = V_{DD1}$ (when pulled down)	$V_{DD1} = 1.5\text{ V}$	2	10	30	μA	3
			$V_{DD1} = 3.0\text{ V}$	30	90	180	μA	
			$V_{DD1} = 5.0\text{ V}$	70	250	600	μA	
	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	$V_{DD1} = 1.5\text{ V}$	-30	-10	-2	μA	
			$V_{DD1} = 3.0\text{ V}$	-180	-90	-30	μA	
			$V_{DD1} = 5.0\text{ V}$	-600	-250	-70	μA	
	I_{IH1Z}	$V_{IH1} = V_{DD1}$ (in a high impedance state)	0.0	—	1.0	μA		
I_{IL1Z}	$V_{IL1} = V_{SS}$ (in a high impedance state)	-1.0	—	0.0	μA			
Input Current 2 (OSC0)	I_{IL2}	$V_{IL2} = V_{SS}$ (when pulled up)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-200	-110	-30	μA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-600	-350	-150	μA	
	I_{IH2R}	$V_{IH2R} = V_{DDH}$ (RC oscillation)	0.0	—	1.0	μA		
	I_{IL2R}	$V_{IL2R} = V_{SS}$ (RC oscillation)	-1.0	—	0.0	μA		
	I_{IH2C}	$V_{IH2C} = V_{DDH}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	0.1	0.5	1.0	μA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.75	1.5	3.0	μA	
	I_{IL2C}	$V_{IL2C} = V_{SS}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-1.0	-0.5	-0.1	μA	
$V_{DD} = V_{DDH} = 5.0\text{ V}$			-3.0	-1.5	-0.75	μA		
Input Current 3 (RESET)	I_{IH3}	$V_{IH3} = V_{DD}$	$V_{DD} = 1.5\text{ V}$	10	50	80	μA	
			$V_{DD} = 3.0\text{ V}$	150	350	600	μA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.5	1.0	2.0	mA	
	I_{IL3}	$V_{IL3} = V_{SS}$	-1.0	—	0.0	μA		
Input Current 4 (TST1, TST2)	I_{IH4}	$V_{IH4} = V_{DD}$	$V_{DD} = 1.5\text{ V}$	50	150	300	μA	
			$V_{DD} = 3.0\text{ V}$	0.5	1.0	1.5	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	1.25	2.5	4.0	mA	
	I_{IL4}	$V_{IL4} = V_{SS}$	-1.0	—	0.0	μA		

DC Characteristics (continued)

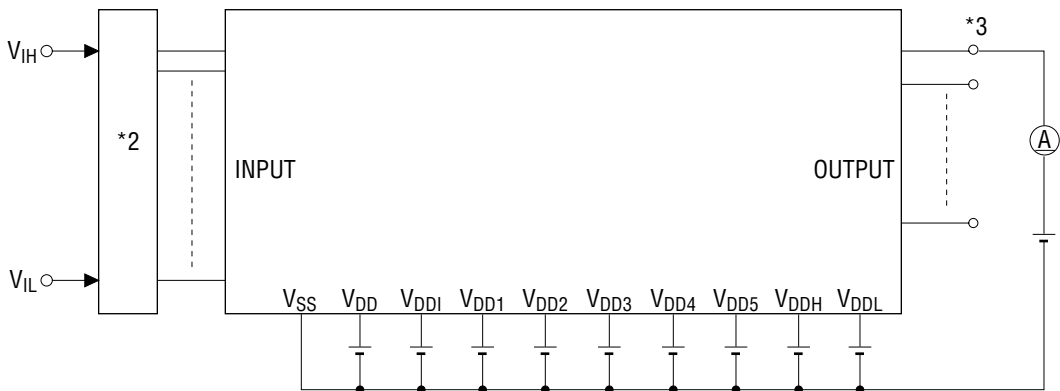
($V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$, $V_{SS} = 0\text{ V}$, $V_{DD1} = 1.1\text{ V}$, $V_{DD2} = 2.2\text{ V}$, $V_{DD3} = 3.3\text{ V}$, $V_{DD4} = 4.4\text{ V}$, $V_{DD5} = 5.5\text{ V}$, $T_a = -20\text{ to }+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PD.0 to PD.3)	V_{IH1}	$V_{DD1} = 1.5\text{ V}$	1.2	—	1.5	V	4
		$V_{DD1} = 3.0\text{ V}$	2.4	—	3.0	V	
		$V_{DD1} = 5.0\text{ V}$	4.0	—	5.0	V	
	V_{IL1}	$V_{DD1} = 1.5\text{ V}$	0.0	—	0.3	V	
		$V_{DD1} = 3.0\text{ V}$	0.0	—	0.6	V	
		$V_{DD1} = 5.0\text{ V}$	0.0	—	1.0	V	
Input Voltage 2 (OSC0)	V_{IH2}	$V_{DD} = V_{DDH} = 3.0\text{ V}$	2.4	—	3.0	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	4.0	—	5.0	V	
	V_{IL2}	$V_{DD} = V_{DDH} = 3.0\text{ V}$	0.0	—	0.6	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.0	—	1.0	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	$V_{DD} = 1.5\text{ V}$	1.35	—	1.5	V	
		$V_{DD} = 3.0\text{ V}$	2.4	—	3.0	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	4.0	—	5.0	V	
	V_{IL3}	$V_{DD} = 1.5\text{ V}$	0.0	—	0.15	V	
		$V_{DD} = 3.0\text{ V}$	0.0	—	0.6	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.0	—	1.0	V	
Hysteresis Width 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PD.0 to PD.3)	ΔV_{T1}	$V_{DD1} = 1.5\text{ V}$	0.05	0.1	0.3	V	
		$V_{DD1} = 3.0\text{ V}$	0.2	0.5	1.0	V	
		$V_{DD1} = 5.0\text{ V}$	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV_{T2}	$V_{DD} = 1.5\text{ V}$	0.05	0.1	0.3	V	
		$V_{DD} = 3.0\text{ V}$	0.2	0.5	1.0	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.25	1.0	1.5	V	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PC.0 to PC.3) (PD.0 to PD.3)	C_{IN}	—	—	—	5	pF	1

Measuring circuit 1



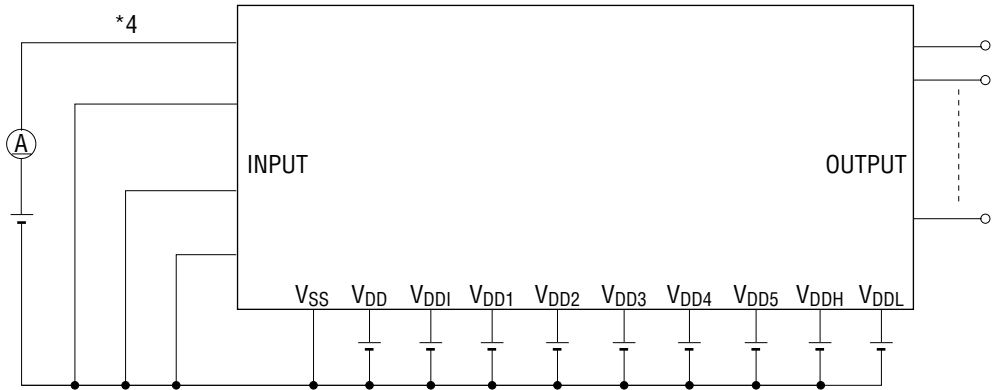
Measuring circuit 2



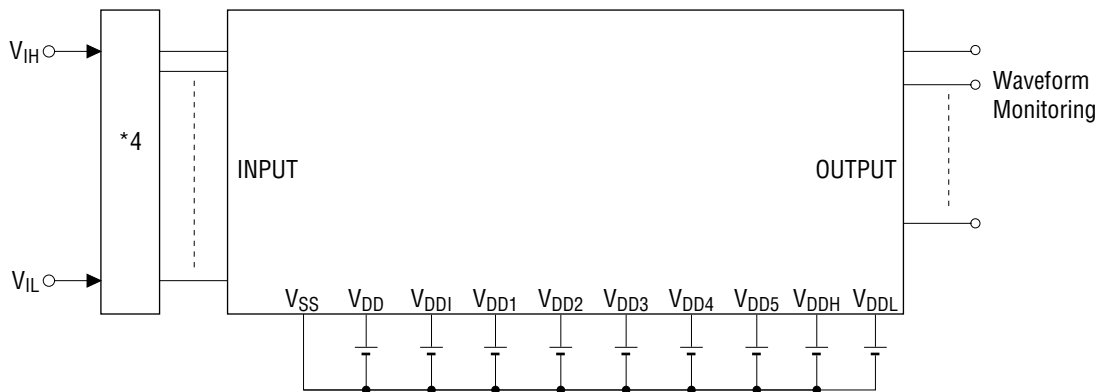
*2 Input logic circuit to determine the specified measuring conditions.

*3 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*4 Measured at the specified input pins.

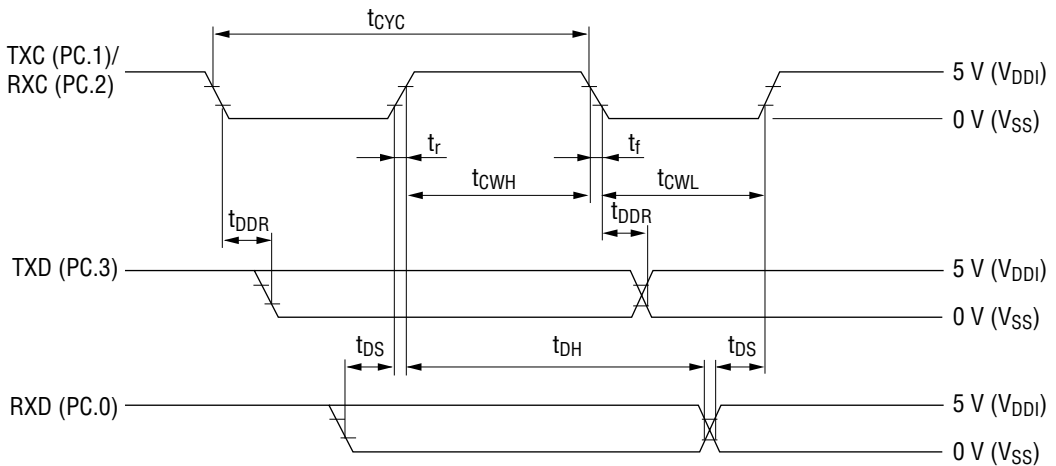
AC Characteristics (Serial Interface, Serial Port)

($V_{DD} = 0.9$ to 5.5 V, $V_{DDH} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, $V_{DDI} = 5.0$ V, $T_a = -20$ to $+70^\circ\text{C}$ unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	μs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	μs
TXC/RXC Input "L" Level Pulse Width	t_{cWL}	—	0.8	—	—	μs
TXC/RXC Input "H" Level Pulse Width	t_{cWH}	—	0.8	—	—	μs
TXC/RXC Input Cycle Time	t_{cYC}	—	2.0	—	—	μs
TXC/RXC Output Cycle Time	$t_{cYC1(0)}$	CPU in operation state at 32 kHz	—	30.5	—	μs
	$t_{cYC2(0)}$	CPU in operation at 2 MHz $V_{DD} = V_{DDH} = 2.7$ V to 5.5 V	—	0.5	—	μs
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	μs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	μs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	μs

Synchronous communication timing
("H" level = 4.0 V, "L" level = 1.0 V)

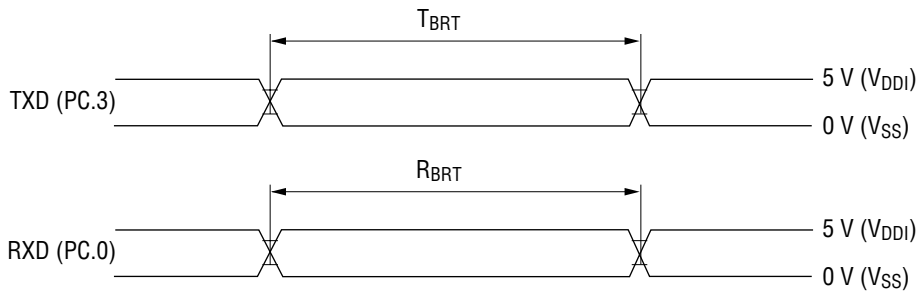


(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	s

f_{BRT} : Baud rates (1200, 2400, 4800, 9600 bps)

UART communication timing
("H" level = 4.0 V, "L" level = 1.0 V)



AC Characteristics (External Memory Interface)

($V_{DD} = 0.9$ to 5.5 V, $V_{DDH} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, $V_{DDI} = 5.0$ V, $T_a = -20$ to $+70^\circ\text{C}$ unless otherwise specified)

(1) Reading from External Memory

(a) When CPU operates at 32.768 kHz

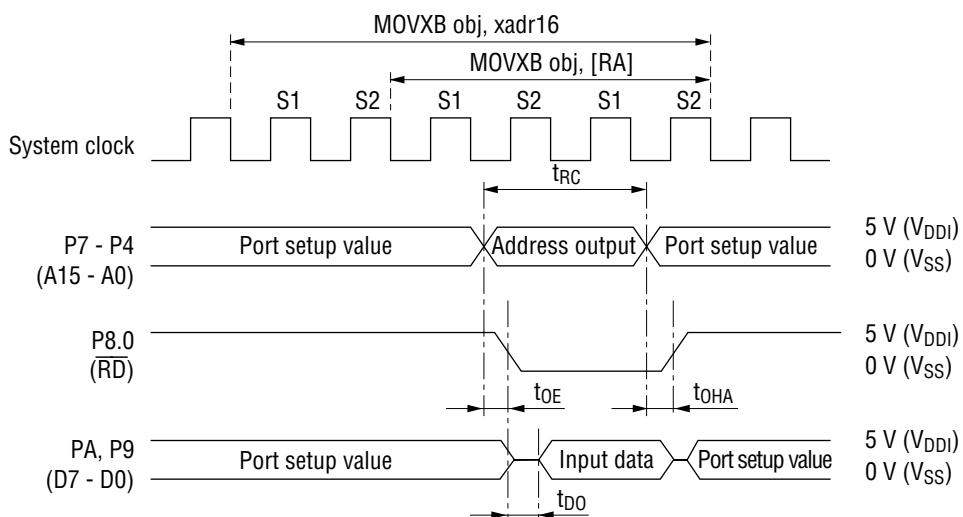
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61.0	—	μs
$\overline{\text{RD}}$ Output Delay Time	t_{OE}	—	—	—	5.0	μs
Output Valid Time	t_{OHA}	—	—	—	5.0	μs
External Memory Output Delay Time	t_{DO}	—	—	—	5.0	μs

(b) When CPU operates at 2 MHz ($V_{DDH} = 2.7$ to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1.0	—	—	μs
$\overline{\text{RD}}$ Output Delay Time	t_{OE}	—	—	—	100	ns
Output Valid Time	t_{OHA}	—	—	—	100	ns
External Memory Output Delay Time	t_{DO}	—	—	—	150	ns

AC characteristics timing

("H" level = 4.0 V, "L" level = 1.0 V)



(2) Writing to External Memory

(a) When CPU operates at 32.768 kHz

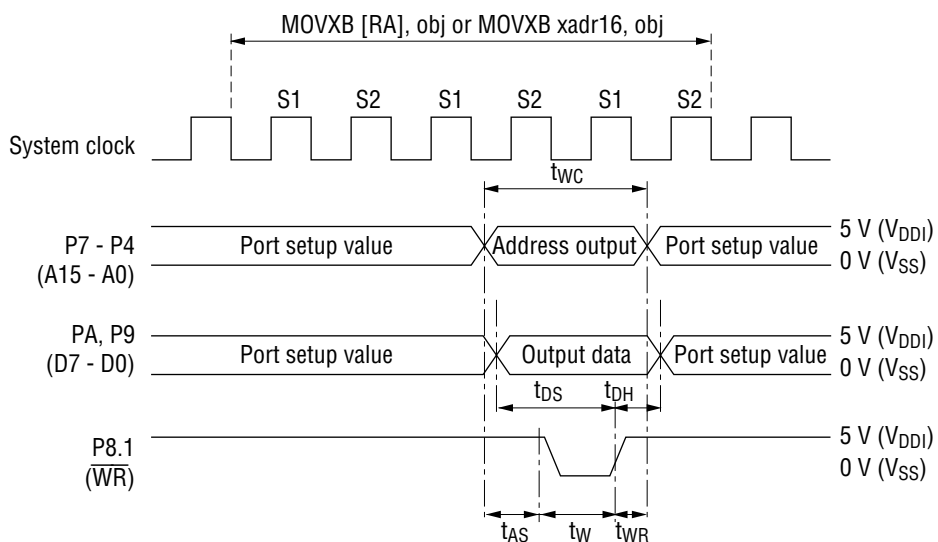
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61.0	—	μs
Address Setup Time	t_{AS}	—	—	30.5	—	μs
Write Time	t_W	—	—	15.3	—	μs
Write Recovery Time	t_{WR}	—	—	15.3	—	μs
Data Setup Time	t_{DS}	—	—	45.8	—	μs
Data Hold Time	t_{DH}	—	—	15.3	—	μs

(b) When CPU operates at 2 MHz ($V_{DDH} = 2.7$ to 5.5 V)

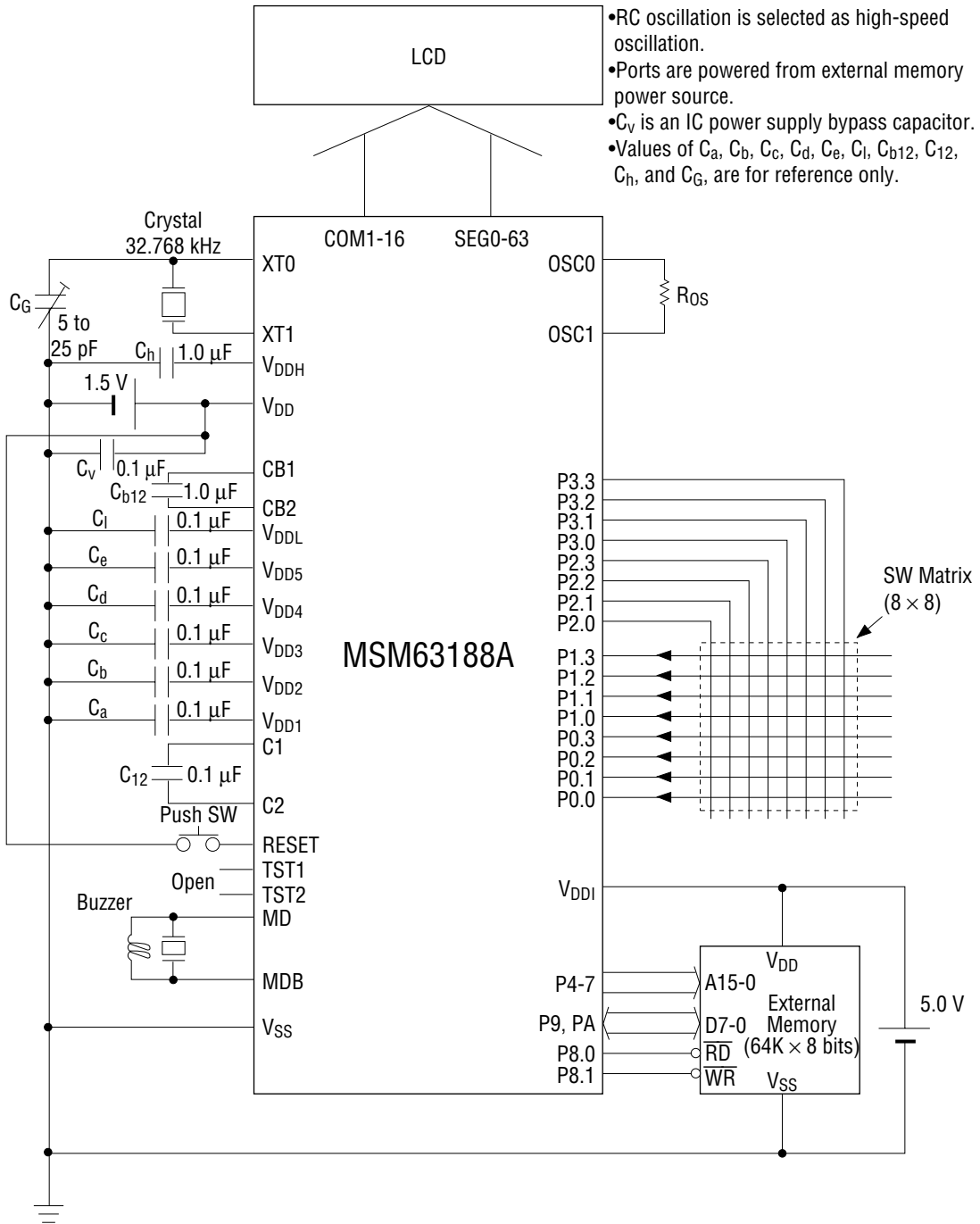
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1.0	—	—	μs
Address Setup Time	t_{AS}	—	0.4	—	—	μs
Write Time	t_W	—	0.2	—	—	μs
Write Recovery Time	t_{WR}	—	0.2	—	—	μs
Data Setup Time	t_{DS}	—	0.7	—	—	μs
Data Hold Time	t_{DH}	—	0.2	—	—	μs

AC characteristics timing

("H" level = 4.0 V, "L" level = 1.0 V)



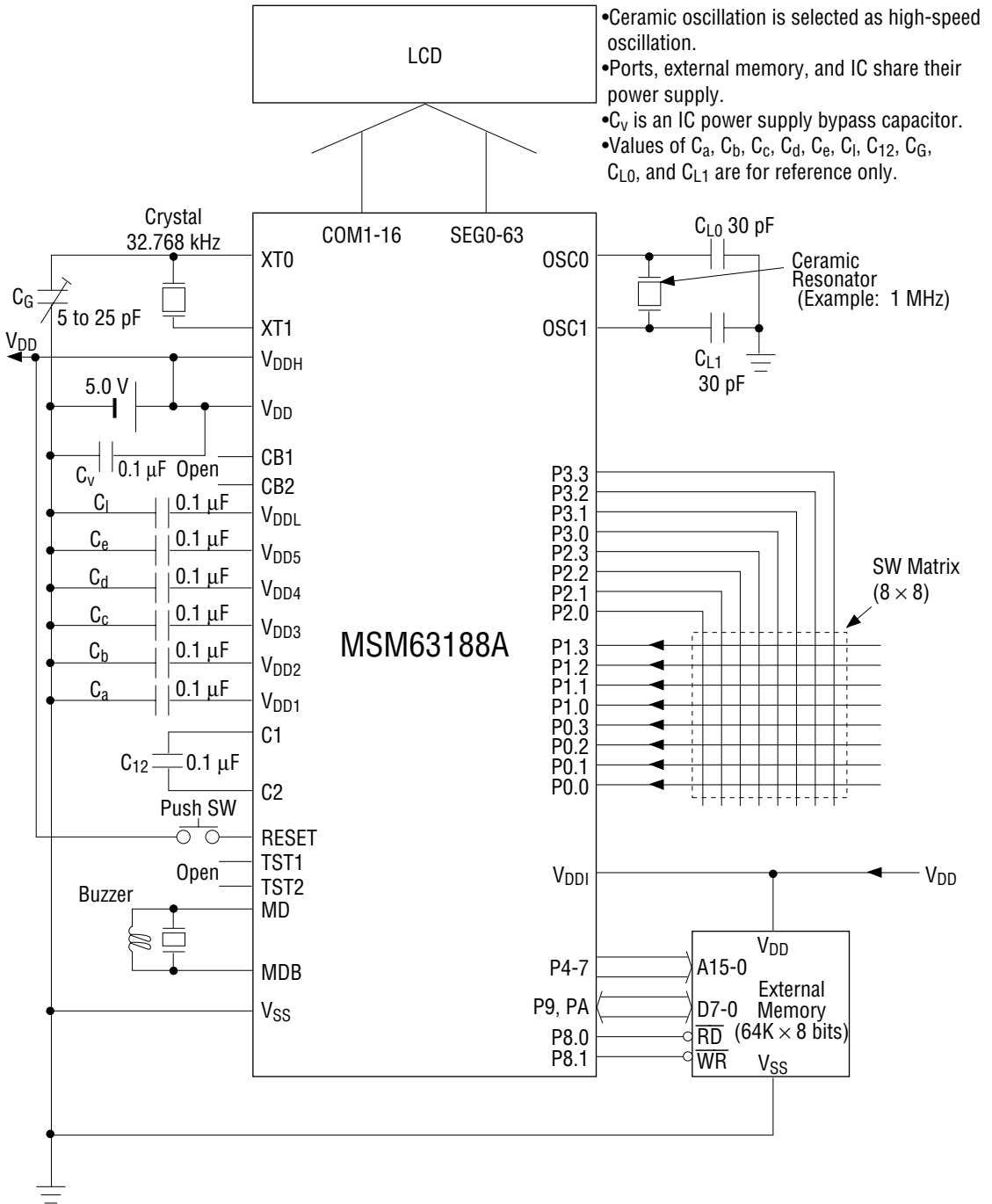
APPLICATION CIRCUITS



Note: VDDI is the power supply pin for the input, output, and input-output ports. Be sure to connect the VDDI pin either to the positive power supply pin (VDD) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with Power Supply Backup

APPLICATION CIRCUITS (continued)



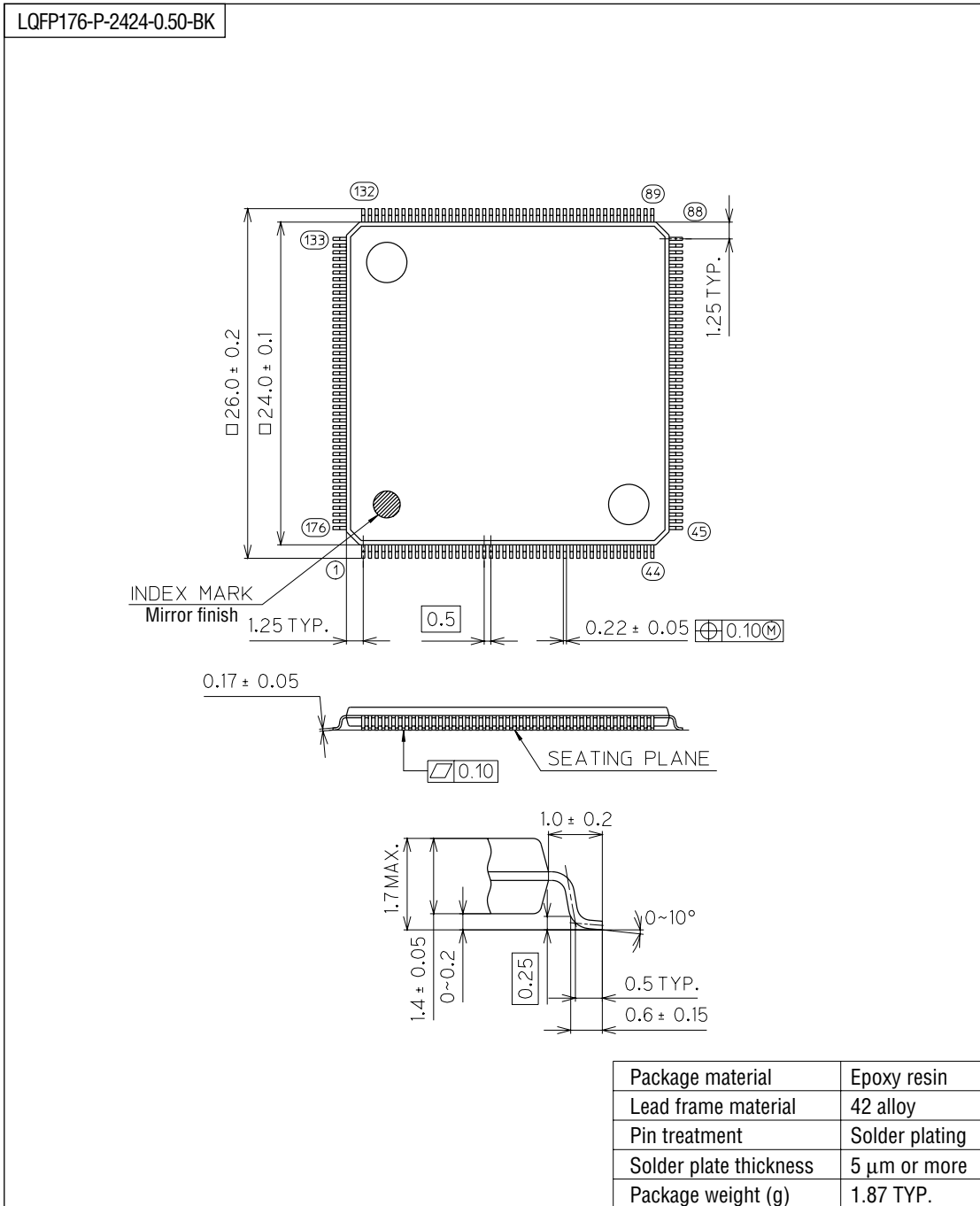
- Ceramic oscillation is selected as high-speed oscillation.
- Ports, external memory, and IC share their power supply.
- C_v is an IC power supply bypass capacitor.
- Values of C_a, C_b, C_c, C_d, C_e, C_i, C₁₂, C_G, C_{L0}, and C_{L1} are for reference only.

Note: V_{DDI} is the power supply pin for the input, output, and input-output ports. Be sure to connect the V_{DDI} pin either to the positive power supply pin (V_{DD}) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with No Power Supply Backup

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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