MK3723
Low Cost 3.3 Volt VCXO

Description

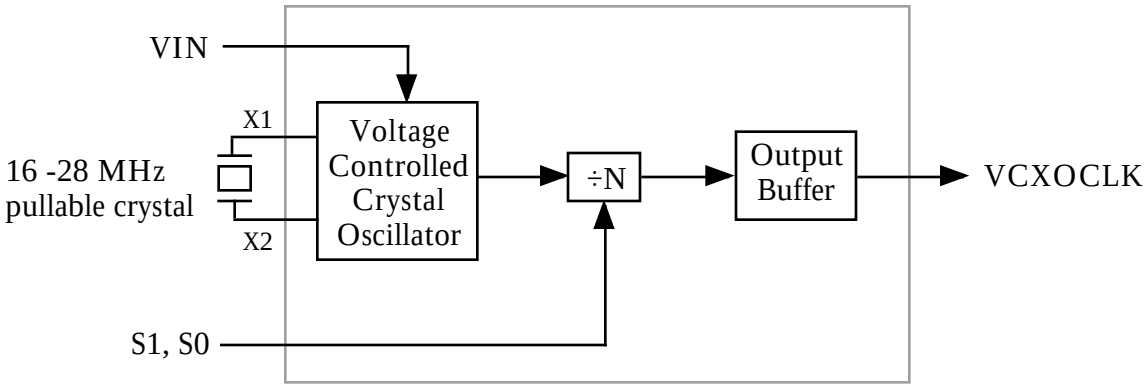
The MK3723 is ICS/MicroClock's lowest cost, low jitter, high performance 3.3 volt VCXO designed to replace expensive VCXO modules. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ±100 ppm. Using ICS/MicroClock's patented VCXO techniques, the device uses an inexpensive external pullable crystal in the range of 16 - 28 MHz to produce a VCXO output clock that is a divide by 2, 4, 6, or 8 or the crystal frequency.

ICS/MicroClock manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. If more clock outputs are needed, see the MK3732 or MK377x family of parts. Consult ICS/MicroClock to eliminate VCXOs, crystals and oscillators from your board.

Features

- Packaged in 8 pin SOIC
- 3.3 V only operating voltage
- 2 MHz to 14 MHz VCXO operation
- Ideal for 26 MHz from a 28 MHz crystal
- Uses an inexpensive external crystal
- On-chip VCXO (patented) with pull range of 200 ppm (minimum)
- VCXO tuning voltage of 0 to 3.3 V
- 12 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- For frequencies between 16.2 MHz and 28 MHz use the MK3721S. For higher than 28 MHz, use the MK3732-05

Block Diagram



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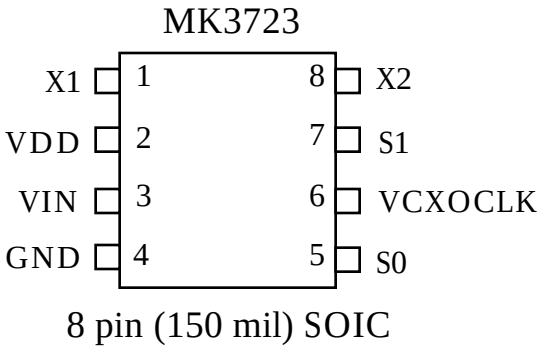
Pin Assignment



8 pin (150 mil) SOIC

Divider Select Table

S1	S0	VCXOCLK (MHz)
0	0	Crystal ÷2
0	1	Crystal ÷4
1	0	Crystal ÷6
1	1	Crystal ÷8

0 = connect directly to ground
1 = connect directly to VDD

Pin Descriptions

Number	Name	Description
1	X1	Crystal connection. Connect to a pullable 10 to 20 MHz crystal.
2	VDD	VDD. Connect to + 3.3 V.
3	VIN	Voltage input to VCXO. Zero to 3.3 V analog input which controls the frequency of the VCXO.
4	GND	Connect to ground.
5	S0	Select pin for VCXO divider. See table above.
6	VCXOCLK	VCXO clock output. Full CMOS output amplitude.
7	S1	Select pin for VCXO divider. See table above.
8	X2	Crystal connection. Connect to a pullable 16 to 28 MHz crystal.

Crystal Specifications

Correlation (load) capacitance	14 pF
Initial accuracy	±20 ppm maximum
Drift over temperature and aging	±50 ppm maximum
C0/C1 ratio	240 maximum
ESR	35 Ω maximum

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3.15		3.45	V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-4mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		4		mA
Short Circuit Current			±50		mA
VIN, VCXO control voltage		0		3.3	V
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Crystal Frequency		16		28	MHz
Input Crystal Accuracy				±30	ppm
VCXO Output Clock Frequency		2		14	MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40	50	60	%
Maximum Absolute Jitter, short term			100		ps
Output frequency pullability, note 2	0V ≤ VIN ≤ 3.3 V	±100	±180		ppm

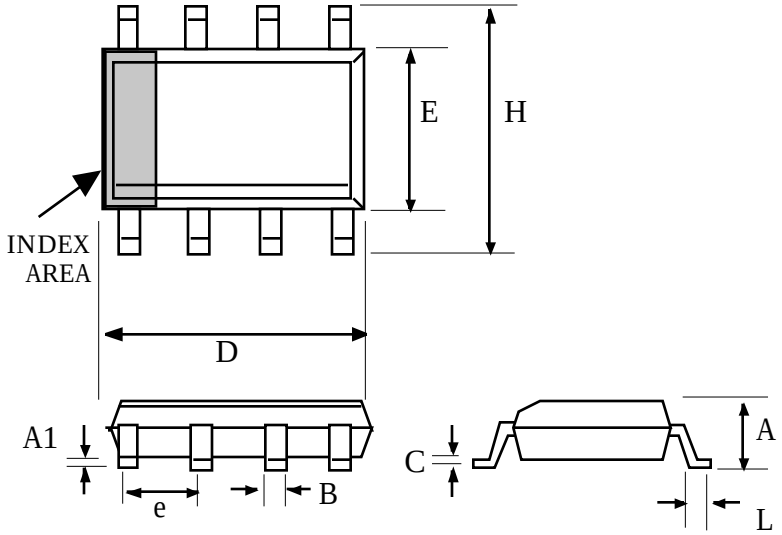
Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With a ICS/MicroClock approved pullable crystal.

External Components

The MK3723 requires a minimum number of external components for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD and GND on pins 2 and 4, as close to the MK3723 as possible. A series termination resistor of 33 Ω may be used for the clock output. The input crystal must be connected as close to the chip as possible. The input crystal should be a parallel mode, pullable, AT cut, with 14 pF load capacitance. See previous page for crystal specifications. Consult ICS for recommended suppliers. IMPORTANT - read application note MAN05 before laying out the PCB.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.1890	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK3723S	MK3723S	tubes	8 pin SOIC	0-70 °C
MK3723STR	MK3723S	tape and reel	8 pin SOIC	0-70 °C