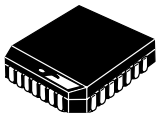
MOTOROLA
Semiconductor Components

Order Number: MC100EP195/D
Rev. 0.1, 05/1999

MC100EP195

PROGRAMMABLE DELAY CHIP

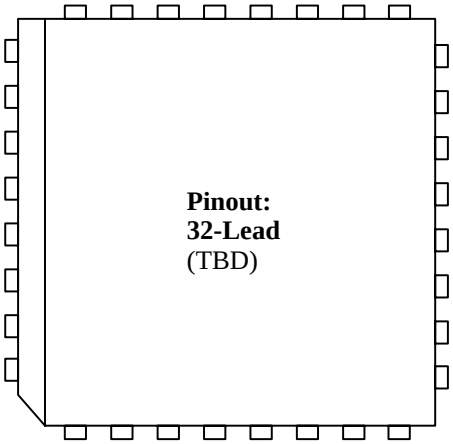


32 Lead TQFP
PLASTIC PACKAGE
CASE TBD

ECLinPS Plus™

Product Preview

Programmable Delay Chip



Pinout:
32-Lead
(TBD)

- 10ns Maximum Case Delay Range
- ≈20ps/Delay Step Resolution
- >1.0GHz Bandwidth
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- On Chip Cascade Circuitry
- 75KΩ Input Pulldown Resistors
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = TBD devices

The MC100EP195 is a programmable delay chip (PDC) designed primarily for clock de-skewing and timing adjustment. It provides variable delay of a differential LVECL input transition.

The delay section consists of a chain of gates organized as shown in the logic symbol. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80 ps. These two elements provide the EP195 with a digitally-selectable resolution of approximately 20 ps. The required device delay is selected by the seven address inputs D[0:8], which are latched on chip by a high signal on the latch enable (LEN) control. When LEN is low latch inputs are transparent and will allow dynamic changes.

Because the delay programmability of the EP195 is achieved by purely differential ECL gate delays the device will operate at frequencies of >1.0 GHz while maintaining over 600 mV of output swing.

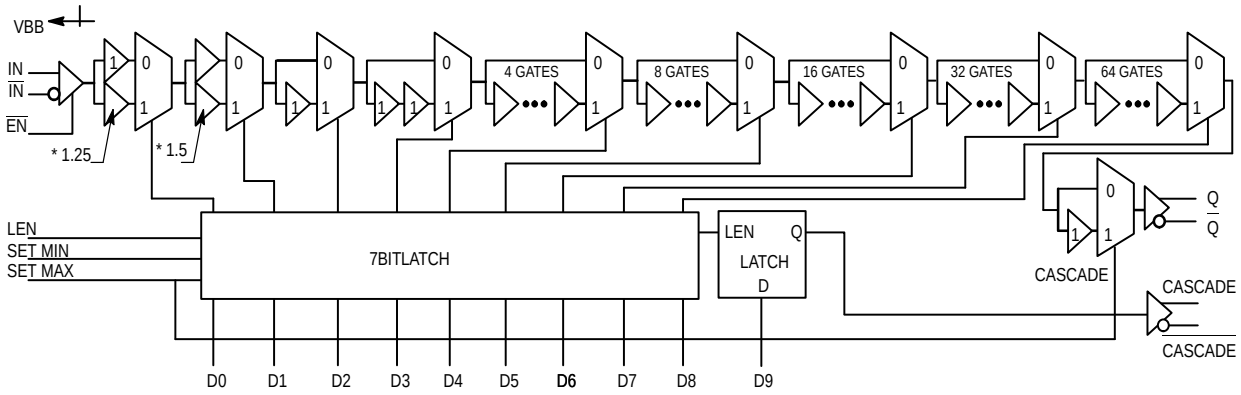
The EP195 thus offers very fine resolution, at very high frequencies, that is selectable entirely from a digital input allowing for very accurate system clock timing.

A tenth latched input, D9, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

PIN NAMES

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:9]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Min Delay Set
SET MAX	Max Delay Set
CASCADE	Cascade Signal Output
V_{BB}	Output Voltage Reference

LOGIC DIAGRAM – SIMPLIFIED



* DELAYS ARE 25% OR 50% LONGER THAN STANDARD (STANDARD ≈ 80 PS)

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)												
		0°C			**25°C**			**85°C**				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current			TBD						TBD	mA	

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)												
		0°C			**25°C**			**85°C**				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
t_{PLH} t_{PHL}	Propagation Delay IN to Q; Tap = 0 IN to Q; Tap = 508 $\overline{EN}$ to Q; Tap = 0 D7 to CASCADE									 TBD	ps	
t_{RANGE}	Programmable Range t_{PD} (max) – t_{PD} (min)										ps	
Δt	Step Delay D0 High D1 High D2 High D3 High D4 High D5 High D6 High D7 High D8 High									 20 40 80 120 240 480 960 1920 3840	ps	6
Lin	Linearity	D1	D0		D1	D0		D1	D0			7
t_{SKEW}	Duty Cycle Skew t_{PHL}–t_{PLH}		 ±30			 ±30			 ±30		ps	 1
t_S	Setup Time D to LEN D to IN $\overline{EN}$ to IN		 0			 0			 0		ps	 2 3
t_h	Hold Time LEN to D IN to $\overline{EN}$										ps	 4
t_R	Release Time $\overline{EN}$ to IN SET MAX to LEN SET MIN to LEN										ps	 5
t_{jit}	Jitter		<5.0			<5.0			<5.0		ps	8
t_r t_f	Output Rise/Fall Time 20–80% (Q) 20–80% (CASCADE)		TBD								ps	

1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs Dn). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

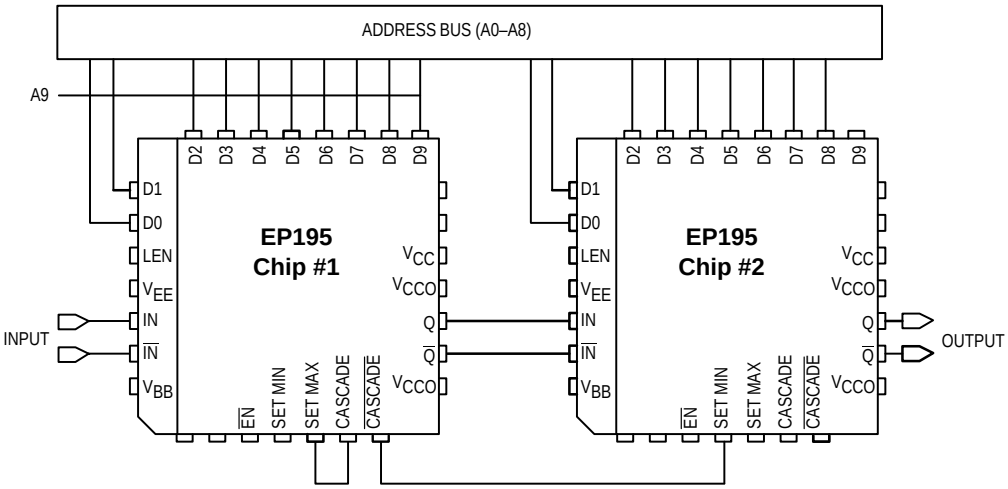


Figure 1. Cascading Interconnect Architecture

Cascading Multiple EP195's

To increase the programmable range of the EP195 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP195's without the need for any external gating. Furthermore this capability requires only one more address line per added EP195. Obviously cascading multiple PDC's will result in a larger programmable range however this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two EP195's. As can be seen, this scheme can easily be expanded for larger EP195 chains. The D9 input of the EP195 is the cascade control pin. With the interconnect scheme of Figure 1 when D9 is asserted it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D9 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0–A8 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A8. If the delay needed is greater than can be achieved with 127.75 gate delays (1111111 on the A0–A8 address bus) D9 will be asserted to signal the need to cascade the delay to the next EP195 device. When D9 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0–A8 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0–A8 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D9 of chip #1 is asserted the delay increases from 127.75 gates to 128 gates. A 128 gate delay is the maximum delay setting for the EP195.

To expand this cascading scheme to more devices one simply needs to connect the D9 input and CASCADE outputs of the current most significant EP195 to the new most significant EP195 in the same manner as pictured in Figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

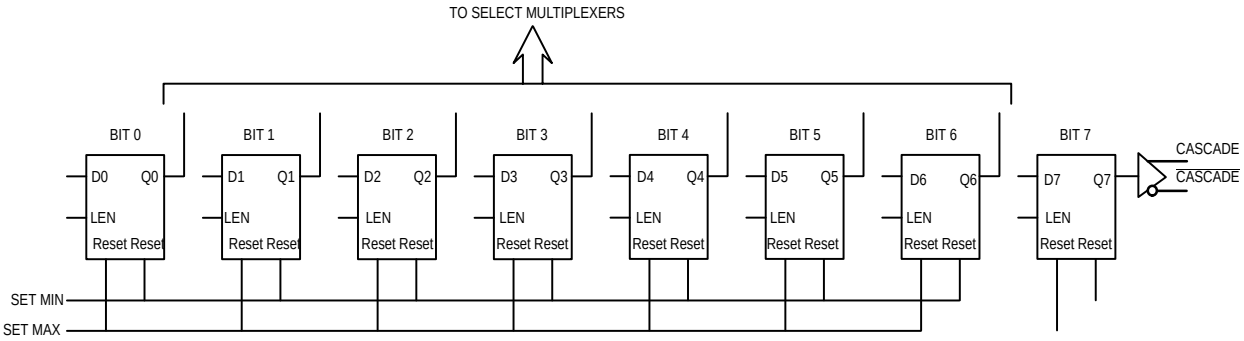


Figure 2. Expansion of the Latch Section of the E195 Block Diagram

OUTLINE DIMENSIONS

TBD SUFFIX
PLASTIC PACKAGE
CASE TBD

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