AK5393

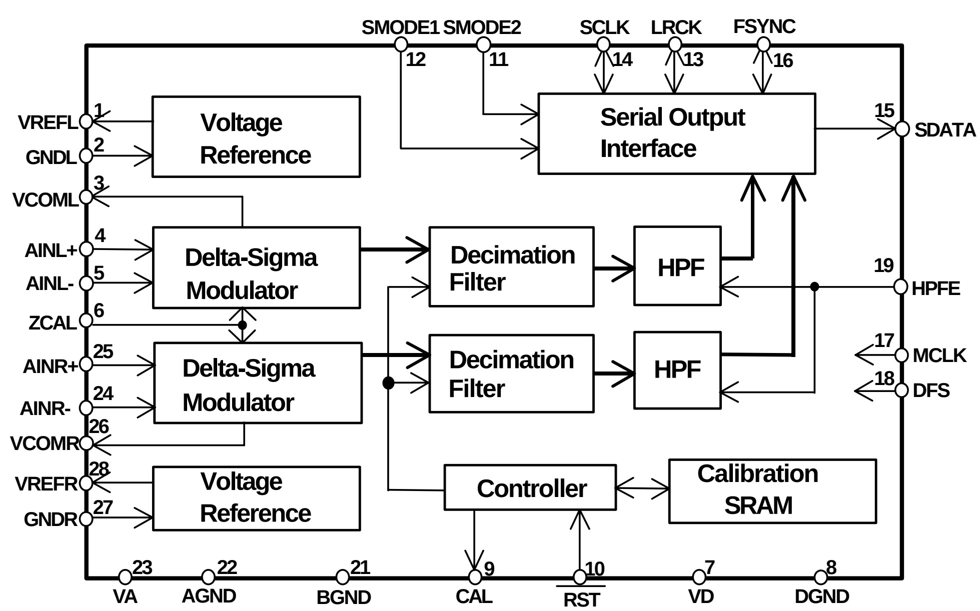
Enhanced Dual Bit ΔΣ 96kHz 24-Bit ADC

GENERAL DESCRIPTION

The AK5393 is a 24bit, 128x oversampling 2ch A/D Converter for professional digital audio systems. The modulator in the AK5393 uses the new developed Enhanced Dual Bit architecture. This new architecture achieves the wide dynamic range, while keeping much the same superior distortion characteristics as conventional Single Bit way. The AK5393 performs 117dB dynamic range, so the device is suitable for professional studio equipment such as digital mixer, digital VTR etc.

FEATURES

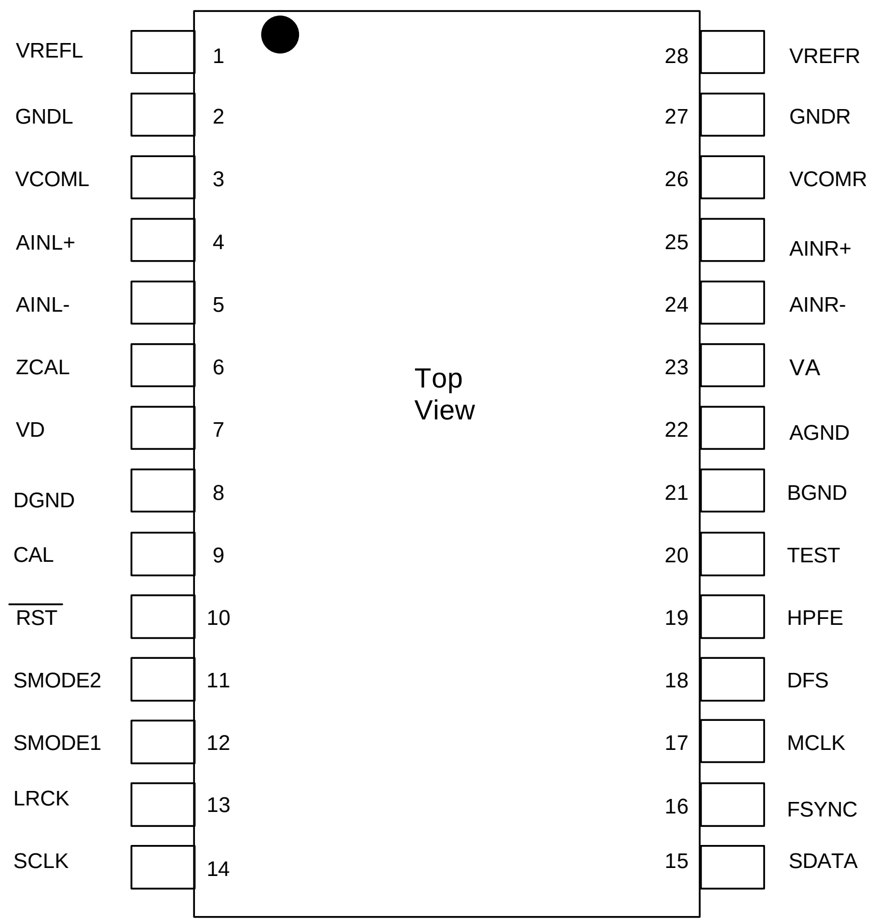
- **Enhanced Dual Bit ADC**
- **Sampling Rate: 1kHz~108kHz**
- **Full Differential Inputs**
- **S/(N+D): 105dB**
- **DR: 117dB**
- **S/N: 117dB**
- **High Performance Linear Phase Digital Anti-Alias filter**
  - **Passband: 0~21.768kHz(@fs=48kHz)**
  - **Ripple: 0.001dB**
  - **Stopband: 110dB**
- **Digital HPF & Offset Calibration for Offset Cancel**
- **Power Supply: 5V±5%(Analog), 3~5.25V(Digital)**
- **Power Dissipation: 470mW**
- **Package: 28pin SOP**
- **AK5392 Pin compatible**



■ Ordering Guide

AK5393-VS –10 ~ +70°C 28pin SOP
AKD5393 AK5393 Evaluation Board

■ Pin Layout



■ Compatibility with AK5392

	AK5392	AK5393
Pin 18	CMODE	DFS
fs (max)	54kHz	108kHz
MCLK (DFS ="L"@fs=48kHz)	256fs/384fs	256fs
MCLK (DFS ="H"@fs=96kHz)	N/A	128fs

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VREFL	O	Lch Reference Voltage Pin, 3.75V Normally connected to GNDL with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.
2	GNDL	-	Lch Reference Ground Pin, 0V
3	VCOML	O	Lch Common Voltage Pin, 2.75V
4	AINL+	I	Lch Analog positive input Pin
5	AINL-	I	Lch Analog negative input Pin
6	ZCAL	I	Zero Calibration Control Pin This pin controls the calibration reference signal. "L" :VCOML and VCOMR "H" : Analog Input Pins (AINL±, AINR±)
7	VD	-	Digital Power Supply Pin, 3.3V
8	DGND	-	Digital Ground Pin, 0V
9	CAL	O	Calibration Active Signal Pin "H" means the offset calibration cycle is in progress. Offset calibration starts when $\overline{\text{RST}}$ goes "H". CAL goes "L" after 8704 LRCK cycles for DFS="L", 17408 LRCK cycles for DFS ="H".
10	$\overline{\text{RST}}$	I	Reset Pin When "L", Digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.
11 12	SMODE2 SMODE1	I I	Serial Interface Mode Select Pin MSB first, 2's compliment. SMODE2 SMODE1 MODE LRCK L L Slave mode : MSB justified : H/L L H Master mode : Similar to I^2S : H/L H L Slave mode : I^2S : L/H H H Master mode : I^2S : L/H
13	LRCK	I/O	Left/Right Channel Select Clock Pin LRCK goes "H" at SMODE2="L" and "L" at SMODE2="H" during reset when SMODE1 "H".

14	SCLK	I/O	Serial Data Clock Pin Data is clocked out on the falling edge of SCLK. Slave mode: SCLK requires more than 48fs clock. Master mode: SCLK outputs a 128fs(DFS="L") or 64fs(DFS="H") clock. SCLK stays "L" during reset.
15	SDATA	O	Serial Data Output Pin MSB first, 2's complement. SDATA stays "L" during reset.
16	FSYNC	I/O	Frame Synchronization Signal Pin Slave mode: When "H", the data bits are clocked out on SDATA. In I^2S mode, FSYNC is don't care. Master mode: FSYNC outputs 2fs clock. FSYNC stays "L" during reset.
17	MCLK	I	Master Clock Input Pin 256fs at DFS="L", 128fs at DFS="H".
18	DFS	I	Double Speed Sampling Mode Pin "L": Normal Speed "H": Double Speed
19	HPFE	I	High Pass Filter Enable Pin "L": Disable "H": Enable
20	TEST	I	Test Pin (pull-down pin) Should be connected to GND.
21	BGND	-	Substrate Ground Pin, 0V
22	AGND	-	Analog Ground Pin, 0V
23	VA	-	Analog Supply Pin, 5V
24	AINR-	I	Rch Analog negative input Pin
25	AINR+	I	Rch Analog positive input Pin
26	VCOMR	O	Rch Common Voltage Pin, 2.75V
27	GNDR	-	Rch Reference Ground Pin, 0V
28	VREFR	O	Rch Reference Voltage Pin, 3.75V Normally connected to GNDR with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor

Note: All digital inputs should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	VA	-0.3	6.0	V
Digital	VD	-0.3	6.0	V
|BGND-DGND| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Analog Input Voltage	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Notes: 1. All voltages with respect to ground.
2. AGND, BGND and DGND must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,BGND,DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	VA	4.75	5.0	5.25	V
(Note 3) Digital	VD	3.0	3.3	5.25	V

Notes: 1. All voltages with respect to ground.
3. The power up sequence between VA and VD is not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=5.0V; VD=3.3V; AGND,BGND,DGND=0V; fs=48kHz; Signal Frequency=1kHz; 24bit Output; Measurement frequency=10Hz~20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Analog Input Characteristics:						
S/(N+D)	fs=48kHz	-1dBFS	98	105		dB
		-20dBFS	-	94		dB
		-60dBFS	-	54		dB
	fs=96kHz BW=40kHz	-1dBFS	96	103		dB
		-20dBFS	-	85		dB
		-60dBFS	-	45		dB
Dynamic Range (-60dBFS with A-Weighted)			112	117		dB
S/N (A-Weighted)			112	117		dB
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift					150	ppm/°C
Offset Error	after calibration, HPF=OFF			±200	±1000	LSB_{24}
	after calibration, HPF=ON			±1		LSB_{24}
Offset Drift (HPF=OFF)			-	±10	-	LSB_{24}/°C
Offset Calibration Range (HPF=OFF)				±50		mV
Input Voltage (AIN+)-(AIN-)			±2.3	±2.45	±2.6	V
Input Impedance			2.4	4		kΩ
Power Supplies						
Power Supply Current						
VA				90	130	mA
VD (fs=48kHz; DFS="L")				6	9	mA
(fs=96kHz; DFS="H")				9	14	mA
Power Dissipation				470	680	mW
Power Supply Rejection (Note 4)				70		dB

Note: 4. DC to 26kHz. 110dB(typ) beyond 26kHz.

FILTER CHARACTERISTICS(fs=48kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; fs=48kHz, DFS="L")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband (Note 5)		PB	0		21.768	kHz
Stopband (Note 5)		SB	26.232			kHz
Passband Ripple		PR			±0.001	dB
Stopband Attenuation (Note 6)		SA	110			dB
Group Delay Distortion		ΔGD		0		us
Group Delay (Note 7)		GD		38.7		1/fs
ADC Digital Filter(HPF):						
Frequency response (Note 5)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz

FILTER CHARACTERISTICS(fs=96kHz)

(Ta=25°C; VA=5.0V±5%; VD=3.0~5.25V; fs=96kHz, DFS="H")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband (Note 5)		PB	0		43.536	kHz
Stopband (Note 5)		SB	52.464			kHz
Passband Ripple		PR			±0.003	dB
Stopband Attenuation (Note 8)		SA	110			dB
Group Delay Distortion		ΔGD		0		us
Group Delay (Note 7)		GD		38.8		1/fs
ADC Digital Filter(HPF):						
Frequency response (Note 5)	-3dB	FR		2.0		Hz
	-0.1dB			13.0		Hz

Notes: 5. The passband and stopband frequencies scale with fs.

6. The analog modulator samples the input at 6.144MHz for an output word rate of 48kHz.
There is no rejection of input signals which are multiples of the sampling frequency
(that is: there is no rejection for n x 6.144MHz ± 21.768kHz, where n=1,2,3···).

7. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register.
40.7/fs(DFS="L"),40.8/fs(DFS="H")typ. at HPF:ON.

8. The analog modulator samples the input at 6.144MHz for an output word rate of 96kHz.
There is no rejection of input signals which are multiples of the sampling frequency
(that is: there is no rejection for n x 6.144MHz ± 43.536kHz, where n=1,2,3···).

DIGITAL CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage Iout=-20μA	VOH	VD-0.1	-	-	V
Low-Level Output Voltage Iout=20μA	VOL	-		0.1	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=5.0V±5%; VD=3.0 ~ 5.25V; C_L=20pF)

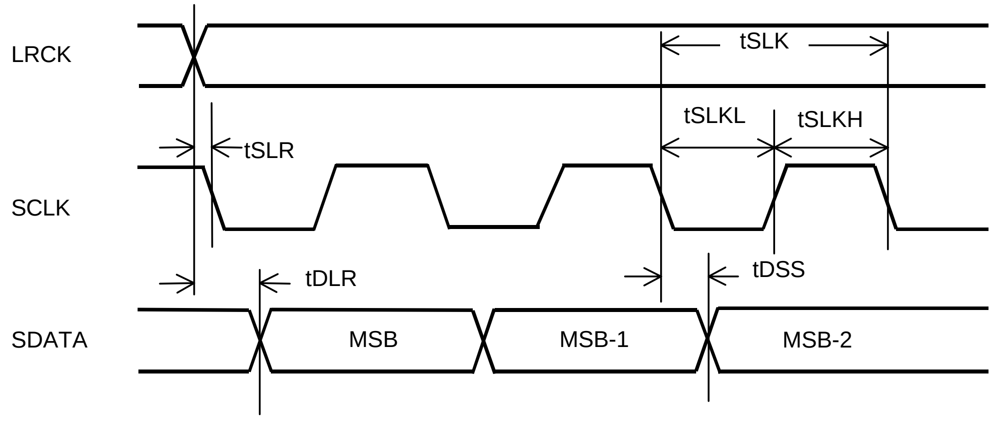
Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock 256fs:	fCLK	0.256	12.288	13.824	MHz
Pulse width Low	tCLKL	29			ns
Pulse width High	tCLKH	29			ns
Serial Data Output Clock (SCLK)	fSLK		6.144	6.912	MHz
Channel Select Clock (LRCK)	fs	1	48	108	kHz
duty cycle		25		75	%
Serial Interface Timing (Note 9)					
Slave Mode(SMODE1="L")					
SCLK Period	tSLK	144.7			ns
SCLK Pulse width Low	tSLKL	65			ns
Pulse width High	tSLKH	65			ns
SCLK falling to LRCK Edge (Note 10)	tSLR	-45		45	ns
LRCK Edge to SDATA MSB Valid	tDLR			45	ns
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-45		45	ns
Master Mode(SMODE1="H")					
SCLK Frequency (DFS="L")	fSLK		128fs		Hz
SCLK Frequency (DFS="H")	fSLK		64fs		Hz
duty cycle			50		%
FSYNC Frequency	fFSYNC		2fs		Hz
duty cycle			50		%
SCLK falling to LRCK Edge	tSLR	-20		20	ns
LRCK Edge to FSYNC rising	tLRF		1		tslk
SCLK falling to SDATA Valid	tDSS			45	ns
SCLK falling to FSYNC Edge	tSF	-20		20	ns
Reset/Calibration timing					
$\overline{RST}$ Pulse width	tRTW	150			ns
$\overline{RST}$ falling to CAL rising	tRCR			50	ns
$\overline{RST}$ rising to CAL falling (Note 11)	tRCF		8704		1/fs
$\overline{RST}$ rising to SDATA Valid (Note 11)	tRTV		8960		1/fs

Notes: 9. Refer to Serial Data interface.

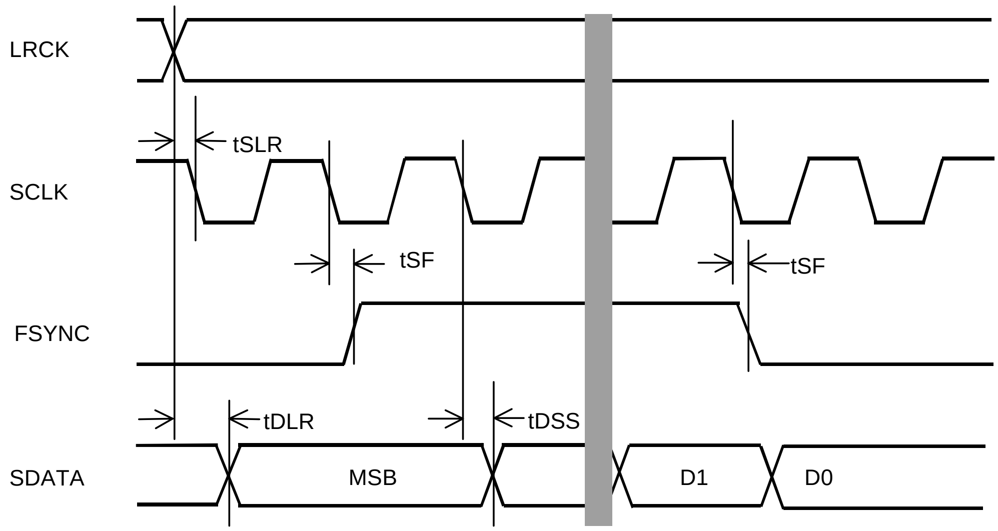
10. Specified LRCK edges not to coincide with the rising edges of SCLK.

11. The number of the LRCK rising edges after $\overline{RST}$ brought high at DFS="L". The value is in master mode. In slave mode it becomes one LRCK clock(1/fs) longer. When DFS="H", tRCF=17408 and tRTV=17920.

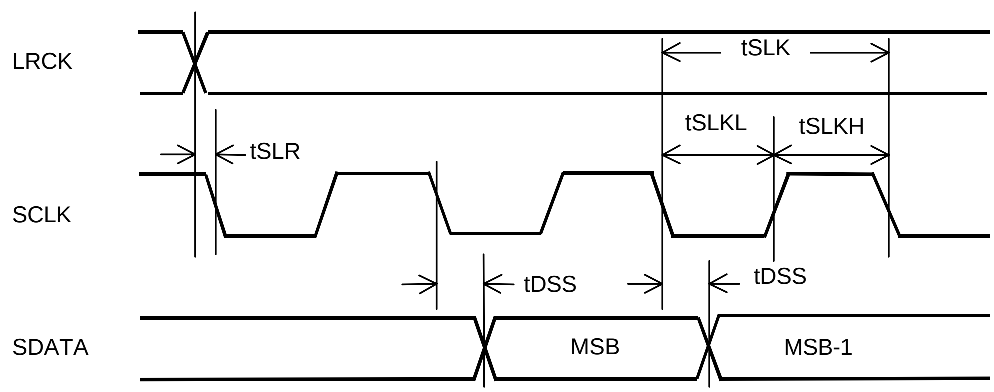
■ Timing Diagram



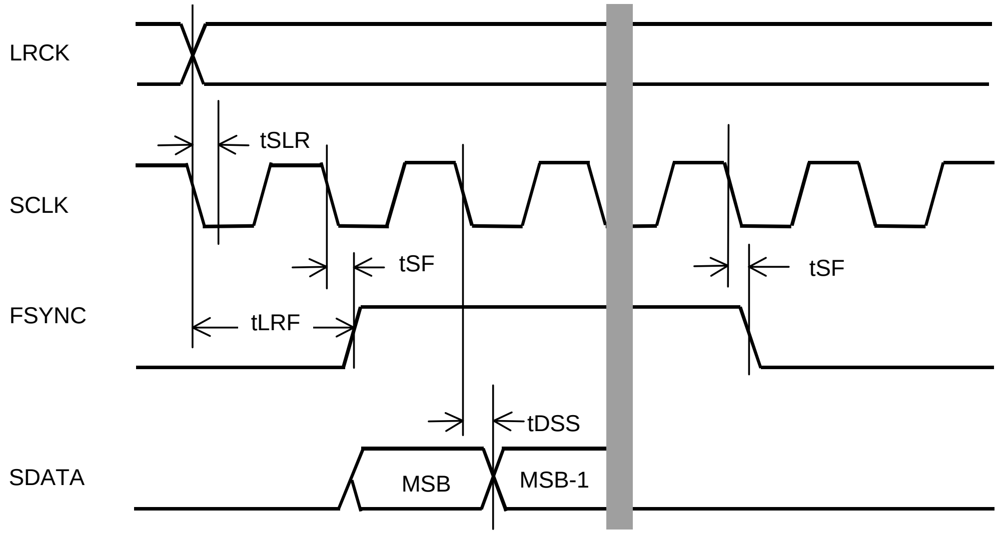
Serial Data Timing (Slave Mode, FSYNC="H")



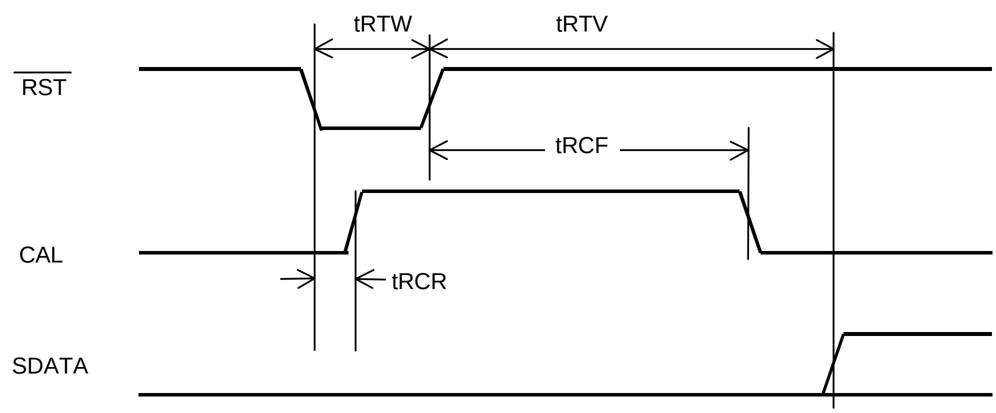
Serial Data Timing (Slave Mode)



Serial Data Timing (I^2S Slave Mode, FSYNC = Don't Care)



Serial Data Timing (Master Mode & I^2S Master Mode, DFS ="L")



Reset & Calibration Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK5393 are MCLK, LRCK(fs), SCLK. MCLK should be synchronized with LRCK but the phase is free of care. MCLK should be 256fs in normal sampling mode(DFS="L") and double sampling mode needs 128fs as MCLK. Table 2 illustrates standard audio word rates and corresponding frequencies used in the AK5393.

As the AK5393 includes the phase detect circuit for LRCK, the AK5393 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is only needed for power-up.

All external clocks must be present unless $\overline{\text{RST}}$ ="L", otherwise excessive current may result from abnormal operation of internal dynamic logic.

Speed	Normal(DFS ="L")	Double(DFS ="H")
LRCK (max)	54kHz	108kHz
SCLK	~128fs	~64fs
MCLK	256fs	128fs

Table 1. System Clocks

fs	MCLK	SCLK
32.0kHz	8.1920MHz	4.0960MHz
44.1kHz	11.2896MHz	5.6448MHz
48.0kHz	12.2880MHz	6.1440MHz
96.0kHz	12.2880MHz	6.1440MHz

Table 2. Examples of System Clock Frequency

■ Serial Data Interface

The AK5393 supports four serial data formats which can be selected via SMODE1 and SMODE2 pins(Table 3). The data format is MSB-first, 2's complement.

Figure	SMODE2	SMODE1	Mode	LRCK
Figure 1	L	L	Slave Mode	Lch = H, Rch =L
Figure 2	L	H	Master Mode	Lch =H, Rch =L
Figure 3	H	L	I^2S Slave Mode	Lch =L, Rch =H
Figure 4	H	H	I^2S Master Mode	Lch =L, Rch =H

Table 3. Serial I/F Format

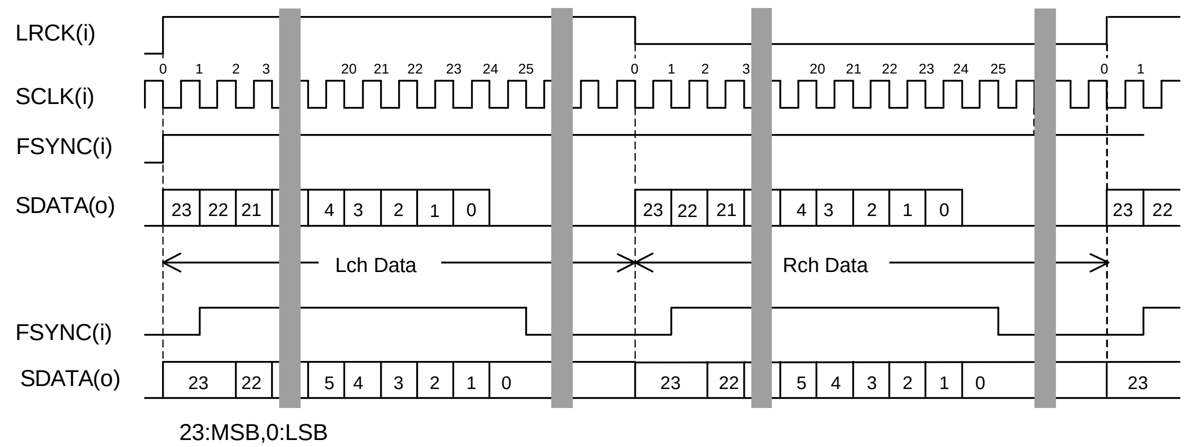


Figure 1. Serial Data Timing (Slave Mode)

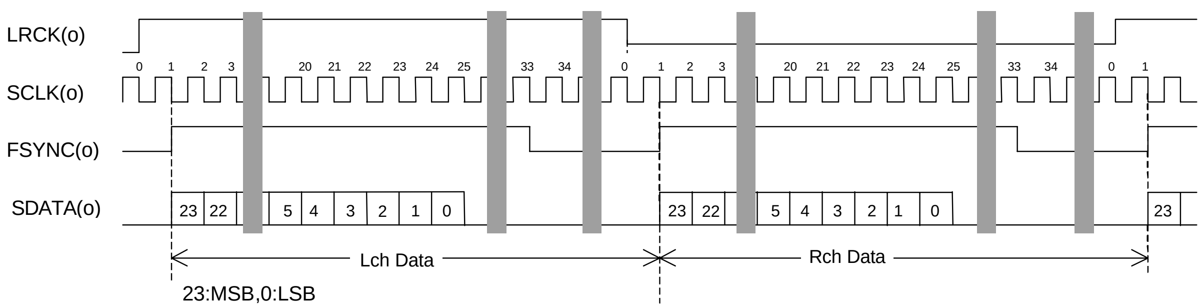


Figure 2. Serial Data Timing (Master mode, DFS="L")

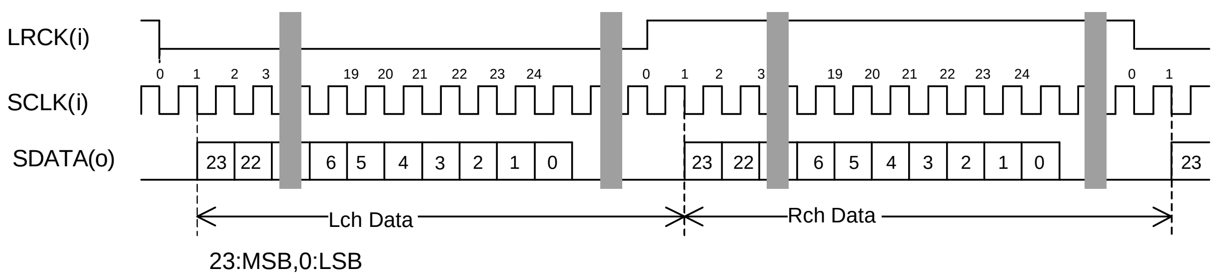


Figure 3. Serial Data Timing (I^2S Slave mode, FSYNC: Don’t care.)

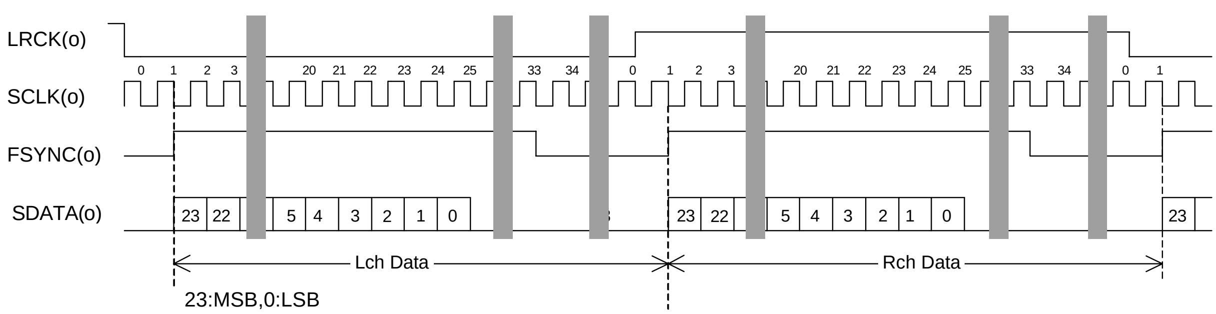


Figure 4. Serial Data Timing (I^2S Master mode, DFS="L")

■ Offset Calibration

When $\overline{\text{RST}}$ pin goes to "L", the digital section is powered-down. Upon returning "H", an offset calibration cycle is started. An offset calibration cycle should always be initiated after power-up.

During the offset calibration cycle, the digital section of the part measures and stores the values of calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AIN+/-) or the VCOM pins depending on the state of the ZCAL pin. With ZCAL "H", the analog input pin voltages are measured, and with ZCAL "L", the VCOM pin voltages are measured. The CAL output is "H" during calibration.

■ Digital High Pass Filter

The AK5393 also has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 1Hz at fs=48kHz and also scales with sampling rate(fs).

SYSTEM DESIGN

Figure 5 and 6 show the system connection diagram. An evaluation board[AKD5393] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

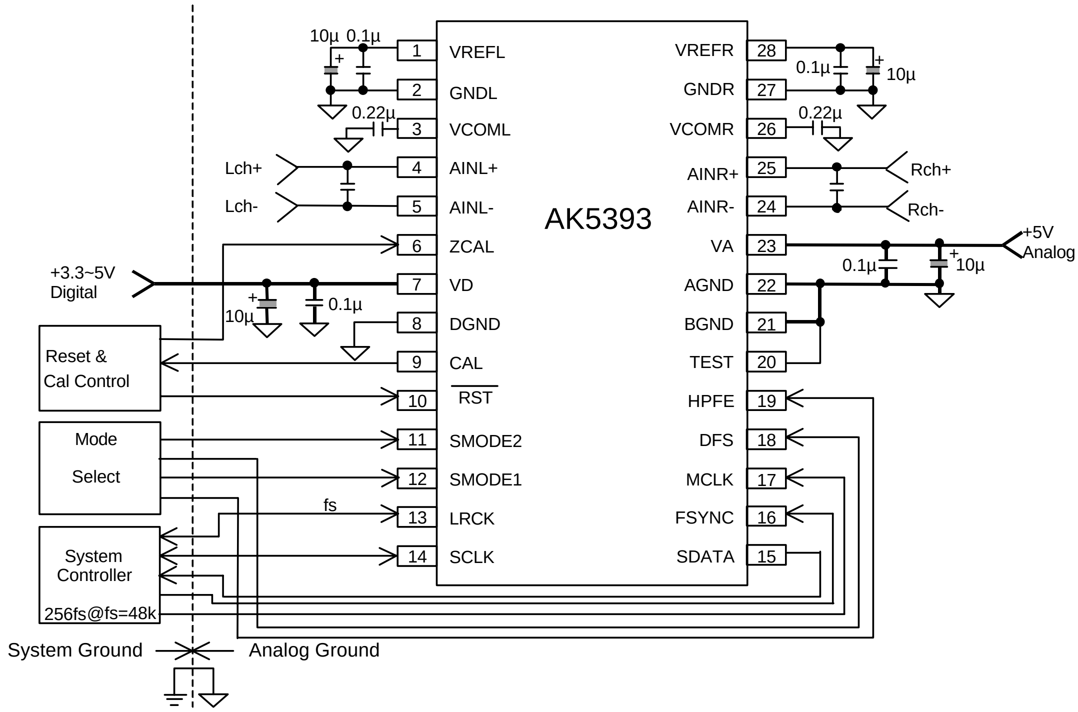


Figure 5. Typical Connection Diagram

Notes:
- LRCK = fs, SCLK=64fs.
- Power lines of VA and VD should be distributed separately from the point with low impedance of regulator etc.
- GND, BGND and DGND must be connected to the same analog ground plane.
- All input pins except pull-down/pull-up pins should not be left floating.

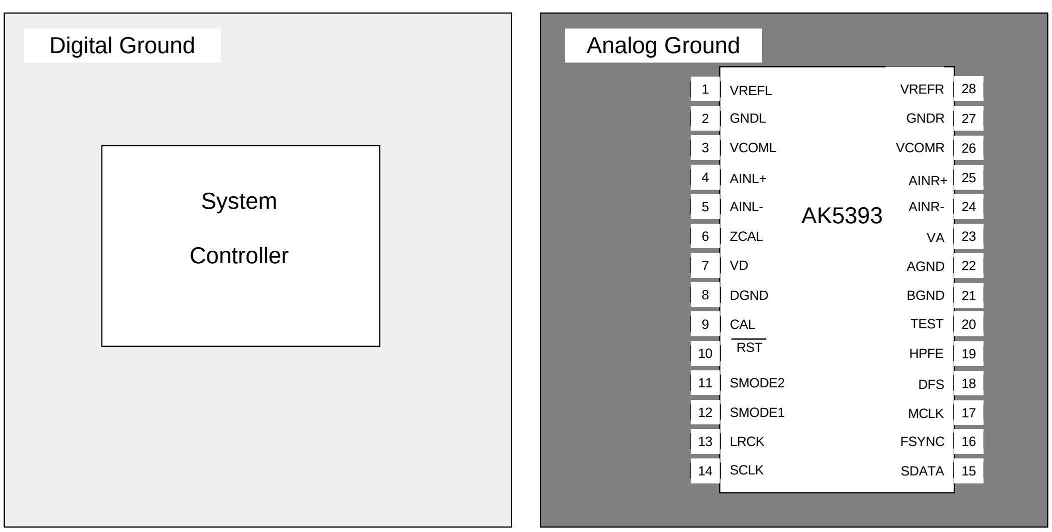


Figure 6 Ground layout

1. Grounding and Power Supply Decoupling

The AK5393 requires careful attention to power supply and grounding arrangements. Analog ground and digital ground should be separate and connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5393 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference and VCOM

The reference voltage for A/D converter is a differential voltage between the VREFL/R output voltage and the GNDL/R input voltage. The GNDL/R are connected to AGND and a 10µF electrolytic capacitor parallel with a 0.1µF ceramic capacitor between the VREFL/R and the GNDL/R eliminate the effects of high frequency noise. Especially a ceramic capacitor should be as near to the pins as possible. And all digital signals, especially clocks, should be kept away from the VREFL/R pins in order to avoid unwanted coupling into the AK5393. No load current may be taken from the VREFL/R pins.

VCOM is a common voltage of the analog signal. In order to eliminate the effects of high frequency noise, a 0.22µF ceramic capacitor should be connected as near to the VCOM pin as possible. And all signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5393. No load current may be drawn from the VCOM pin.

3. Analog Inputs

Analog signal is differentially input into the modulator via the AIN+ and the AIN- pins. The input voltage is the difference between AIN+ and AIN- pins. The full-scale of each pin is nominally ± 2.45Vpp(typ). The AK5393 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative full scale. The ideal code is 000000H (@24bit) with no input signal. The DC offset is removed by the offset calibration.

The AK5393 samples the analog inputs at 128fs(6.144MHz @fs=48kHz,DFS="L"). The digital filter rejects noise above the stop band except for multiples of 128fs. A simple RC filter may be used to attenuate any noise around 128fs and most audio signals do not have significant energy at 128fs.

The AK5393 accepts +5V supply voltage. Any voltage which exceeds the upper limit of VA+0.3V and lower limit of AGND-0.3V and any current beyond 10mA for the analog input pins(AIN+ /-) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ±15V in other analog circuits.

Figure 7shows an input buffer circuit example 1. This is a full-differential input buffer circuit with an inverted-amp (gain :-10dB). The capacitor of 10nF between AIN+ /- decreases the clock feed through noise of modulator, and composes a 1st order LPF(fc=360kHz) with 22ohm resistor before the capacitor. This circuit also has a 1st order LPF(fc=370kHz) composed of op-amp. In this example, the internal offset is removed by self calibration. The evaluation board should be referred about the detail.

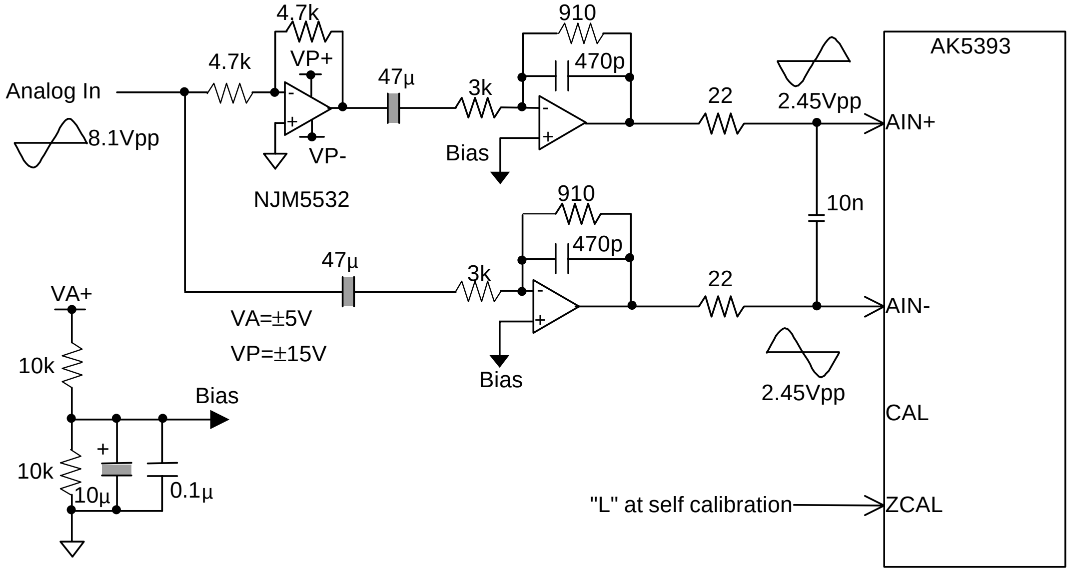


Figure 7 Differential Input Buffer Example 1

Figure 8 shows an input buffer circuit example 2. (1st order HPF; fc=0.66Hz, Table 4, 1st order LPF; fc=590kHz, gain=-14dB, Table 5). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is +/-12.4Vpp (AK5393: +/-2.45Vpp Typ.).

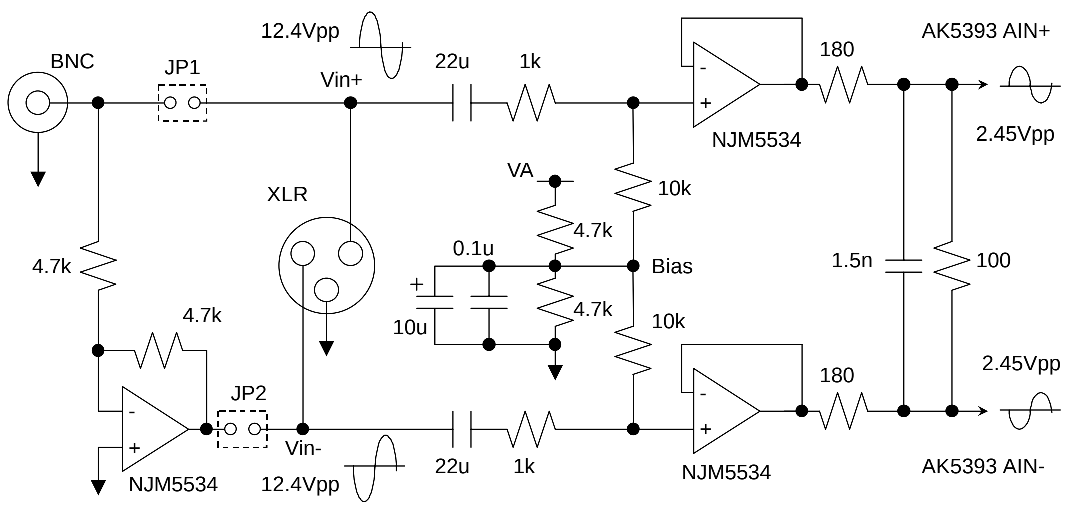


Figure 8 Differential Input Buffer Example 2

fin	1Hz	10Hz
Frequency Response	-1.56dB	-0.02dB

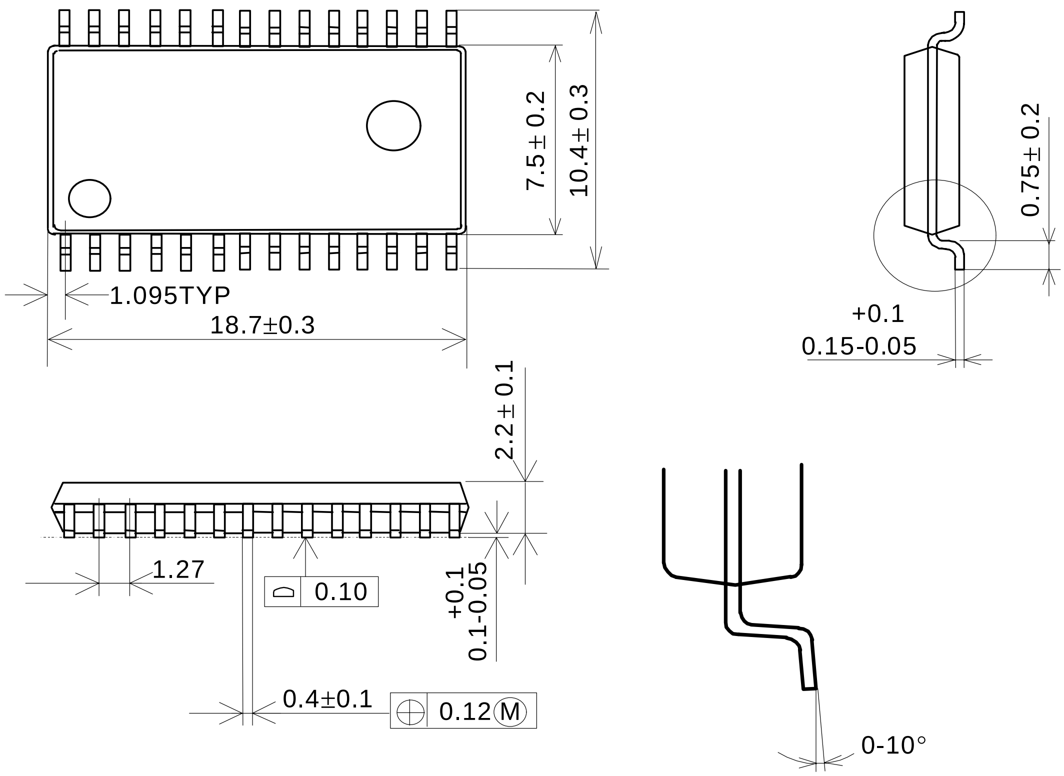
Table 4. Frequency Response of HPF

fin	20kHz	40kHz	6.144MHz
Frequency Response	-0.005dB	-0.02dB	-15.6dB

Table 5. Frequency Response of LPF

PACKAGE

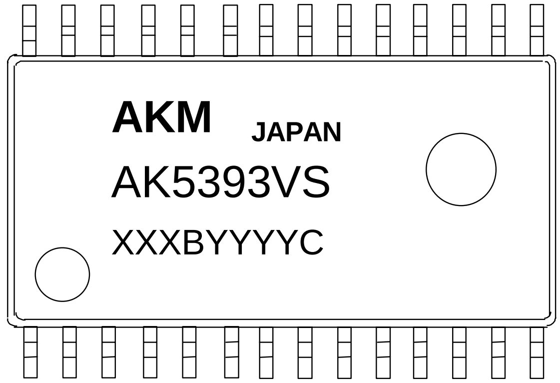
28pin SOP (Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of XXXBYYYYC

XXXB: Lot # (X : numbers, B : alphabet)
YYYYC: Data Code (Y : numbers, C : alphabet)