

T-29-27



2N5452-2N5454

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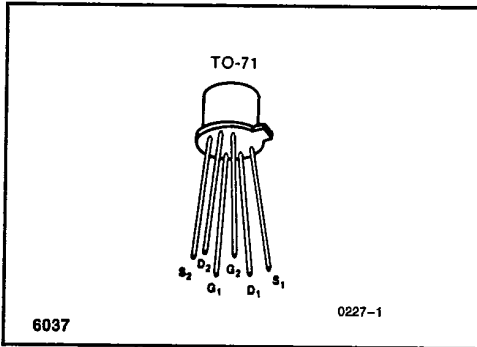
## Dual N-Channel JFET

### General Purpose Amplifier

#### GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

#### PIN CONFIGURATION



#### FEATURES

- Low Offset Voltage
- Low Drift
- Low Capacitance
- Low Output Conductance

#### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)  
 Gate-Source or Gate Drain Voltage  
 (Note 1) ..... -50V  
 Gate Current (Note 1) ..... 50mA  
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+200^\circ\text{C}$   
 Operating Temperature Range .....  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead Temperature (Soldering, 10sec) .....  $+300^\circ\text{C}$

	One Side	Both Sides
Power Dissipation ( $T_C = 85^\circ\text{C}$ ) ..	250mW	500mW
Derate above $25^\circ\text{C}$ .....	2.9mW/ $^\circ\text{C}$	4.3mW/ $^\circ\text{C}$

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ORDERING INFORMATION

TO-71
2N5452
2N5453
2N5454

#### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5452		2N5453		2N5454		Units
			Min	Max	Min	Max	Min	Max	
$I_{GSS}$	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-100		-100		-100	pA
				-200		-200		-200	nA
$BV_{GSS}$	Gate-Source Breakdown Voltage	$V_{DS} = 0, I_G = -1\mu\text{A}$	-50		-50		-50		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_D = 1\text{nA}$	-1	-4.5	-1	-4.5	-1	-4.5	V
$V_{GS}$	Gate-Source Voltage	$V_{DS} = 20V, I_D = 50\mu\text{A}$	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2	
$V_{GS(f)}$	Gate-Source Forward Voltage	$V_{DS} = 0, I_G = 1\text{mA}$		2		2		2	
$I_{DSS}$	Saturation Drain Current	$V_{DS} = 20V, V_{GS} = 0$	0.5	5.0	0.5	5.0	0.5	5.0	mA

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NOTE: All typical values have been characterized but are not tested.

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## ELECTRICAL CHARACTERISTICS (Continued) (T<sub>A</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5452		2N5453		2N5454		Units	
			Min	Max	Min	Max	Min	Max		
g <sub>fs</sub>	Common-Source Forward Transconductance (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 1kHz	1000	3000	1000	3000	1000	3000	μs
			f = 100MHz	1000		1000		1000		
g <sub>os</sub>	Common-Source Output Conductance	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA	f = 1kHz		3.0		3.0		3.0	μs
					1.0		1.0		1.0	
C <sub>iss</sub>	Common-Source Input Capacitance (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		4.0		4.0		4.0	pF	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 1MHz		1.2		1.2	1.2		
C <sub>dgo</sub>	Drain-Gate Capacitance (Note 2)		V <sub>DG</sub> = 10V, I <sub>S</sub> = 0		1.5		1.5	1.5		
e <sub>n</sub>	Equivalent Short Circuit Input Noise Voltage	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 1kHz		20		20	20	nV √Hz	
NF	Common-Source Spot Noise Figure (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0 R <sub>G</sub> = 10MΩ	f = 100Hz		0.5		0.5	0.5	dB	
I <sub>DSS1</sub> /I <sub>DSS2</sub>	Drain Saturation Current Ratio	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		0.95	1.0	0.95	1.0	0.95	1.0	
V <sub>GS1</sub> -V <sub>GS2</sub>	Differential Gate-Source Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA			5.0		10.0		15.0	mV
Δ V <sub>GS1</sub> -V <sub>GS2</sub>   ΔT	Gate-Source Voltage Differential Change with Temperature		T = 25°C to -55°C		0.4		0.8		2.0	
			T = 25°C to +125°C		0.5		1.0		2.5	
g <sub>fs1</sub> /g <sub>fs2</sub>	Transconductance Ratio		f = 1kHz	0.97	1.0	0.97	1.0	0.95	1.0	
g <sub>os1</sub> -g <sub>os2</sub>	Differential Output Conductance				0.25		0.25		0.25	μs

NOTES: 1. Per transistor.  
2. For design reference only, not 100% tested.

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