

TJA1080

FlexRay transceiver

Rev. 01 — 20 July 2006

Preliminary data sheet

1. General description

The TJA1080 is a FlexRay transceiver, which is compatible with the FlexRay electrical physical layer specification V2.1 Rev. A (see [Ref. 1](#)). It is primarily intended for communication systems from 1 Mbit/s to 10 Mbit/s, and provides an advanced interface between the protocol controller and the physical bus in a FlexRay network.

The TJA1080 can be configured to be used as an active star transceiver or as a node transceiver.

The TJA1080 provides differential transmit capability to the network and differential receive capability to the FlexRay controller. It offers excellent EMC performance as well as high ESD protection.

The TJA1080 actively monitors the system performance using dedicated error and status information (readable by any microcontroller), as well as internal voltage and temperature monitoring.

The TJA1080 supports the mode control as used in Philips TJA1054 (see [Ref. 2](#)) and TJA1041 (see [Ref. 3](#)) CAN transceivers.

2. Features

2.1 Optimized for time triggered communication systems

- Data transfer up to 10 Mbit/s
- Usable for 14 V and 42 V powered systems
- Very low ElectroMagnetic Emission (EME) to support unshielded cable
- Differential receiver with high common-mode range for ElectroMagnetic Immunity (EMI)
- Transceiver can be used for small linear passive bus topologies as well as active star topologies
- Auto I/O level adaptation to host controller supply voltage V_{IO}
- Bus guardian interface included
- Automotive product qualification in accordance with AEC-Q100

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2.2 Low power management

- Low power management including two inhibit switches
- Very low current in Sleep and Standby mode
- Wake-up via wake-up symbol on the bus lines (remote), negative edge on pin WAKE (local), and a positive edge on pin STBN if V_{IO} is present
- Wake-up source recognition
- Automatic power-down (in star Sleep mode) in star configuration

2.3 Diagnosis (detection and signalling)

- Overtemperature detection
- Short-circuit on bus lines
- V_{BAT} power-on flag (first battery connection and cold start)
- Pin TXEN and pin BGE clamping
- Undervoltage detection on pins V_{BAT} , V_{CC} and V_{IO}
- Wake source indication

2.4 Protections

- Bus pins protected against 8 kV HBM ESD pulses
- Bus pins protected against transients in automotive environment (ISO 7637 class C compliant)
- Bus pins short-circuit proof to battery voltage (14 V and 42 V) and ground
- Fail-safe mode in case of an undervoltage on pins V_{BAT} , V_{CC} or V_{IO}
- Passive behavior of bus lines in the event that transceiver is not powered up

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	supply voltage on pin V_{BAT}	no time limit	-0.3	-	+60	V
		operating range	6.5	-	60	V
V_{CC}	supply voltage	no time limit	-0.3	-	+5.5	V
		operating range	4.75	-	5.25	V
V_{BUF}	supply voltage on pin V_{BUF}	no time limit	-0.3	-	+5.5	V
		operating range	4.75	-	5.25	V
V_{IO}	supply voltage on pin V_{IO}	no time limit	-0.3	-	+5.5	V
		operating range	2.2	-	5.25	V
V_{TRXD0}	voltage on pin TRXD0		-0.3		+5.5	V
V_{TRXD1}	voltage on pin TRXD1		-0.3		+5.5	V
V_{BP}	voltage on pin BP		-60	-	+60	V
V_{BM}	voltage on pin BM		-60	-	+60	V
I_{BAT}	supply current on pin V_{BAT}	low power modes in node configuration	-	35	50	μ A
		normal power modes	-	0.075	1	mA

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CC}	supply current	low power modes	-1	0	+5	μA
		Normal mode; V _{BGE} = 0 V; V _{TXEN} = V _{IO} ; Receive only mode; star Idle mode	-	10	15	mA
		Normal mode; V _{BGE} = V _{IO} ; V _{TXEN} = 0 V; V _{BUF} open	[1] -	28.5	35	mA
		Normal mode; V _{BGE} = V _{IO} ; V _{TXEN} = 0 V; R _{bus} = ∞ Ω	-	10	15	mA
		star Transmit mode	-	50	62	mA
		star Receive mode	-	38	42	mA
I _{IO}	supply current on pin V _{IO}	low power modes	-1	+1	+5	μA
		Normal and Receive only mode; V _{TXD} = V _{IO}	-	30	1000	μA
V _{OH(dif)}	differential HIGH-level output voltage	on pins BP and BM; 40 Ω < R _{bus} < 55 Ω; V _{CC} = V _{BUF} = 5 V	600	800	1200	mV
V _{OL(dif)}	differential LOW-level output voltage	on pins BP and BM; 40 Ω < R _{bus} < 55 Ω; V _{CC} = V _{BUF} = 5 V	-1200	-800	-600	mV
V _{IH(dif)}	differential HIGH-level input voltage	on pins BP and BM; normal power modes; -10 V < V _{BP} < +15 V; -10 V < V _{BM} < +15 V	150	225	300	mV
V _{IL(dif)}	differential LOW-level input voltage	on pins BP and BM; normal power modes; -10 V < V _{BP} < +15 V; -10 V < V _{BM} < +15 V	-300	-225	-150	mV
T _{vj}	virtual junction temperature		[2] -40	-	+150	°C

[1] Current flows from V_{CC} to V_{BUF}. This means that the maximum sum current I_{CC} + I_{BUF} is 35 mA.

[2] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature T_{vj} is: T_{vj} = T_{amb} + TD x R_{th(j-a)}, where R_{th(j-a)} is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

4. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
TJA1080TS/N	SSOP20	plastic shrink small outline package; 20 leads; body with 5.3 mm	SOT339-1

5. Block diagram

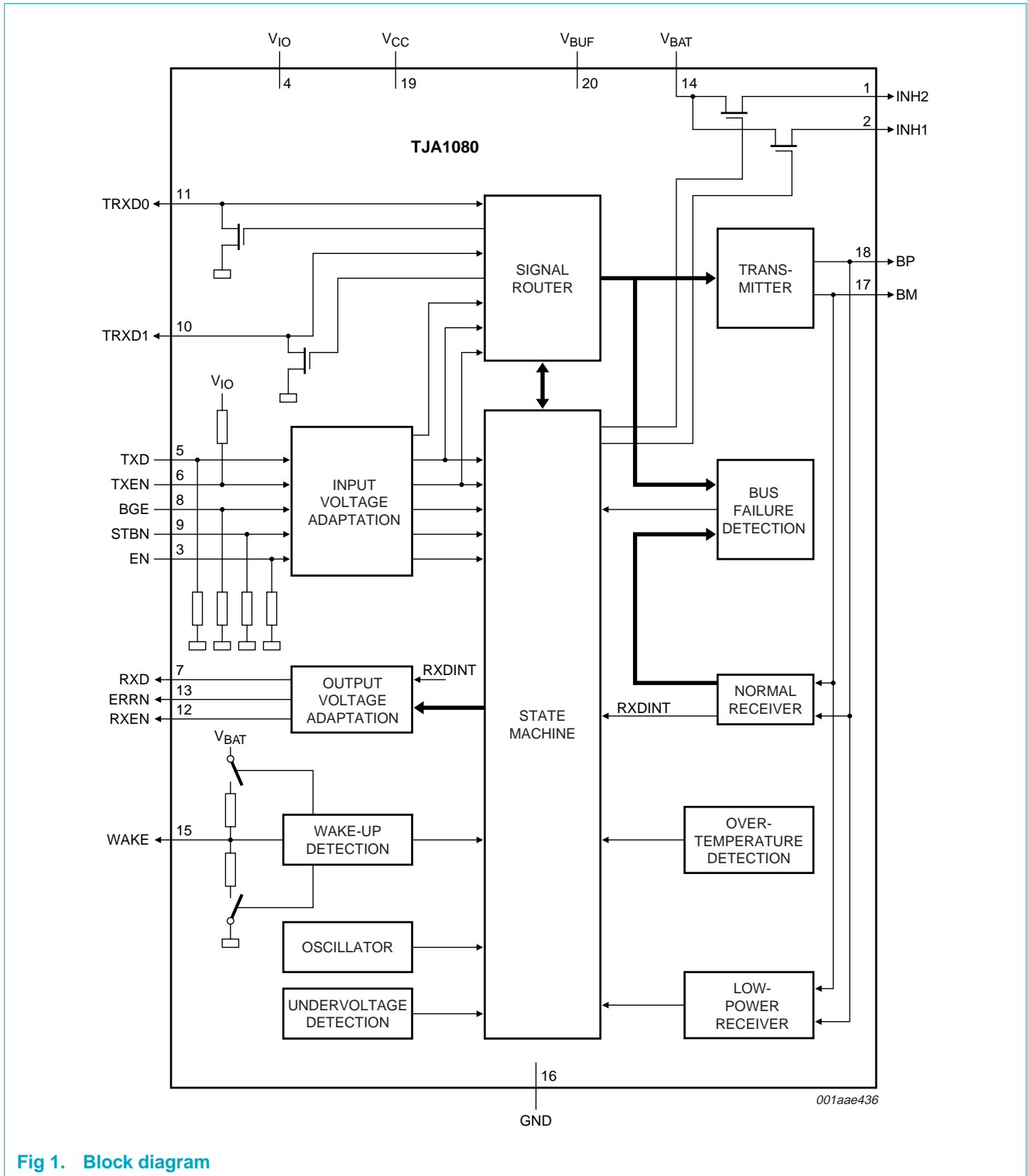
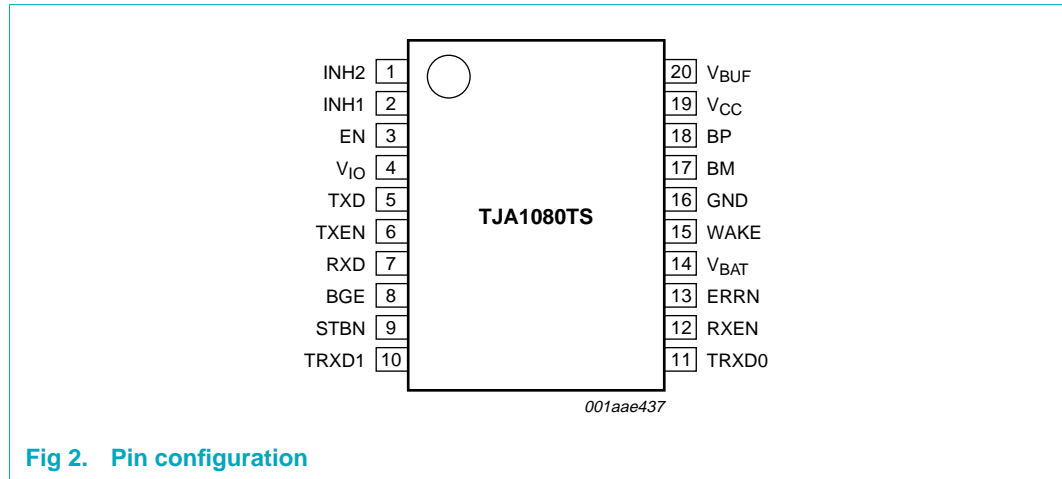


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
INH2	1	O	inhibit 2 output for switching external voltage regulator
INH1	2	O	inhibit 1 output for switching external voltage regulator
EN	3	I	enable input; when HIGH enabled; internal pull-down
V _{IO}	4	P	supply voltage for V _{IO} voltage level adaptation
TXD	5	I	transmit data input; internal pull-down
TXEN	6	I	transmitter enable input; when HIGH transmitter disabled; internal pull-up
RXD	7	O	receive data output
BGE	8	I	bus guardian enable input; when LOW transmitter disabled; internal pull-down
STBN	9	I	standby input; when LOW low power mode; internal pull-down
TRXD1	10	I/O	data bus line 1 for inner star connection
TRXD0	11	I/O	data bus line 0 for inner star connection
RXEN	12	O	receive data enable output; when LOW bus activity detected
ERRN	13	O	error diagnoses output; when LOW error detected
V _{BAT}	14	P	battery supply voltage
WAKE	15	I	local wake-up input; internal pull-up or pull-down (depends on voltage at pin WAKE)
GND	16	P	ground
BM	17	I/O	bus line minus
BP	18	I/O	bus line plus
V _{CC}	19	P	supply voltage (+5 V)
V _{BUF}	20	P	buffer supply voltage

7. Functional description

The block diagram of the total transceiver is illustrated in [Figure 1](#).

7.1 Operating configurations

7.1.1 Node configuration

In node configuration the transceiver operates as a stand-alone transceiver.

The transceiver can be configured as node by connecting pins TRXD0 and TRXD1 to ground during a power-on situation (PWON flag is set). The configuration will be latched when the PWON flag is reset.

The following operating modes are selectable:

- Normal: normal power mode
- Receive: normal power mode
- Standby: low power mode
- Go-to-sleep: low power mode
- Sleep: low power mode

7.1.2 Star configuration

In star configuration the transceiver operates as a branch of a FlexRay active star.

The transceiver can be configured as star by connecting pin TRXD0 or TRXD1 to V_{BUF} during a PWON situation (PWON flag is set). The configuration will be latched when the PWON flag is reset.

It is possible to redirect data from one branch to other branches via the inner bus. It is also possible to send data to all branches via pin TXD, if pins TXEN and BGE have the correct polarity.

The following operating modes are available:

- Star idle: normal power mode
- Star transmit: normal power mode
- Star receive: normal power mode
- Star sleep: low power mode
- Star standby: low power mode
- Star locked: normal power mode

In the star configuration all modes are autonomously controlled by the transceiver, except in the case of a wake-up.

7.1.3 Bus activity and idle detection

The following mechanisms for activity and idle detection are valid for node and star configurations in normal power modes:

- If the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$, then activity is detected on the bus lines and pin RXEN is switched to LOW which results in pin RXD being released
- If, after bus activity detection, the differential voltage on the bus lines is higher than $V_{IH(dif)}$, pin RXD will go HIGH
- If, after bus activity detection, the differential voltage on the bus lines is lower than $V_{IL(dif)}$, pin RXD will go LOW
- If the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$, then idle is detected on the bus lines and pin RXEN is switched to HIGH. This results in pin RXD being blocked (pin RXD is switched to HIGH or stays HIGH)

Additionally, in star configuration, activity and idle can be detected:

- If pin TXEN is LOW for longer than $t_{det(act)(TXEN)}$, activity is detected on pin TXEN
- If pin TXEN is HIGH for longer than $t_{det(idle)(TXEN)}$, idle is detected on pin TXEN
- If pin TRXD0 or TRXD1 is LOW for longer than $t_{det(act)(TRXD)}$, activity is detected on pins TRXD0 and TRXD1
- If pin TRXD0 or TRXD1 is HIGH for longer than $t_{det(idle)(TRXD)}$, idle is detected on pins TRXD0 and TRXD1

7.2 Operating modes in node configuration

The TJA1080 provides two control pins STBN and EN in order to select one of the modes of operation in node configuration. See [Table 4](#) for a detailed description of the pin signalling in node configuration, and [Figure 3](#) for the timing diagram.

All modes are directly controlled via pins EN and STBN unless an undervoltage situation is present.

If V_{IO} and (V_{BUF} or V_{BAT}) are within their operating range, pin ERRN indicates the error flag.

Table 4. Pin signalling in node configuration

Pin	Mode				
	Normal	Receive only	Go-to-sleep	Standby	Sleep
STBN	HIGH	HIGH	LOW	LOW	LOW
EN	HIGH	LOW	HIGH	LOW	X
ERRN	LOW: error flag set [3]		LOW: wake flag set [4]		
	HIGH: error flag set [3] [4]		HIGH: wake flag reset [4]		
RXEN	LOW: bus activity		LOW: wake flag set [4]		
	HIGH: bus idle		HIGH: wake flag reset [4]		
RXD	LOW: bus DATA_0		LOW: wake flag set [4]		
	HIGH: bus DATA_1 or idle		HIGH: wake flag reset [4]		

Table 4. Pin signalling in node configuration ...continued

Pin	Mode				
	Normal	Receive only	Go-to-sleep	Standby	Sleep
INH1	HIGH		HIGH	HIGH	float [4]
INH2	HIGH		float [5]	float [5]	float [4]
Transmitter	enabled	disabled [4]	disabled [4]		

[3] Pin ERRN provides a serial interface for retrieving diagnostic information.

[4] Valid if V_{IO} and V_{BUF} or V_{BAT} are present.

[5] If wake flag is not set.

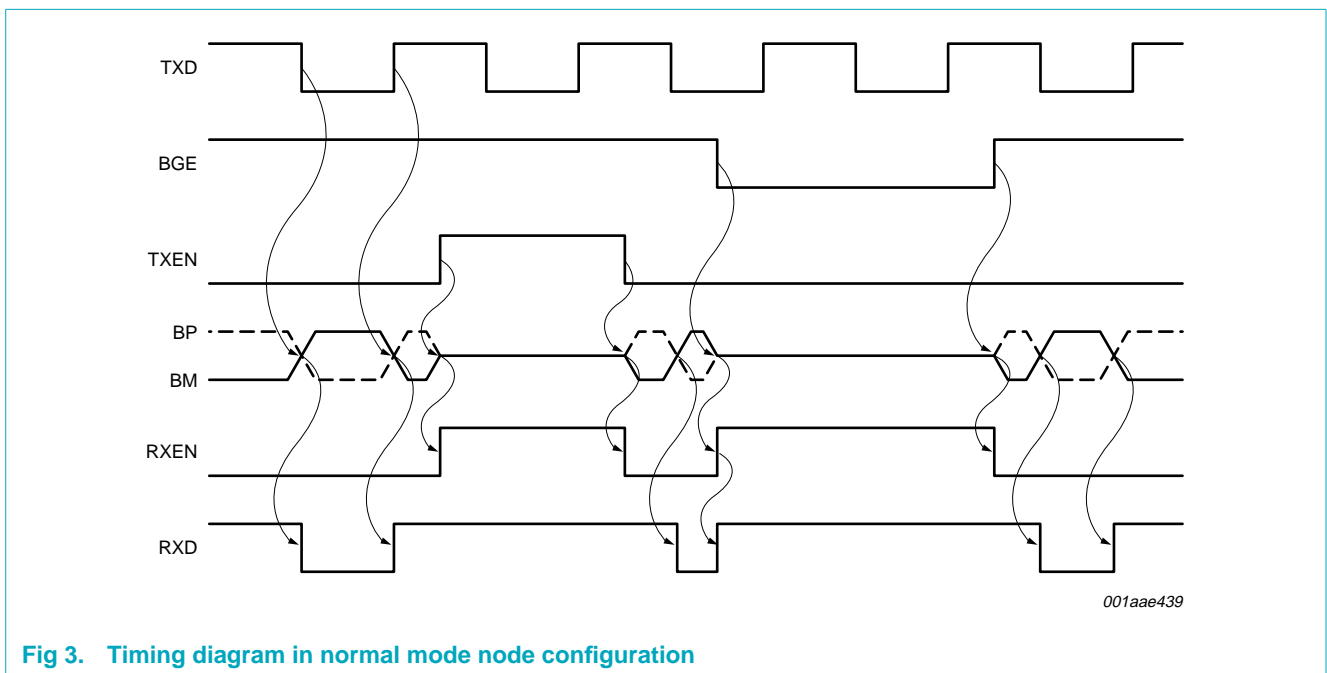
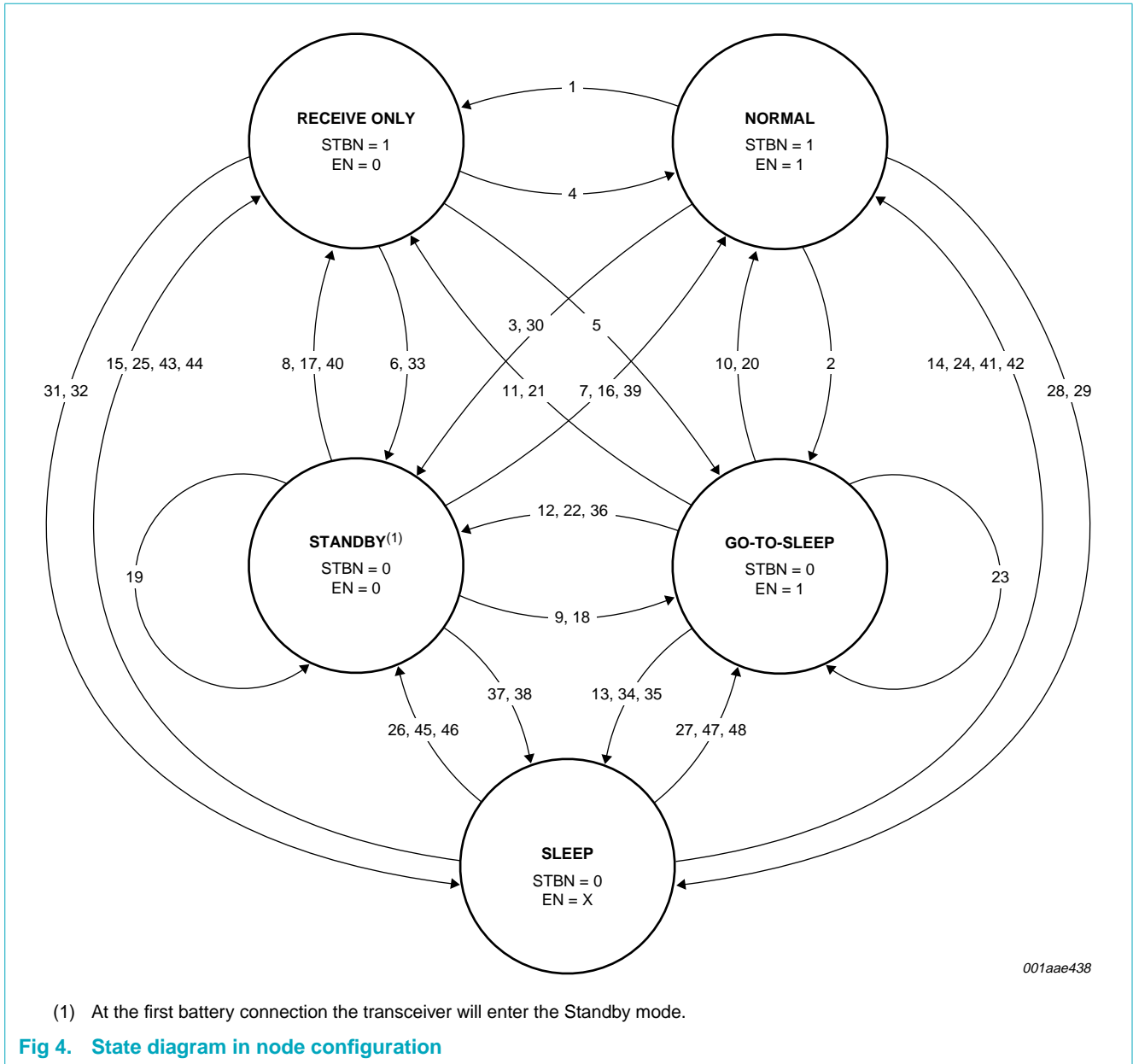


Fig 3. Timing diagram in normal mode node configuration

The state diagram in node configuration is illustrated in [Figure 4](#).



The state transitions are represented with numbers, which correspond with the numbers in the last column of [Table 5](#) to [Table 8](#).

Table 5. State transitions forced by EN and STBN (node configuration)

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	UV _{VIO}	UV _{VBAT}	UV _{VCC}	PWON	Wake	
Normal	receive only	1	H	→ L	cleared	cleared	cleared	cleared	cleared	
	go-to-sleep	2	→ L	H	cleared	cleared	cleared	cleared	cleared	
	standby	3	→ L	→ L	cleared	cleared	cleared	cleared	cleared	[1]
Receive only	normal	4	H	→ H	cleared	cleared	cleared	X	X	
	go-to-sleep	5	→ L	→ H	cleared	cleared	cleared	X	X	
	standby	6	→ L	L	cleared	cleared	cleared	X	X	
Standby	normal	7	→ H	→ H	cleared	cleared	2 → cleared	X	1 → set	[2][3]
	receive only	8	→ H	L	cleared	cleared	2 → cleared	X	1 → set	[2][3]
	go-to-sleep	9	L	→ H	cleared	cleared	X	X	X	
Go-to-sleep	normal	10	→ H	H	cleared	cleared	cleared	X	1 → set	[2][4]
	receive only	11	→ H	→ L	cleared	cleared	cleared	X	1 → set	[2][4]
	standby	12	L	→ L	cleared	cleared	X	X	X	[4]
	sleep	13	L	H	cleared	cleared	X	X	cleared	[5]
Sleep	normal	14	→ H	H	2 → cleared	2 → cleared	2 → cleared	X	1 → set	[2][3]
	receive only	15	→ H	L	2 → cleared	2 → cleared	2 → cleared	X	1 → set	[2][3]

[1] STBN must be set to LOW 60 μs after EN.

[2] Positive edge on pin STBN sets the wake flag.

[3] Setting the wake flag clears the UV_{VIO}, UV_{VBAT} and UV_{VCC} flag.

[4] Hold time of go-to-sleep is less than the minimum hold time.

[5] Hold time of go-to-sleep becomes greater than the minimum hold time.

Table 6. State transitions forced by a wake-up (node configuration)

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	Wake	UV _{VIO}	UV _{VBAT}	UV _{VCC}	PWON	
Standby	normal	16	H	H	→ set	cleared	cleared	1 → cleared	X	[1]
	receive only	17	H	L	→ set	cleared	cleared	1 → cleared	X	[1]
	go-to-sleep	18	L	H	→ set	cleared	cleared	1 → cleared	X	[1]
	standby	19	L	L	→ set	cleared	cleared	1 → cleared	X	[1]
Go-to-sleep	normal	20	H	H	→ set	cleared	cleared	cleared	X	
	receive only	21	H	L	→ set	cleared	cleared	cleared	X	
	standby	22	L	L	→ set	cleared	cleared	cleared	X	
	go-to-sleep	23	L	H	→ set	cleared	cleared	cleared	X	
Sleep	normal	24	H	H	→ set	1 → cleared	1 → cleared	1 → cleared	X	[1]
	receive only	25	H	L	→ set	1 → cleared	1 → cleared	1 → cleared	X	[1]
	standby	26	L	L	→ set	1 → cleared	1 → cleared	1 → cleared	X	[1]
	go-to-sleep	27	L	H	→ set	1 → cleared	1 → cleared	1 → cleared	X	[1]

[1] Setting the wake flag clears the UV_{VIO}, UV_{VBAT} and UV_{VCC} flag.

Table 7. State transitions forced by an undervoltage condition (node configuration)
 → indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Flag					Note	
			UV _{VIO}	UV _{VBAT}	UV _{VCC}	PWON	Wake		
Normal	sleep	28	→ set	cleared	cleared	cleared	cleared	1 → cleared	[1]
	sleep	29	cleared	→ set	cleared	cleared	cleared	1 → cleared	[1]
	standby	30	cleared	cleared	→ set	cleared	cleared	1 → cleared	[1]
Receive only	sleep	31	→ set	cleared	cleared	X	X	1 → cleared	[1]
	sleep	32	cleared	→ set	cleared	X	X	1 → cleared	[1]
	standby	33	cleared	cleared	→ set	X	X	1 → cleared	[1]
Go-to-sleep	sleep	34	→ set	cleared	cleared	X	X	1 → cleared	[1]
	sleep	35	cleared	→ set	cleared	X	X	1 → cleared	[1]
	standby	36	cleared	cleared	→ set	X	X	1 → cleared	[1]
Standby	sleep	37	→ set	cleared	X	X	X	1 → cleared	[1][2]
	sleep	38	cleared	→ set	X	X	X	1 → cleared	[1][3]

[1] UV_{VIO}, UV_{VBAT} or UV_{VCC} detected clears the wake flag.

[2] UV_{VIO} overrules UV_{VCC}.

[3] UV_{VBAT} overrules UV_{VCC}.

Table 8. State transitions forced by an undervoltage recovery (node configuration)
 → indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	UV _{VIO}	UV _{VBAT}	UV _{VCC}	PWON	Wake	
Standby	normal	39	H	H	cleared	cleared	→ cleared	X	X	[1]
	receive only	40	H	L	cleared	cleared	→ cleared	X	X	[1]
Sleep	normal	41	H	H	cleared	→ cleared	cleared	X	1 → set	[2][3]
	normal	42	H	H	→ cleared	cleared	cleared	X	X	[4]
	receive only	43	H	L	cleared	→ cleared	cleared	X	1 → set	[2][3]
	receive only	44	H	L	→ cleared	cleared	cleared	X	X	[4]
	standby	45	L	L	cleared	→ cleared	cleared	X	1 → set	[2][3]
	standby	46	L	L	→ cleared	cleared	cleared	X	X	[4]
	go-to-sleep	47	L	H	cleared	→ cleared	cleared	X	1 → set	[2][3]
	go-to-sleep	48	L	H	→ cleared	cleared	cleared	X	X	[4]

[1] Recovery of UV_{VCC} flag.

[2] Recovery of UV_{VBAT} flag.

[3] Clearing the UV_{VBAT} flag sets the wake flag.

[4] Recovery of UV_{VIO} flag.

7.2.1 Normal mode

In Normal mode the transceiver is able to transmit and receive data via the bus lines BP and BM. The output of the normal receiver is directly connected to pin RXD.

The transmitter behavior in normal mode of operation, with no time-out present on pins TXEN and BGE and the temperature flag not set is given in [Table 9](#).

In this mode pins INH1 and INH2 are set HIGH.

Table 9. Transmitter function table

BGE	TXEN	TXD	Transmitter
L	X	X	transmitter is disabled
X	H	X	transmitter is disabled
H	L	H	transmitter is enabled; the bus lines are actively driven; BP is driven HIGH and BM is driven LOW
H	L	L	transmitter is enabled; the bus lines are actively driven; BP is driven LOW and BM is driven HIGH

7.2.2 Receive only mode

In receive only mode the transceiver can only receive data. The transmitter is disabled, regardless of the voltages on pins BGE and TXEN.

In this mode pins INH1 and INH2 are set HIGH.

7.2.3 Standby mode

In Standby mode the transceiver enters a low power mode which means very low current consumption. In the Standby mode the device is not able to transmit or receive data and the low power receiver is activated to monitor bus activity.

Standby mode can be entered if the correct polarity is applied to pins EN and STBN (see [Figure 4](#) and [Table 5](#)) or an undervoltage is present on pin V_{CC} ; see [Figure 4](#).

If an undervoltage is present on pin V_{CC} , direct switching to a normal power mode is not possible. By applying a positive edge on pin STBN and thus setting the wake flag, all undervoltage flags are reset and therefore switching to a normal power mode is possible. The transceiver will then enter the mode indicated on pins EN and STBN

In this mode the transceiver can be switched to any other mode if no undervoltage is present on pins V_{IO} and V_{BAT} .

Pin INH1 is set to HIGH. If the wake flag is set, pin INH2 is set to HIGH and pins RXEN and RXD are set to LOW, otherwise pin INH2 is floating and pins RXEN and RXD are set to HIGH; see [Section 7.5](#).

7.2.4 Go-to-sleep mode

In this mode the transceiver behaves as in Standby mode. If this mode is selected for a longer time than the go-to-sleep command hold time (minimum hold time) and the wake flag has been previously cleared, the transceiver will enter Sleep mode, regardless of the voltage on pin EN.

If the voltage regulator that supplies the host is switched via pin INH1, pin EN becomes LOW if pin INH1 is switched off.

7.2.5 Sleep mode

In Sleep mode the transceiver has entered a low power mode. The only difference with Standby mode is that pin INH1 is also set floating. Sleep mode is directly entered if the $UV_{V_{IO}}$ or $UV_{V_{BAT}}$ flag is set.

In this mode the transceiver can be switched to any other mode if no undervoltage is present on pins V_{IO} , V_{CC} and V_{BAT} . In case of an undervoltage on pin V_{CC} or V_{BAT} while V_{IO} is present, the wake flag is set by a positive edge on pin STBN.

The undervoltage flags will be reset by setting the wake flag, and therefore the transceiver will enter the mode indicated on pins EN and STBN if V_{IO} is present.

A detailed description of the wake-up mechanism is given in [Section 7.5](#).

7.3 Operating modes in star configuration

In star configuration mode control via pins EN and STBN is not possible. The transceiver autonomously controls the operating modes except in the case of wake-up.

The timing diagram of a transceiver configured in star configuration is illustrated in [Figure 6](#). The state diagram in star configuration is illustrated in [Figure 5](#). A detailed description of the pin signalling in star configuration is given in [Table 10](#).

If V_{IO} and (V_{BUF} or V_{BAT}) are within their operating range, pin ERRN will indicate the error flag.

Table 10. Pin signalling in star configuration

Mode	TRXD0 / TRXD1	ERRN		RXEN		RXD		Transmitter	INH1	INH2
		LOW	HIGH	LOW	HIGH	LOW	HIGH			
Star Transmit	output [1] input [2]	error flag set [3]	error flag reset [3]	bus activity	bus idle	bus DATA_0	bus DATA_1	enabled	HIGH	HIGH
Star Receive	output							disabled [1]		
Star Idle	input									
Star Locked	input									
Star Standby	input	error flag set [1][3]	Error flag reset [1][3]	wake flag set [1]	wake flag reset [1]	wake flag set [1]	wake flag reset [1]			
Star Sleep	input								float [1]	float [1]

[1] Valid if V_{IO} and (V_{BUF} or V_{BAT}) are present.

[2] TRXD lines are switched as input if TRXD activity is the initiator for star Transmit mode.

[3] Pin ERRN provides a serial interface for retrieving diagnostic information.

[4] TRXD lines switched as output if TXEN activity is the initiator for star Transmit mode.

Pin BGE has to be connected to pin V_{IO} in order to enable the transmitter via pin TXEN. If pin BGE is connected to ground, it is not possible to activate the transmitter via pin TXEN. If pin TXEN is not used (no controller connected to the transceiver), it has to be connected to pin V_{IO} in order to prevent TXEN activity detection.

In all modes pin RXD is connected to the output of the normal mode receiver and therefore represents the data on the bus lines.

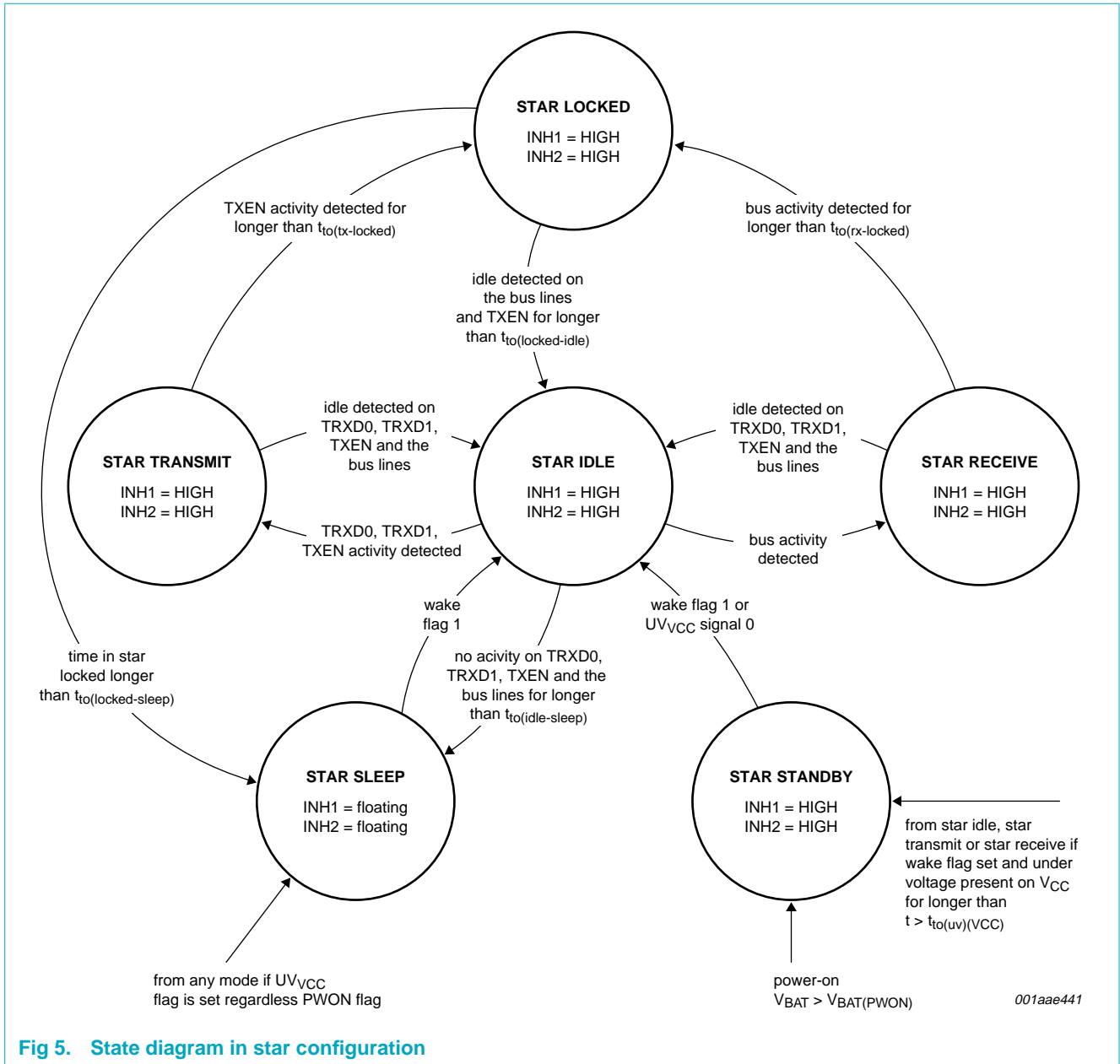
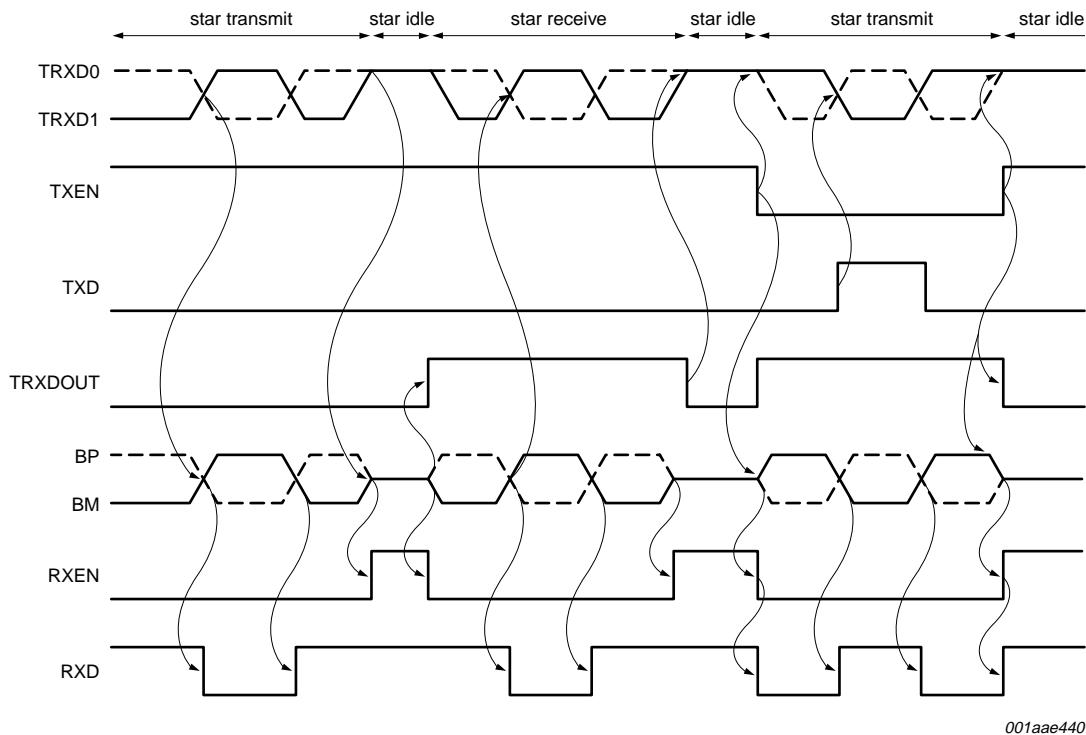


Fig 5. State diagram in star configuration



TRXDOUT is a virtual signal that indicates the state of the TRXD lines. TRXDOUT HIGH means TRXD lines switched as output. TRXDOUT LOW means TRXD lines switched as input.

Fig 6. Timing diagram in star configuration

7.3.1 Star Idle mode

This mode is entered if one of the following events occurs:

- From star Receive mode and star Transmit mode if idle is detected on the bus lines, on pin TXEN and on pins TRXD0 and TRXD1.
- If the transceiver is in star Locked mode and idle is detected on the bus lines and pin TXEN for longer than $t_{to(locked-idle)}$.
- If the transceiver is in star Standby mode and the wake flag is set or no undervoltage is present.
- If the transceiver is in star Sleep mode and the wake flag is set, the transceiver enters star Idle mode in order to obtain a stable starting point (no glitches on the bus lines etc).
- In star Idle mode the transceiver monitors pins TXEN, TRXD0 and TRXD1 and the bus lines for activity. In this mode the transmitter is disabled.

7.3.2 Star Transmit mode

This mode is entered if one of the following events occur:

- If the transceiver is in star Idle mode and activity is detected on pin TXEN.
- If the transceiver is in star Idle mode and activity is detected on pins TRXD0 and TRXD1.

In star Transmit mode the transmitter is enabled and the transceiver can transmit data on the bus lines. It transmits the data received on pins TXD or TRXD0 and TRXD1 on the bus lines.

7.3.3 Star Receive mode

This mode is entered if the transceiver is in star Idle mode and activity has been detected on the bus lines.

In star Receive mode the transceiver transmit data via the TRXD0 and TRXD1 lines to other transceivers connected to the bus lines. The transmitter is always disabled.

7.3.4 Star Standby mode

This mode is entered if one of the following events occur:

- From star Idle, star Transmit or star Receive modes if the wake flag is set and an undervoltage on pin V_{CC} is present for longer than $t_{to(uv)}(V_{CC})$.
- If the PWON flag is set.

In star Standby mode the transceiver enters a low power mode. In this mode the current consumption is as low as possible to prevent discharging the capacitor at pin V_{BUF} .

If pins V_{IO} and V_{BUF} are within their temperature range, pins RXD and RXEN will indicate the wake flag.

7.3.5 Star Sleep mode

This mode is entered if one of the following events occur:

- From any mode if an undervoltage on pin V_{CC} is present for longer than $t_{det(uv)}(V_{CC})$.
- If the transceiver is in star Idle mode and no activity is detected on the bus lines and pins TXEN, TRXD0 and TRXD1 for longer than $t_{to(idle-sleep)}$.
- If star Locked mode is active for longer than $t_{to(locked-sleep)}$.

In star Sleep mode the transceiver will enter a low power mode. In this mode the current consumption is as low as possible to prevent the car battery from discharging. The inhibit switches are switched off.

In this mode the wake flag wakes the transceiver. A detailed description of the wake-up mechanism is given in [Section 7.5](#).

If pins V_{IO} and V_{BUF} are within their temperature range, pins RXD and RXEN will indicate the wake flag.

7.3.6 Star Locked mode

This mode is entered if one of the following events occur:

- If the transceiver is in star Transmit mode and activity on pin TXEN is detected for longer than $t_{to(tx-locked)}$.
- If the transceiver is in star Receive mode and activity is detected on the bus lines for longer than $t_{to(rx-locked)}$.

This mode is a fail-silent mode and in this mode the transmitter is disabled.

7.4 Start-up

7.4.1 Node configuration

Node configuration can be selected by applying a voltage lower than $0.3V_{BUF}$ to pins TRXD0 and TRXD1 during power-on. Node configuration is latched by resetting the PWON flag while the voltage on pins TRXD0 and TRXD1 is lower than $0.3V_{BUF}$; see [Section 7.7.4](#) for (re)setting the PWON flag.

7.4.2 Star configuration

Star configuration can be selected by applying a voltage higher than $0.7V_{BUF}$ to pins TRXD0 or TRXD1 during power-on. Star configuration is latched by resetting the PWON flag while one of the voltages on pins TRXD0 or TRXD1 is higher than $0.7V_{BUF}$. See [Section 7.7.4](#) for (re)setting the PWON flag. In this case the transceiver goes from node Standby mode to star Idle mode.

7.5 Wake-up mechanism

7.5.1 Node configuration

If a node configured transceiver is in Sleep mode (pins INH1 and INH2 are switched off), it will enter Standby mode or go-to-sleep mode (depending on the level at pin EN). In both modes pin INH1 is switched on, pin INH2 is switched on or off depending on whether the wake flag is set.

If no undervoltage is present on pins V_{IO} and V_{BAT} , the transceiver switches immediately to the mode indicated on pins EN and STBN.

In Standby, go-to-sleep and Sleep mode pins RXD and RXEN are driven LOW if the wake flag is set.

7.5.2 Star configuration

If a star configured transceiver is in Sleep mode (pins INH1 and INH2 are switched off) it will enter star Idle mode (pins INH1 and INH2 are switched on) if the wake flag is set. In star Idle mode, the transceiver enters the appropriate mode directly, depending on which event has set the wake flag:

- If the wake-up source was pin WAKE or a positive edge on pin STBN, the transceiver will remain in star Idle mode.
- If the wake-up source was activity detected on pins TRXD0 and TRXD1, the transceiver will change from star Idle mode to star Transmit mode.

- If the wake-up source was a wake-up symbol, the transceiver will change from star Idle mode to star Receive mode.

7.5.3 Bus wake-up

Bus wake-up is detected if two consecutive DATA_0 of at least $t_{det(wake)DATA_0}$ separated by an idle or DATA_1 of at least $t_{det(wake)idle}$, followed by an idle or DATA_1 of at least $t_{det(wake)idle}$ are present on the bus lines within $t_{det(wake)tot}$.

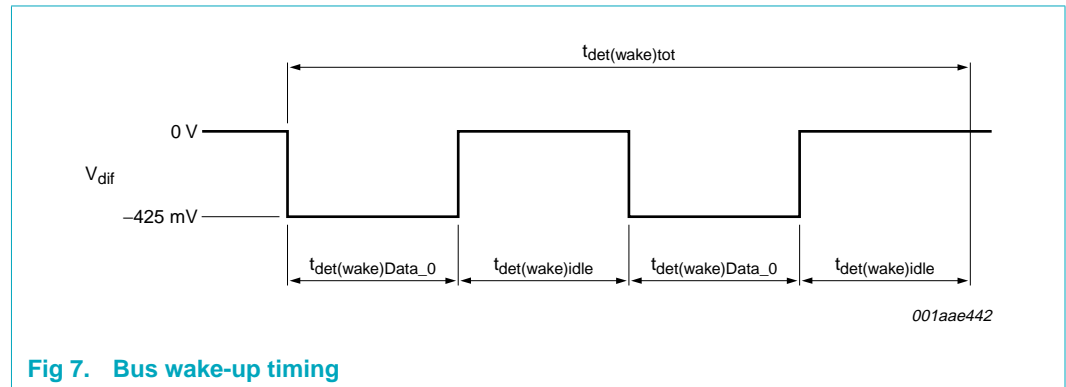


Fig 7. Bus wake-up timing

7.5.4 Local wake-up via pin WAKE

If the voltage on pin WAKE is lower than $V_{th(det)(WAKE)}$ for longer than $t_{wake(WAKE)}$ (falling edge on pin WAKE) a local wake-up event on pin WAKE is detected. At the same time, the biasing of this pin is switched to pull-down.

If the voltage on pin WAKE is higher than $V_{th(det)(WAKE)}$ for longer than t_{wake} , the biasing of this pin is switched to pull-up, and no local wake-up will be detected.

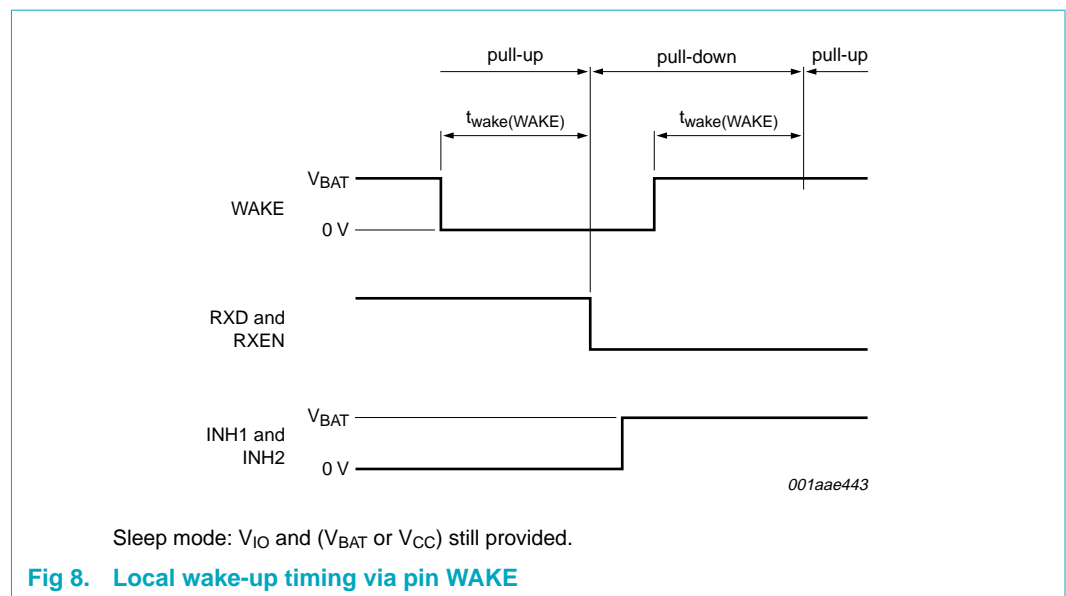


Fig 8. Local wake-up timing via pin WAKE

7.6 Fail silent behavior

In order to be fail silent, undervoltage detection is implemented. An undervoltage will be detected on pins V_{CC} , V_{IO} and V_{BAT} .

7.6.1 V_{BAT} undervoltage

- Node configuration: If the $UV_{V_{BAT}}$ flag is set the transceiver will enter Sleep mode (pins INH1 and INH2 are switched off) regardless of the voltage present on pins EN and STBN. If the undervoltage recovers the wake flag will be set and the transceiver will enter the mode determined by the voltages on pins EN and STBN.
- Star configuration: The TJA1080 in star configuration is able to transmit and receive data as long as V_{CC} and V_{IO} are within their operating range, regardless of the undervoltage on V_{BAT} .

7.6.2 V_{CC} undervoltage

- Node configuration: If the $UV_{V_{CC}}$ flag is set the transceiver will enter the Standby mode (pin INH2 is switched off) regardless of the voltage present on pins EN and STBN. If the undervoltage recovers or the wake flag is set mode switching via pins EN and STBN is possible.
- Star configuration: If the $UV_{V_{CC}}$ flag is set the transceiver will enter the star Sleep mode.

7.6.3 V_{IO} undervoltage

- Node configuration: If the voltage on pin V_{IO} is lower than $V_{uvd(V_{IO})}$ (even if the $UV_{V_{IO}}$ flag is reset) pins EN, STBN, TXD and BGE are set LOW (internally) and pin TXEN is set HIGH (internally). If the $UV_{V_{IO}}$ flag is set the transceiver will enter Sleep mode (pins INH1 and INH2 are switched off).
- Star configuration: If an undervoltage is present on pin V_{IO} (even if the $UV_{V_{IO}}$ flag is reset) pins EN, STBN, TXD and BGE are set LOW (internally) and pin TXEN is set HIGH (internally). If the V_{IO} undervoltage flag is set, pin INH1 is switched off. If an undervoltage is present on pin V_{IO} and V_{CC} is within the operating range, the TJA1080 will forward the received data to all other branches.

7.7 Flags

7.7.1 Local wake-up source flag

The local wake-up source flag can only be set in a low power mode. When a wake-up event on pin WAKE is detected (see [Section 7.5.4](#)) it sets the local wake-up source flag. The local wake-up source flag is reset by entering a low power mode.

7.7.2 Remote wake-up source flag

The remote wake-up source flag can only be set in a low power mode. When a bus wake-up event is detected on the bus lines (see [Section 7.5.3](#)) it sets the remote wake-up source flag. The remote wake-up source flag is reset by entering a low power mode.

7.7.3 Wake flag

The wake flag is set if one of the following events occurs:

- The local or remote wake-up source flag is set (edge sensitive)
- A positive edge is detected on pin STBN if V_{IO} is present
- Recovery of the UV_{VBAT} flag (only in node configuration)
- By recognizing activity on pins TRXD0 and TRXD1 (only in star configuration)

In node configuration the wake flag is reset by entering Normal mode, a low power mode or setting one of the undervoltage flags. In star configuration the wake flag is reset by entering a low power mode or by recovery of the UV_{VCC} signal (without $t_{rec(uv)(VCC)}$).

7.7.4 Power-on flag

The PWON flag is set if the internal supply voltage for the digital part becomes higher than the lowest value it needs to operate. In node configuration, entering Normal mode resets the PWON flag. In star configuration the PWON flag is reset when the UV_{VCC} signal goes LOW (no undervoltage detected).

7.7.5 Node or star configuration flag

Configuration flag set means node configuration.

7.7.6 Temperature medium flag

The temperature medium flag is set if the junction temperature exceeds $T_{j(warn)(medium)}$ in a normal power mode. The temperature medium flag is reset when the junction temperature becomes lower than $T_{j(warn)(medium)}$ in a normal power mode. No action will be taken if this flag is set.

7.7.7 Temperature high flag

The temperature high flag is set if the junction temperature exceeds $T_{j(dis)(high)}$ in a normal power mode.

In node configuration the temperature high flag is reset if a negative edge is applied to pin TXEN while the junction temperature is lower than $T_{j(dis)(high)}$ in a normal power mode. In star configuration mode the temperature high flag is reset by any activity detection (edge) while the junction temperature is lower than $T_{j(dis)(high)}$ in a normal power mode.

If the temperature high flag is set the transmitter is disabled and pins TRXD0 and TRXD1 are switched off.

7.7.8 TXEN_BGE clamped flag

The TXEN_BGE clamped flag is set if pin TXEN is LOW and pin BGE is HIGH for longer than $t_{det(CL)(TXEN_BGE)}$. The TXEN_BGE clamped flag is reset if pin TXEN is HIGH or pin BGE is LOW. If the TXEN_BGE flag is set, the transmitter is disabled.

7.7.9 Bus error flag

The bus error flag is set if pin TXEN is LOW and pin BGE is HIGH and the data received from the bus lines (pins BP and BM) is different to that received on pin TXD. The TJA1080 also expects that a data frame begins with a bit value other than the last bit of the previous data frame.

This is the case for a valid data frame which begins with the DATA_0 period of the Transmission Start Sequence (TSS) and ends with the DATA_1 bit of the Frame End Sequence (FES). Any violation of this frame format will be detected by the TJA1080. Consequently, when transmitting a wake-up pattern, a bus error will be signalled. This error indication should be ignored and the status register should be cleared by reading the vector.

No action will be taken if the bus error flag is set.

7.7.10 UV_{V_{BAT}} flag

The UV_{V_{BAT}} flag is set if the voltage on pin V_{BAT} is lower than V_{uvd(V_{BAT})}. The UV_{V_{BAT}} flag is reset if the voltage is higher than V_{uvd(V_{BAT})} or by setting the wake flag; see [Section 7.6.1](#).

7.7.11 UV_{V_{CC}} flag

The UV_{V_{CC}} flag is set if the voltage on pin V_{CC} is lower than V_{uvd(V_{CC})} for longer than t_{det(uv)(V_{CC})}. The flag is reset if the voltage on pin V_{CC} is higher than V_{uvd(V_{CC})} for longer than t_{rec(uv)(V_{CC})} or the wake flag is set; see [Section 7.6.2](#).

7.7.12 UV_{V_{IO}} flag

The UV_{V_{IO}} flag is set if the voltage on pin V_{IO} is lower than V_{uvd(V_{IO})} for longer than t_{det(uv)(V_{IO})}. The flag is reset if the voltage on pin V_{IO} is higher than V_{uvd(V_{IO})} or the wake flag is set; see [Section 7.6.3](#).

7.7.13 Error flag

The error flag is set if one of the status bits S4 to S12 is set. The error flag is reset if none of the S4 to S12 status bits are set; see [Table 11](#).

7.8 TRXD collision

A TRXD collision is detected when two or more TJA1080s in star configuration enter star Receive mode.

7.9 Status register

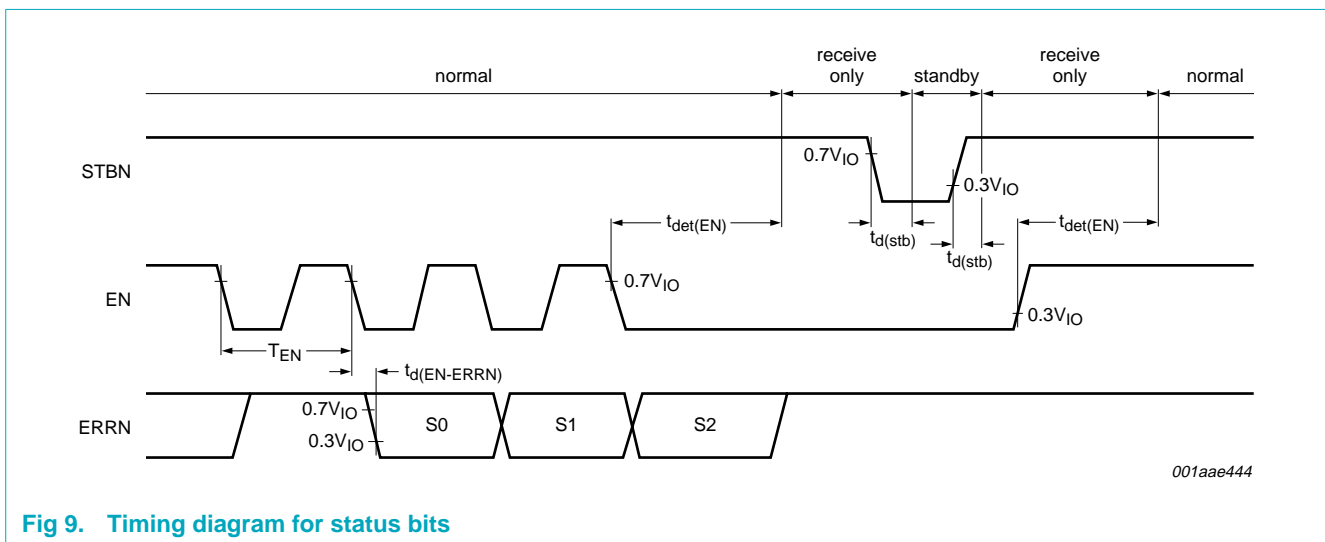
The status register can be read out on pin ERRN by using pin EN as clock; the status bits are given in [Table 11](#). The timing diagram is illustrated in [Figure 9](#).

The status register is accessible if the UV_{V_{IO}} flag is not set in node or star configuration. A negative edge on pin EN starts the read out. Within the period t_{d(EN-ERRN)} after the first edge on pin EN, pin ERRN will go HIGH if it was previously LOW. On the second negative edge on pin EN the first status bit (S0) will be shifted out. The status bits are valid after t_{d(EN-ERRN)}. If no edge is detected on pin EN for longer than t_{det(EN)}, the transceiver will enter the state selected on pins EN and STBN (node configuration) and status bit S4 to S12 will be reset if the corresponding flag has been reset.

Pin ERRN is LOW if the corresponding status bit is set.

Table 11. Status bits

Bit number	Status bit	Description
S0	LOCAL WAKEUP	local wake-up source flag is redirected to this bit
S1	REMOTE WAKEUP	remote wake-up source flag is redirected to this bit
S2	NODE CONFIG	node configuration flag is redirected to this bit
S3	PWON	status bit set means PWON flag has been set previously
S4	BUS ERROR	status bit set means bus error flag has been set previously
S5	TEMP HIGH	status bit set means temperature high flag has been set previously
S6	TEMP MEDIUM	status bit set means temperature medium flag has been set previously
S7	TXEN_BGE CLAMPED	status bit set means TXEN_BGE clamped flag has been set previously
S8	UVVBAT	status bit set means UV_{VBAT} flag has been set previously
S9	UVVCC	status bit set means UV_{VCC} flag has been set previously
S10	UVVIO	status bit set means UV_{VIO} flag has been set previously
S11	STAR LOCKED	status bit is set if star Locked mode has been entered previously
S12	TRXD COLLISION	status bit is set if a TRXD collision has been detected previously



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Fig 9. Timing diagram for status bits

8. Limiting values

Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{BAT}	supply voltage on pin V _{BAT}	no time limit	-0.3	+60	V	
		operating range	6.5	60	V	
V _{CC}	supply voltage	no time limit	-0.3	+5.5	V	
		operating range	4.75	5.25	V	
V _{BUF}	supply voltage on pin V _{BUF}	no time limit	-0.3	+5.5	V	
		operating range	4.75	5.25	V	
V _{IO}	supply voltage on pin V _{IO}	no time limit	-0.3	+5.5	V	
		operating range	2.2	5.25	V	
V _{INH1}	voltage on pin INH1		-0.3	V _{BAT} + 0.3	V	
V _{INH2}	voltage on pin INH2		-0.3	V _{BAT} + 0.3	V	
V _{WAKE}	voltage on pin WAKE		-0.3	V _{BAT} + 0.3	V	
I _{o(WAKE)}	output current on pin WAKE	pin GND not connected	-15	-	mA	
V _{BGE}	voltage on pin BGE	no time limit	-0.3	V _{IO} + 0.3	V	
V _{TXEN}	voltage on pin TXEN	no time limit	-0.3	V _{IO} + 0.3	V	
V _{TXD}	voltage on pin TXD	no time limit	-0.3	V _{IO} + 0.3	V	
V _{ERRN}	voltage on pin ERRN	no time limit	-0.3	V _{IO} + 0.3	V	
V _{RXD}	voltage on pin RXD	no time limit	-0.3	V _{IO} + 0.3	V	
V _{RXEN}	voltage on pin RXEN	no time limit	-0.3	V _{IO} + 0.3	V	
V _{EN}	voltage on pin EN	no time limit	-0.3	+5.5	V	
V _{STBN}	voltage on pin STBN	no time limit	-0.3	+5.5	V	
V _{TRXD0}	voltage on pin TRXD0	no time limit	-0.3	+5.5	V	
V _{TRXD1}	voltage on pin TRXD1	no time limit	-0.3	+5.5	V	
V _{BP}	voltage on pin BP		-60	+60	V	
V _{trt}	transient voltage	on pins BP and BM	[1]	-200	+200	V
		on pin V _{BAT}	[2]	-200	+200	V
		on pin V _{BAT}	[3]	6.5	60	V
		on pin V _{BAT}	[4]	-	60	V
T _{stg}	storage temperature		-55	+150	°C	
T _{vj}	virtual junction temperature		[5]	-40	+150	°C
V _{ESD}	electrostatic discharge voltage	HBM on pins BP and BM to ground	[6]	-8.0	+8.0	kV
		HBM at any other pin	[7]	-4.0	+4.0	kV
		MM on all pins	[8]	-200	+200	V
		CDM on all pins	[9]	-1000	+1000	V

[1] According to ISO 7637, part 3 test pulses a and b; Class C; see [Figure 13](#); R_L = 45 Ω; C_L = 100 pF.

[2] According to ISO 7637, part 2 test pulses 1, 2, 3a and 3b; Class C; see [Figure 13](#); R_L = 45 Ω; C_L = 100 pF.

[3] According to ISO 7637, part 2 test pulse 4; Class C; see [Figure 13](#); R_L = 45 Ω; C_L = 100 pF.

[4] According to ISO 7637, part 2 test pulse 5b; Class C; see [Figure 13](#); R_L = 45 Ω; C_L = 100 pF.

- [5] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature T_{vj} is: $T_{vj} = T_{amb} + TD \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value to be used for the calculation of T_{vj} . The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
- [6] HBM: C = 100 pF; R = 1.5 k Ω .
- [7] HBM: C = 100 pF; R = 1.5 k Ω .
- [8] MM: C = 200 pF; L = 0.75 μ H; R = 10 Ω .
- [9] CDM: C = 330 pF; R = 150 Ω .

9. Thermal characteristics

Table 13. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	126	K/W
$R_{th(j-s)}$	thermal resistance from junction to substrate	in free air	-	K/W

10. Static characteristics

Table 14. Static characteristics

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BUF} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.^{[1][2]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin V_{BAT}						
I_{BAT}	supply current on pin V_{BAT}	low power modes in node configuration	-	35	50	μA
		star Sleep mode	-	40	50	μA
		star Standby mode	-	75	150	μA
		normal power modes	-	0.075	1	mA
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin V_{BAT}		2.75	3.8	4,5	V
Pin V_{CC}						
I_{CC}	supply current	low power modes	-1	0	+5	μA
		Normal mode; $V_{BGE} = 0\text{ V}$; $V_{TXEN} = V_{IO}$; Receive only mode; star Idle mode	-	10	15	mA
		Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$; V_{BUF} open	[3] -	28.5	35	mA
		Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$; $R_{bus} = \infty\text{ }\Omega$	-	10	15	mA
		star Transmit mode	-	50	62	mA
		star Receive mode	-	38	42	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		2.75	3.8	4.5	V
Pin V_{IO}						
I_{IO}	supply current on pin V_{IO}	low power modes	-1	+1	+5	μA
		Normal and Receive only mode; $V_{TXD} = V_{IO}$	-	30	1000	μA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1	1.5	2	V
$V_{uvr(VIO)}$	undervoltage recovery voltage on pin V_{IO}		1	1.6	2.2	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin V_{IO}		25	<td>	<td>	mV

Table 14. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V}$ to 60 V ; $V_{CC} = 4.75\text{ V}$ to 5.25 V ; $V_{BUF} = 4.75\text{ V}$ to 5.25 V ; $V_{IO} = 2.2\text{ V}$ to 5.25 V ; $T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.^{[1][2]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin V_{BUF}						
I_{BUF}	supply current on pin V_{BUF}	low power modes in node configuration	-1	0	+5	μA
		low power modes in star configuration				
		$V_{BUF} = 0\text{ V}$; $V_{CC} = 0\text{ V}$	-40	-20	+1	μA
		$V_{BUF} = 5.25\text{ V}$	-1	0	+5	μA
		Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$; $V_{BUF} = V_{CC}$	[3] -	26.5	35	mA
		star Transmit mode	-	47	62	mA
		star Receive mode	-	35	42	mA
		Normal mode; $V_{BGE} = 0\text{ V}$; $V_{TXEN} = V_{IO}$; Receive only mode; star Idle mode	-	10	15	mA
$V_{BUF(on)}$	on-state voltage on pin V_{BUF}	V_{CC} switch is switched on; Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$; $V_{CC} >$ maximum value of $V_{Uvd}(V_{CC})$	$V_{CC} - 0.25$	$V_{CC} - 0.05$	V_{CC}	V
$V_{BUF(off)}$	off-state voltage on pin V_{BUF}	V_{CC} switch is switched off; low power modes in star configuration; $V_{CC} <$ minimum value of $V_{Uvd}(V_{CC})$	4.5	4.9	5.25	V
Pin EN						
$V_{IH(EN)}$	HIGH-level input voltage on pin EN		$0.7V_{IO}$	$0.5V_{IO}$	5.5	V
$V_{IL(EN)}$	LOW-level input voltage on pin EN		-0.3	$0.5V_{IO}$	$0.3V_{IO}$	V
$I_{IH(EN)}$	HIGH-level input current on pin EN	$V_{EN} = 0.7V_{IO}$	3	8	11	μA
$I_{IL(EN)}$	LOW-level input current on pin EN	$V_{EN} = 0\text{ V}$	-1	0	+1	μA
Pin STBN						
$V_{IH(STBN)}$	HIGH-level input voltage on pin STBN		$0.7V_{IO}$	$0.5V_{IO}$	5.5	V
$V_{IL(STBN)}$	LOW-level input voltage on pin STBN		-0.3	$0.5V_{IO}$	$0.3V_{IO}$	V
$I_{IH(STBN)}$	HIGH-level input current on pin STBN	$V_{STBN} = 0.7V_{IO}$	3	8	11	μA
$I_{IL(STBN)}$	LOW-level input current on pin STBN	$V_{STBN} = 0\text{ V}$	-1	0	+1	μA

Table 14. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BUF} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.^{[1][2]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin TXEN						
$V_{IH(TXEN)}$	HIGH-level input voltage on pin TXEN		$0.7V_{IO}$	$0.5V_{IO}$	$V_{IO} + 0.3$	V
$V_{IL(TXEN)}$	LOW-level input voltage on pin TXEN		-0.3	$0.5V_{IO}$	$0.3V_{IO}$	V
$I_{IH(TXEN)}$	HIGH-level input current on pin TXEN	$V_{TXEN} = V_{IO}$	-1	0	+1	μA
$I_{IL(TXEN)}$	LOW-level input current on pin TXEN	$V_{TXEN} = 0.3V_{IO}$	-12	-9	-3	μA
$I_{L(TXEN)}$	leakage current on pin TXEN	$V_{TXEN} = 5.25\text{ V}$; $V_{IO} = 0\text{ V}$	-1	0	+1	μA
Pin BGE						
$V_{IH(BGE)}$	HIGH-level input voltage on pin BGE		$0.7V_{IO}$	$0.5V_{IO}$	$V_{IO} + 0.3$	V
$V_{IL(BGE)}$	LOW-level input voltage on pin BGE		-0.3	$0.5V_{IO}$	$0.3V_{IO}$	V
$I_{IH(BGE)}$	HIGH-level input current on pin BGE	$V_{BGE} = 0.7V_{IO}$	3	8	11	μA
$I_{IL(BGE)}$	LOW-level input current on pin BGE	$V_{BGE} = 0\text{ V}$	-1	0	+1	μA
Pin TXD						
$V_{IH(TXD)}$	HIGH-level input voltage on pin TXD	normal power modes	$0.7V_{IO}$	$0.5V_{IO}$	$V_{IO} + 0.3$	V
$V_{IL(TXD)}$	LOW-level input voltage on pin TXD	normal power modes	-0.3	$0.5V_{IO}$	$0.3V_{IO}$	V
$I_{IH(TXD)}$	HIGH-level input current on pin TXD	$V_{TXD} = V_{IO}$	70	300	650	μA
$I_{IL(TXD)}$	LOW-level input current on pin TXD	normal power modes; $V_{TXD} = 0\text{ V}$	-5	0	+5	μA
		low power modes	-1	0	+1	μA
$I_{LI(TXD)}$	input leakage current on pin TXD	$V_{TXD} = 5.25\text{ V}$; $V_{IO} = 0\text{ V}$	-1	0	+1	μA
Pin RXD						
$I_{OH(RXD)}$	HIGH-level output current on pin RXD	$V_{RXD} = V_{IO} - 0.4\text{ V}$; $V_{IO} = V_{CC}$	-2	-4	-15	mA
$I_{OL(RXD)}$	LOW-level output current on pin RXD	$V_{RXD} = 0.4\text{ V}$	2	7	20	mA
Pin ERRN						
$I_{OH(ERRN)}$	HIGH-level output current on pin ERRN	node configuration; $V_{ERRN} = V_{IO} - 0.4\text{ V}$; $V_{IO} = V_{CC}$	-1500	-550	-100	μA
		star configuration; $V_{ERRN} = V_{IO} - 0.4\text{ V}$; $V_{IO} = V_{CC}$	-1	0	+1	μA

Table 14. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BUF} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.^{[1][2]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OL(ERRN)}$	LOW-level output current on pin ERRN	$V_{ERRN} = 0.4\text{ V}$	300	700	1500	μA
Pin RXEN						
$I_{OH(RXEN)}$	HIGH-level output current on pin RXEN	$V_{RXEN} = V_{IO} - 0.4\text{ V}$; $V_{IO} = V_{CC}$	-4	-1.5	-0.5	mA
$I_{OL(RXEN)}$	LOW-level output current on pin RXEN	$V_{RXEN} = 0.4\text{ V}$	1	3	8	mA
Pins TRXD0 and TRXD1						
$V_{IH(TRXD0)}$	HIGH-level input voltage on pin TRXD0	star Idle and star Transmit mode	$0.7V_{BUF}$	$0.5V_{BUF}$	$V_{BUF} + 0.3$	V
$V_{IL(TRXD0)}$	LOW-level input voltage on pin TRXD0	star Idle and star Transmit mode	-0.3	$0.5V_{BUF}$	$0.3V_{BUF}$	V
$V_{OL(TRXD0)}$	LOW-level output voltage on pin TRXD0	$R_{pu} = 200\text{ }\Omega$	-0.3	+0.3	+0.8	V
$V_{IH(TRXD1)}$	HIGH-level input voltage on pin TRXD1	star Idle and star Transmit mode	$0.7V_{BUF}$	$0.5V_{BUF}$	$V_{BUF} + 0.3$	V
$V_{IL(TRXD1)}$	LOW-level input voltage on pin TRXD1	star Idle and star Transmit mode	-0.3	$0.5V_{BUF}$	$0.3V_{BUF}$	V
$V_{OL(TRXD1)}$	LOW-level output voltage on pin TRXD1	$R_{pu} = 200\text{ }\Omega$	-0.3	+0.3	+0.8	V
Pins BP and BM						
$V_{o(idle)(BP)}$	idle output voltage on pin BP	Normal, Receive only, star Idle, star Transmit and star Receive mode; $V_{TXEN} = V_{IO}$	$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
		Standby, go-to-sleep, Sleep, star Standby and star Sleep mode	-0.1	0	+0.1	V
$V_{o(idle)(BM)}$	idle output voltage on pin BM	Normal, receive only, star Idle, star Transmit and star Receive mode; $V_{TXEN} = V_{IO}$	$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
		Standby, go to sleep, Sleep, star Standby and star Sleep mode	-0.1	0	+0.1	V
$I_{o(idle)BP}$	idle output current on pin BP	$-60\text{ V} < V_{BP} < +60\text{ V}$	1	3	7.5	mA
$I_{o(idle)BM}$	idle output current on pin BM	$-60\text{ V} < V_{BM} < +60\text{ V}$	1	3	7.5	mA
$V_{o(idle)(dif)}$	differential idle output voltage		-25	0	+25	mV
$V_{OH(dif)}$	differential HIGH-level output voltage	$40\text{ }\Omega < R_{bus} < 55\text{ }\Omega$; $V_{CC} = V_{BUF} = 5\text{ V}$	600	800	1200	mV
$V_{OL(dif)}$	differential LOW-level output voltage	$40\text{ }\Omega < R_{bus} < 55\text{ }\Omega$; $V_{CC} = V_{BUF} = 5\text{ V}$	-1200	-800	-600	mV

Table 14. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BUF} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.^{[1][2]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH(dif)}$	differential HIGH-level input voltage	normal power modes; $-10\text{ V} < V_{BP} < +15\text{ V}$; $-10\text{ V} < V_{BM} < +15\text{ V}$	150	225	300	mV
$V_{IL(dif)}$	differential LOW-level input voltage	normal power modes; $-10\text{ V} < V_{BP} < +15\text{ V}$; $-10\text{ V} < V_{BM} < +15\text{ V}$	-300	-225	-150	mV
		low power modes; $-10\text{ V} < V_{BP} < +15\text{ V}$; $-10\text{ V} < V_{BM} < +15\text{ V}$	-400	-225	-125	mV
$ V_{I(dif)det(act)} $	activity detection differential input voltage (absolute value)	normal power modes	150	225	300	mV
$ I_{O(sc)(BP)} $	short-circuit output current on pin BP (absolute value)	$V_{BP} = 0\text{ V}, 60\text{ V}$	10	20	30	mA
$ I_{O(sc)(BM)} $	short-circuit output current on pin BM (absolute value)	$V_{BM} = 0\text{ V}, 60\text{ V}$	10	20	30	mA
$R_{i(BP)}$	input resistance on pin BP	Idle level; $R_{bus} = \infty\text{ }\Omega$	10	20	40	k Ω
$R_{i(BM)}$	input resistance on pin BM	Idle level; $R_{bus} = \infty\text{ }\Omega$	10	20	40	k Ω
$R_{i(dif)(BP-BM)}$	differential input resistance between pin BP and pin BM	Idle level; $R_{bus} = \infty\text{ }\Omega$	20	40	80	k Ω
$I_{LI(BP)}$	input leakage current on pin BP	$V_{BP} = 5\text{ V}$; $V_{BAT} = V_{CC} = V_{IO} = 0\text{ V}$	-10	0	+10	μA
$I_{LI(BM)}$	input leakage current on pin BM	$V_{BM} = 5\text{ V}$; $V_{BAT} = V_{CC} = V_{IO} = 0\text{ V}$	-10	0	+10	μA
$V_{cm(bus)(DATA_0)}$	DATA_0 bus common mode voltage	$R_{bus} = 45\text{ }\Omega$	$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
$V_{cm(bus)(DATA_1)}$	DATA_1 bus common mode voltage	$R_{bus} = 45\text{ }\Omega$	$0.4V_{BUF}$	$0.5V_{BUF}$	$0.6V_{BUF}$	V
$\Delta V_{cm(bus)}$	bus common mode voltage difference	$R_{bus} = 45\text{ }\Omega$	-25	0	+25	mV
Pin INH1						
$V_{OH(INH1)}$	HIGH-level output voltage on pin INH1	$I_{INH1} = -0.2\text{ mA}$	$V_{BAT} - 0.8$	$V_{BAT} - 0.3$	V_{BAT}	V
$I_{L(INH1)}$	leakage current on pin INH1	Sleep mode	-5	0	+5	μA
$I_{OL(INH1)}$	LOW-level output current on pin INH1	$V_{INH1} = 0\text{ V}$	-15	-8	-	mA

Table 14. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V}$ to 60 V ; $V_{CC} = 4.75\text{ V}$ to 5.25 V ; $V_{BUF} = 4.75\text{ V}$ to 5.25 V ; $V_{IO} = 2.2\text{ V}$ to 5.25 V ; $T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.^{[1][2]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin INH2						
$V_{OH(INH2)}$	HIGH-level output voltage on pin INH2	$I_{INH2} = -0.2\text{ mA}$	$V_{BAT} - 0.8$	$V_{BAT} - 0.3$	V_{BAT}	V
$I_{L(INH2)}$	leakage current on pin INH2	Sleep mode	-5	0	+5	μA
$I_{OL(INH2)}$	LOW-level output current on pin INH2	$V_{INH2} = 0\text{ V}$	-15	-8	-	mA
Pin WAKE						
$V_{th(det)(WAKE)}$	detection threshold voltage on pin WAKE	low power mode	2.5	3.7	4.5	V
$I_{IL(WAKE)}$	LOW-level input current on pin WAKE	$V_{WAKE} = 2.4\text{ V}$ for $t > t_{wake(WAKE)}$	3	6.5	11	μA
$I_{IH(WAKE)}$	HIGH-level input current on pin WAKE	$V_{WAKE} = 4.6\text{ V}$ for $t > t_{wake(WAKE)}$	-11	-6.5	-3	μA
Temperature protection						
$T_{j(warn)(medium)}$	medium warning junction temperature		155	165	175	$^{\circ}\text{C}$
$T_{j(dis)(high)}$	high disable junction temperature		180	190	200	$^{\circ}\text{C}$

- [1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % are tested at $125\text{ }^{\circ}\text{C}$ for dies on wafer level (pre-testing) and above this for cased products 100 % are tested at $T_{amb} = -40\text{ }^{\circ}\text{C}$ and $+25\text{ }^{\circ}\text{C}$ (final testing) unless otherwise specified. Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range. For bare dies all parameters are only guaranteed with the backside of the bare die connected to ground.
- [2] At power-up V_{BAT} should be supplied first. When V_{BAT} reaches 6.5 V , V_{CC} and V_{IO} may be switched on with a delay of at least $60\text{ }\mu\text{s}$ with respect to V_{BAT} .
- [3] Current flows from V_{CC} to V_{BUF} . This means that the maximum sum current $I_{CC} + I_{BUF}$ is 35 mA .

11. Dynamic characteristics

Table 15. Dynamic characteristics

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BUF} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC^[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pins BP and BM						
$t_{d(\text{TXD-bus})}$	delay time from TXD to bus	Normal or star Transmit mode	[2]			
		DATA_0	-	31	50	ns
		DATA_1	-	32	50	ns
$\Delta t_{d(\text{TXD-bus})}$	delay time difference from TXD to bus	Normal or star Transmit mode; between DATA_0 and DATA_1	[2]	1	4	ns
$t_{d(\text{TRXD-bus})}$	delay time from TRXD to bus	star Transmit mode	[3]			
		DATA_0	-	27	50	ns
		DATA_1	-	28	50	ns
$\Delta t_{d(\text{TRXD-bus})}$	delay time difference from TRXD to bus	star Transmit mode; between DATA_0 and DATA_1	[3][4]	1	5	ns
$t_{d(\text{bus-RXD})}$	delay time from bus to RXD	normal or star Transmit mode; $C_{RXD} = 15\text{ pF}$; see Figure 11				
		DATA_0	-	28	50	ns
		DATA_1	-	30	50	ns
$\Delta t_{d(\text{bus-RXD})}$	delay time difference from bus to RXD	normal or star Transmit mode; $C_{RXD} = 15\text{ pF}$; between DATA_0 and DATA_1; see Figure 11	-	2	5	ns
$t_{d(\text{bus-TRXD})}$	delay time from bus to TRXD	star Receive mode; see Figure 11				
		DATA_0	-	28	50	ns
		DATA_1	-	28	50	ns
$\Delta t_{d(\text{bus-TRXD})}$	delay time difference from bus to TRXD	star Receive mode; between DATA_0 and DATA_1; see Figure 11	[4]	0	5	ns
$t_{d(\text{TXEN-busidle})}$	delay time from TXEN to bus idle	Normal mode	-	28	50	ns
$t_{d(\text{TXEN-busact})}$	delay time from TXEN to bus active	Normal mode	-	22	50	ns
$t_{d(\text{BGE-busidle})}$	delay time from BGE to bus idle	Normal mode	-	30	50	ns
$t_{d(\text{BGE-busact})}$	delay time from BGE to bus active	Normal mode	-	22	50	ns
$t_{r(\text{dif})(\text{bus})}$	bus differential rise time	10 % to 90 %; $R_L = 45\text{ }\Omega$; $C_L = 100\text{ pF}$	8	12	23	ns
$t_{f(\text{dif})(\text{bus})}$	bus differential fall time	90 % to 10 %; $R_L = 45\text{ }\Omega$; $C_L = 100\text{ pF}$	8	12	23	ns

Table 15. Dynamic characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BUF} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC^[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
WAKE symbol detection						
$t_{det(wake)DATA_0}$	DATA_0 wake-up detection time	Standby, Sleep, star Standby or star Sleep mode; $-10\text{ V} < V_{BP} < +15\text{ V}$; $-10\text{ V} < V_{BM} < +15\text{ V}$	1	2.2	4	μs
$t_{det(wake)idle}$	idle wake-up detection time		1	2.5	4	μs
$t_{det(wake)tot}$	total wake-up detection time		50	-	115	μs
Undervoltage						
$t_{det(uv)(VCC)}$	undervoltage detection time on pin V_{CC}		100	-	670	ms
$t_{rec(uv)(VCC)}$	undervoltage recovery time on pin V_{CC}		1	-	5.2	ms
$t_{det(uv)(VIO)}$	undervoltage detection time on pin V_{IO}		100	-	670	ms
$t_{to(uv)(VCC)}$	undervoltage time-out time on pin V_{CC} for entering Standby mode	star configuration; wake flag is set	432	-	900	μs
Activity detection						
$t_{det(act)(TXEN)}$	activity detection time on pin TXEN	star configuration	100	140	200	ns
$t_{det(act)(TRXD)}$	activity detection time on pin TRXD	star configuration	100	140	200	ns
$t_{det(act)(bus)}$	activity detection time on bus pins	V_{dif} : 0 \rightarrow 400 mV	100	150	250	ns
$t_{det(idle)(TXEN)}$	idle detection time on pin TXEN	star configuration	100	140	200	ns
$t_{det(idle)(TRXD)}$	idle detection time on pin TRXD	star configuration	50	75	100	ns
$t_{det(idle)(bus)}$	idle detection time on bus pins	V_{dif} : 400 mV \rightarrow 0	100	150	250	ns
Star modes						
$t_{to(idle-sleep)}$	idle to sleep time-out time		640	-	2660	ms
$t_{to(tx-locked)}$	transmit to locked time-out time		2600	-	10400	μs
$t_{to(rx-locked)}$	receive to locked time-out time		2600	-	10400	μs
$t_{to(locked-sleep)}$	locked to sleep time-out time		64	-	333	ms
$t_{to(locked-idle)}$	locked to idle time-out time		1.4	-	5.1	μs
Node modes						
$t_d(STBN-RXD)$	STBN to RXD delay time	wake flag set	-	1	2	μs
$t_d(STBN-INH2)$	STBN to INH2 delay time		-	3	10	μs
$t_h(gotosleep)$	go-to-sleep hold time		20	35	50	μs
Status register						
$t_{det}(EN)$	detection time on pin EN	for mode control	20	-	80	μs
T_{EN}	time period on pin EN	for reading status bits	4	-	20	μs
$t_d(EN-ERRN)$	delay time from EN to ERRN	for reading status bits	-	0.8	2	μs

Table 15. Dynamic characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{BUF} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$; $R_{TRXD} = 200\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC^[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
WAKE						
$t_{\text{wake(WAKE)}}$	wake-up time on pin WAKE	low power mode; falling edge on pin WAKE; $6.5\text{ V} < V_{BAT} < 27\text{ V}$	5	25	100	μs
		low power mode; falling edge on pin WAKE; $27\text{ V} < V_{BAT} < 60\text{ V}$	25	75	175	μs
Miscellaneous						
$t_{\text{detCL(TXEN_BGE)}}$	TXEN_BGE clamp detection time		2600	-	10400	μs

- [1] At power-up V_{BAT} should be supplied first. When V_{BAT} reaches 6.5 V, V_{CC} and V_{IO} may be switched on with a delay of at least 60 μs with respect to V_{BAT} .
- [2] Rise and fall time (10 % to 90 %) of $t_{r(\text{TXD})}$ and $t_{f(\text{TXD})} = 5\text{ ns}$.
- [3] Rise and fall time (10 % to 90 %) of $t_{r(\text{TRXD})}$ and $t_{f(\text{TRXD})} = 5\text{ ns}$.
- [4] The worst case asymmetry from one branch to another is the sum of the delay difference from TRXD0 and TRXD1 to DATA_0 and DATA_1 plus the delay difference from DATA_0 and DATA_1 to TRXD0 and TRXD1. The TJA1080 should not be used in topologies with cascaded stars.

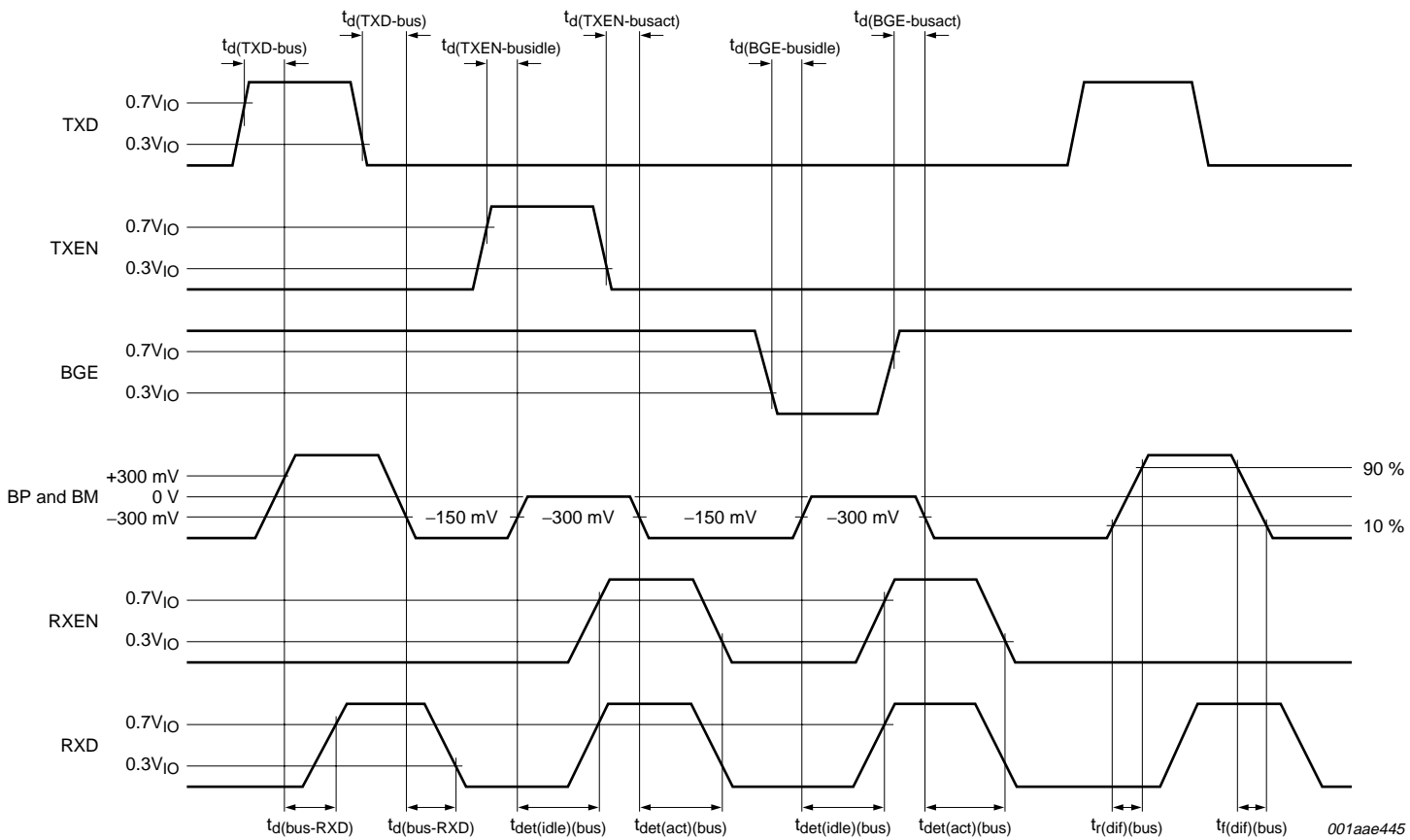
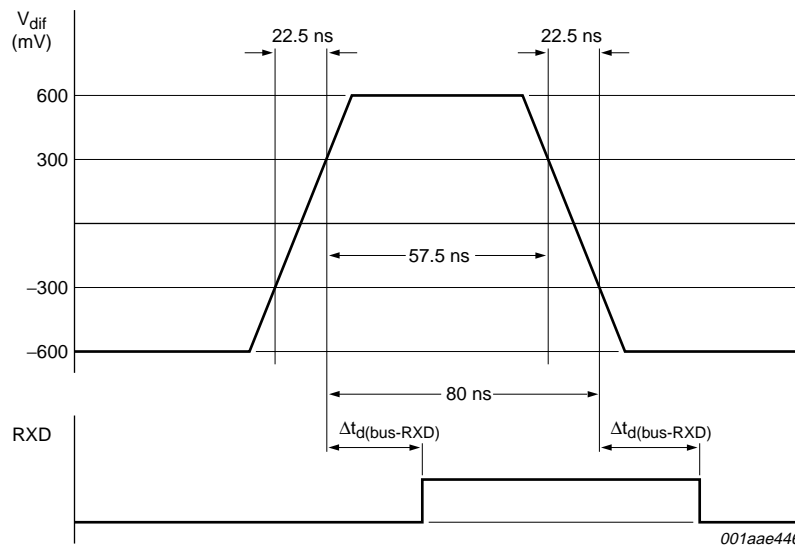
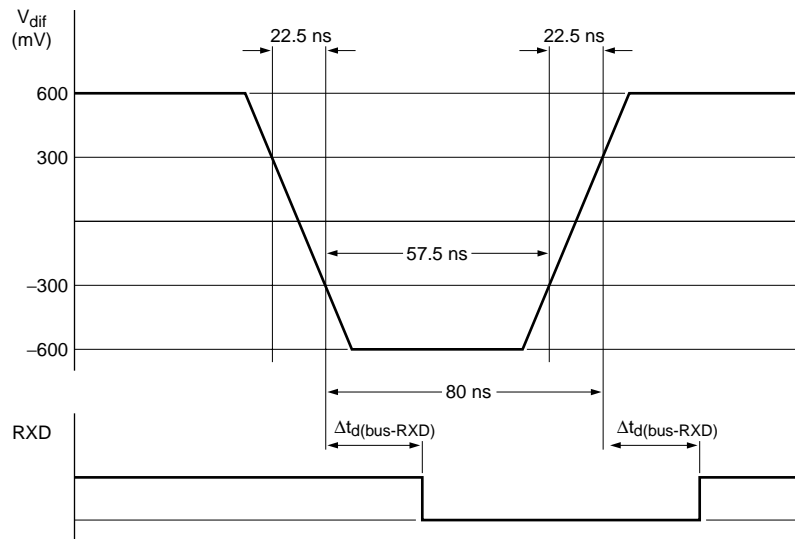


Fig 10. Detailed timing diagram in node configuration



001aae446

V_{dif} is the receiver test signal.

Fig 11. Receiver test signal

12. Test information

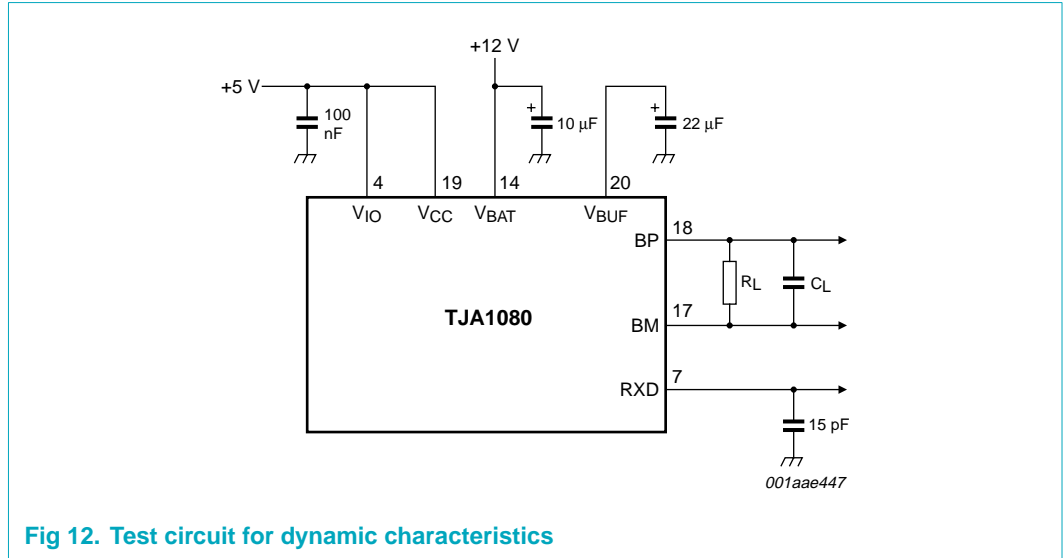


Fig 12. Test circuit for dynamic characteristics

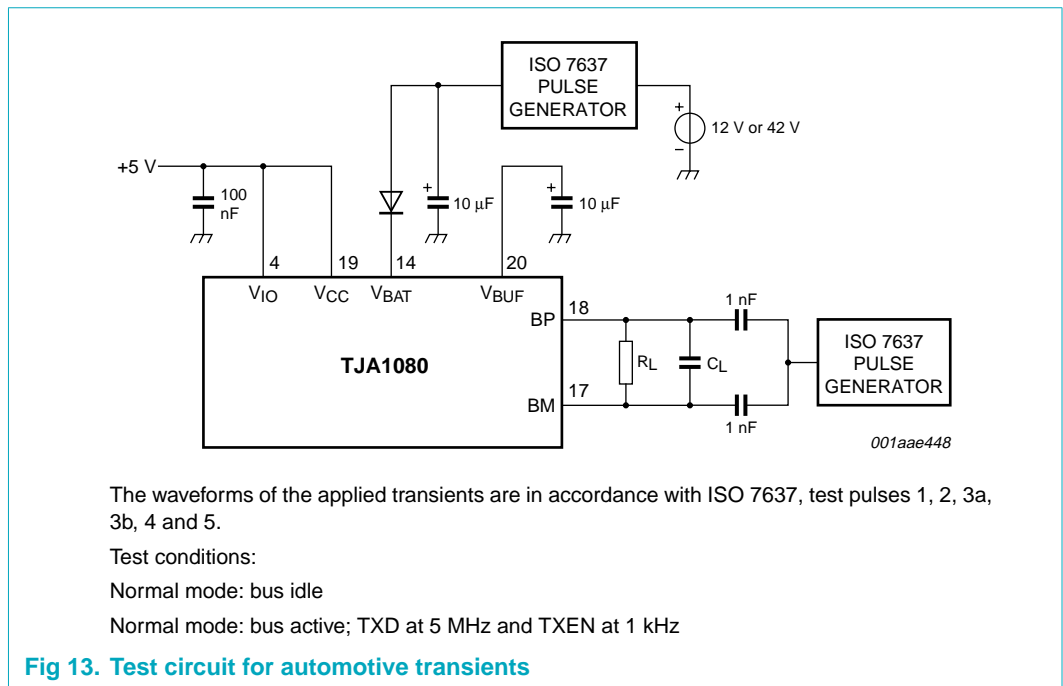


Fig 13. Test circuit for automotive transients

13. Package outline

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

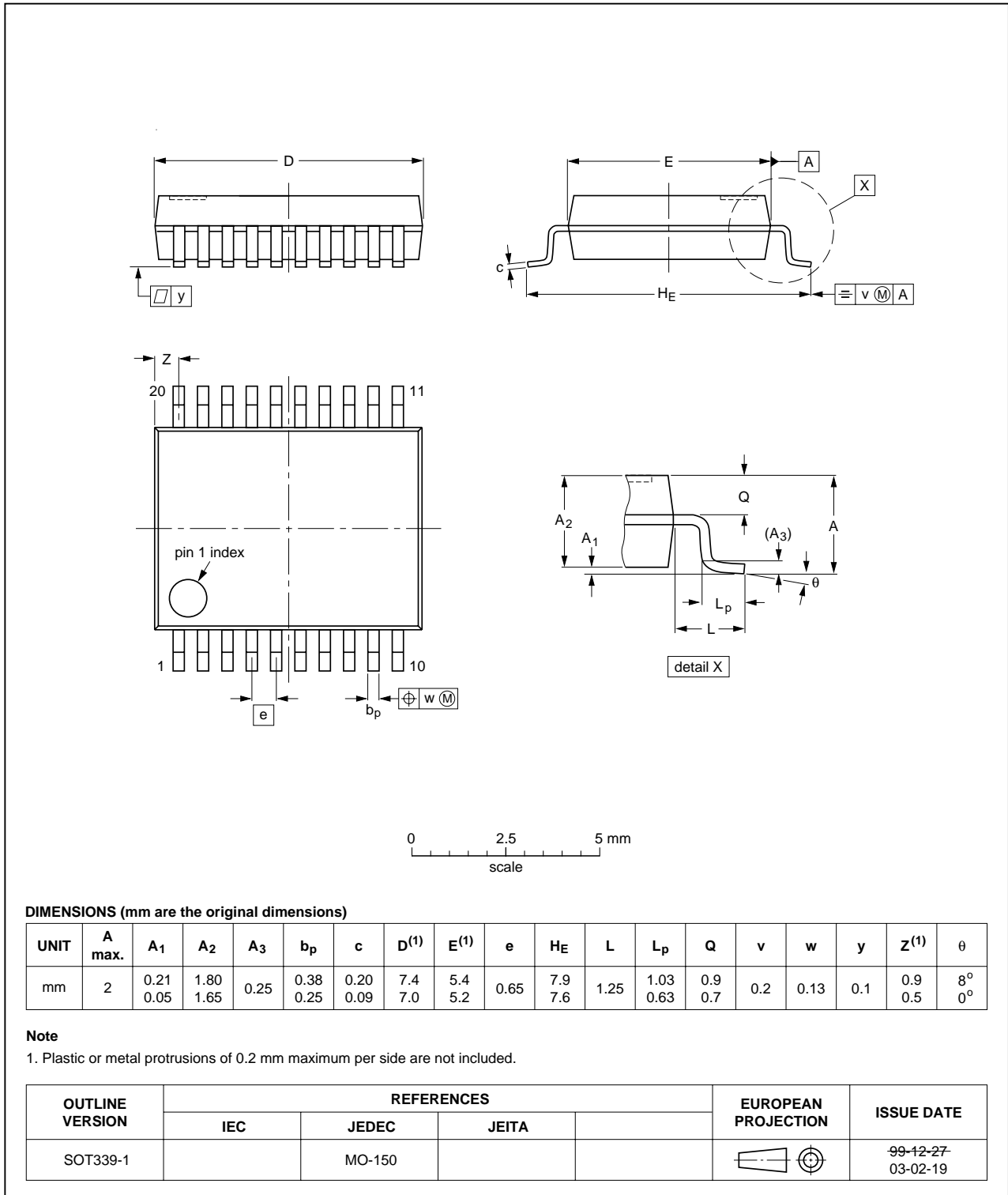


Fig 14. Package outline SOT339-1 (SSOP20)

14. Soldering

14.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 16. SnPb eutectic process - package peak reflow temperatures (from J-STD-020C July 2004)

Package thickness	Volume mm ³ < 350	Volume mm ³ ≥ 350
< 2.5 mm	240 °C + 0/-5 °C	225 °C + 0/-5 °C
≥ 2.5 mm	225 °C + 0/-5 °C	225 °C + 0/-5 °C

Table 17. Pb-free process - package peak reflow temperatures (from J-STD-020C July 2004)

Package thickness	Volume mm ³ < 350	Volume mm ³ 350 to 2000	Volume mm ³ > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 18. Suitability of surface mount IC packages for wave and reflow soldering methods

Package ^[1]	Soldering method	
	Wave	Reflow ^[2]
BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ^[4]	suitable
PLCC ^[5] , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ^{[5][6]}	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ^[7]	suitable
CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding $217\text{ °C} \pm 10\text{ °C}$ measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 19. Abbreviations

Abbreviation	Description
CAN	Communications Area Network
CDM	Charge Device Model
EMC	ElectroMagnetic Compatibility
EME	ElectroMagnetic Emission
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PWON	Power-on

16. References

- [1] **EPL** — FlexRay Communications System Electrical Physical Layer Specification Version 2.1 Rev. A, FlexRay Consortium, Dec 2005
- [2] **PS41** — Product Specification: TJA1041; High speed CAN transceiver, www.semiconductors.philips.com
- [3] **PS54** — Product Specification: TJA1054; Fault-tolerant CAN transceiver, www.semiconductors.philips.com

17. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1080_1	20060720	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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