THC63LVD104A

90MHz 30Bits COLOR LVDS Receiver

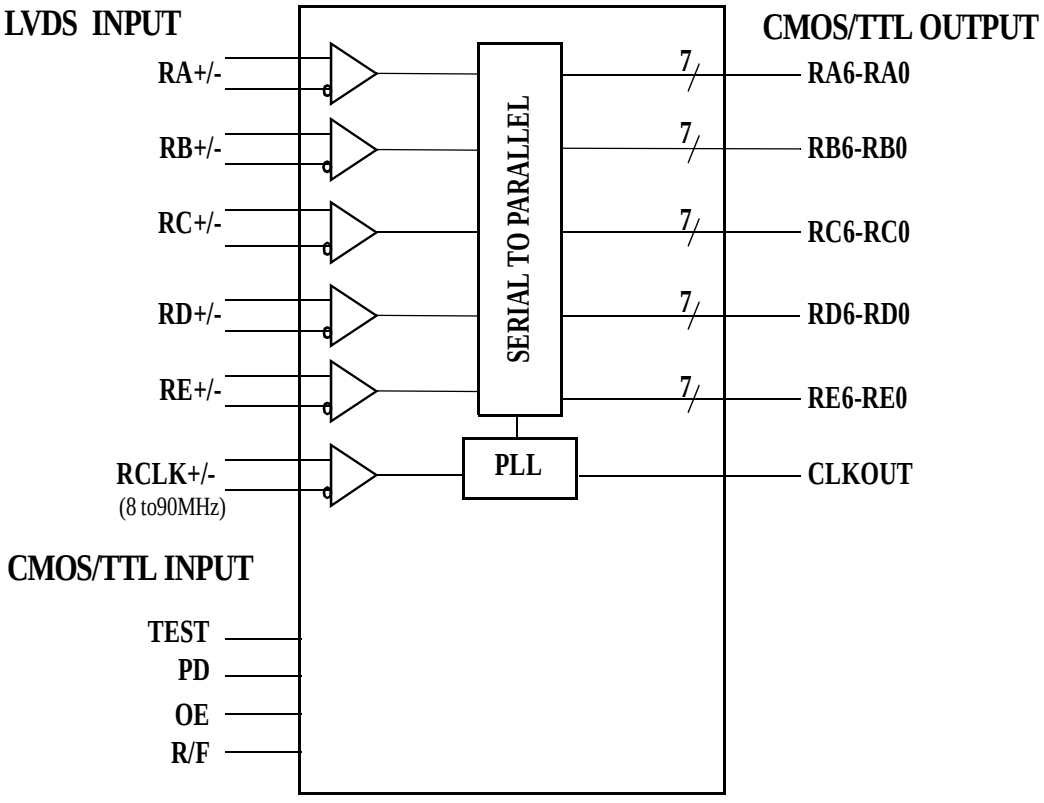
General Description

The THC63LVD104A receiver is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to WXGA resolutions. The THC63LVD104A converts the LVDS data streams back into 35bits of CMOS/TTL data with rising edge or falling edge clock for convenient with a variety of LCD panel controllers.At a transmit clock frequency of 90MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC,VSYNC,DE,CNTL1,CNTL2) are transmitted at an effective rate of 630Mbps per LVDS channel.Using a 90MHz clock, the data throughput is 394Mbytes per second.

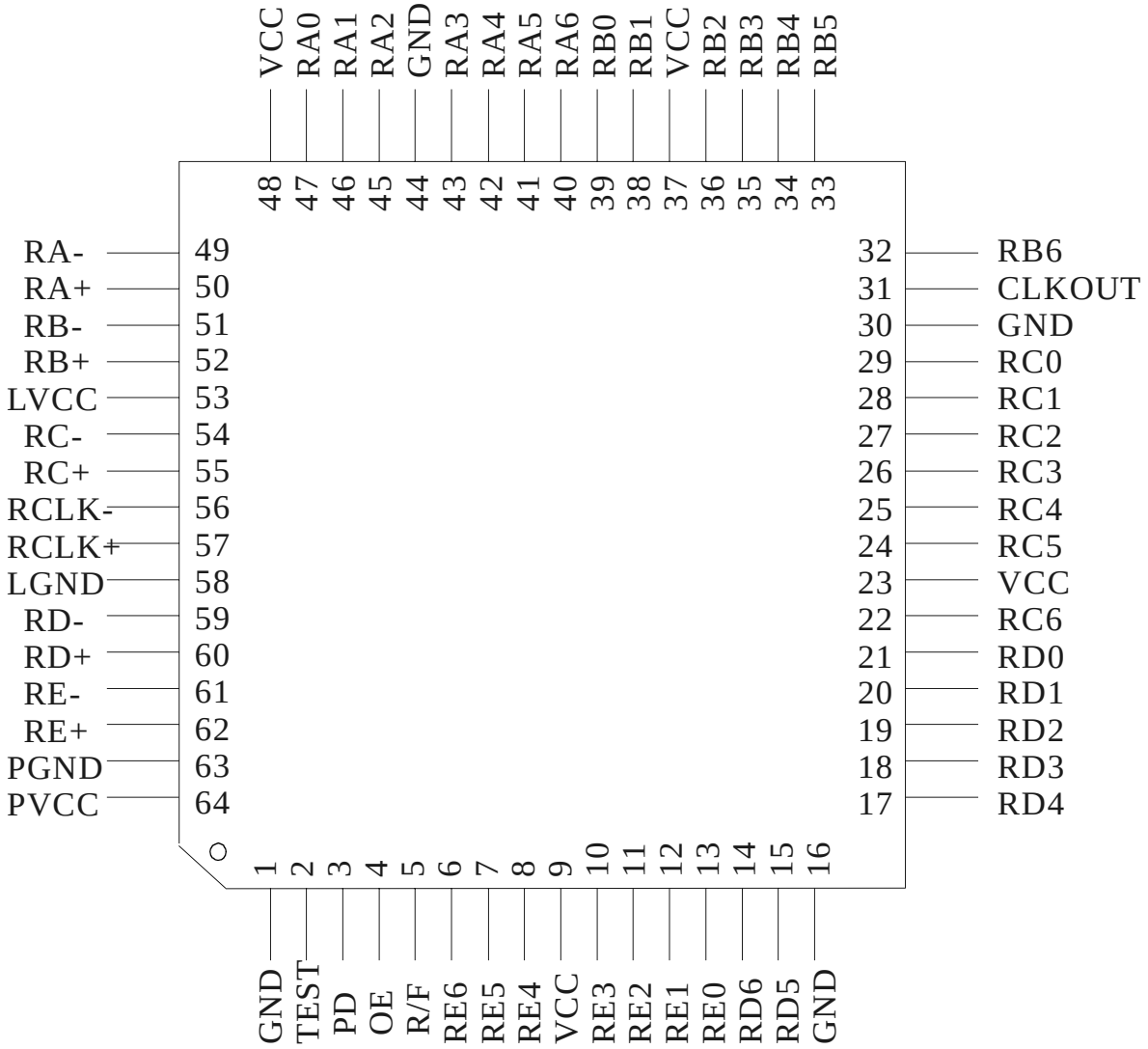
Features

- Wide dot clock range: 8-90MHz suited for NTSC, VGA, SVGA, XGA, and WXGA
- PLL requires no external components
- 50% output clock duty cycle
- TTL clock edge programmable
- Power down mode
- Low power single 3.3V CMOS design
- 64pin TQFP
- Backward compatible with THC63LVDF64x (18bits) / F84x(24bits)

Block Diagram



Pin Out



Pin Description

Pin Name	Pin #	Type	Description
RA+, RA-	50, 49	LVDS IN	LVDS Data In.
RB+, RB-	52, 51	LVDS IN	
RC+, RC-	55, 54	LVDS IN	
RD+, RD-	60, 59	LVDS IN	
RE+,RE-	62, 61	LVDS IN	
RCLK+, RCLK-	57, 56	LVDS IN	LVDS Clock In.
RA6 ~ RA0	40,41,42,43,45,46,47	OUT	CMOS/TTL Data Outputs.
RB6 ~ RB0	32,33,34,35,36,38,39	OUT	
RC6 ~ RC0	22,24,25,26,27,28,29	OUT	
RD6 ~ RD0	14,15,17,18,19,20,21	OUT	
RE6 ~ RE0	6,7,8,10,11,12,13	OUT	
TEST	2	IN	Test pin, must be “L” for normal operation.
PD	3	IN	H: Normal operation, L: Power down (all outputs are “L”)
OE	4	IN	H:Output enable (Normal operation). L:Output disable(all outputs are Hi-Z)
R/F	5	IN	Output Clock Triggering Edge Select. H: Rising edge, L: Falling edge
VCC	9,23,37,48	Power	Power Supply Pins for TTL outputs and digital circuitry.
CLKOUT	31	OUT	Clock out.
GND	1,16,30,44	Ground	Ground Pins for TTL outputs and digital circuitry.
LVCC	53	Power	Power Supply Pin for LVDS inputs.
LGND	58	Ground	Ground Pin for LVDS inputs.
PVCC	64	Power	Power Supply Pin for PLL circuitry.
PGND	63	Ground	Ground Pin for PLL circuitry.

PD	R/F	OE	Data Outputs (Rxn)	CLKOUT
0	0	0	Hi-Z	Hi-Z
0	0	1	All 0	Fixed Low
0	1	0	Hi-Z	Hi-Z
0	1	1	All 0	Fixed Low
1	0	0	Hi-Z	Hi-Z
1	0	1	Data Out	It latches output data on falling edge.
1	1	0	Hi-Z	Hi-Z
1	1	1	Data Out	It latches output data on rising edge.

** Rxn

x = A,B,C,D,E

n = 0,1,2,3,4,5,6

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Resistance to soldering heat	+260°C /10sec
Maximum Power Dissipation @+25°C	1.0W

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH}= -4mA (data) I_{OH}= -8mA (clock)	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}= 4mA (data) I_{OL}= 8mA (clock)			0.4	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	µA

LVDS Receiver DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input High Threshold	V_{OC}= 1.2V			100	mV
V_{TL}	Differential Input Low Threshold	V_{OC}= 1.2V	-100			mV
I_{INL}	Input Current	V_{IN}= 2.4V / 0V V_{CC}= 3.6V			±20	µA

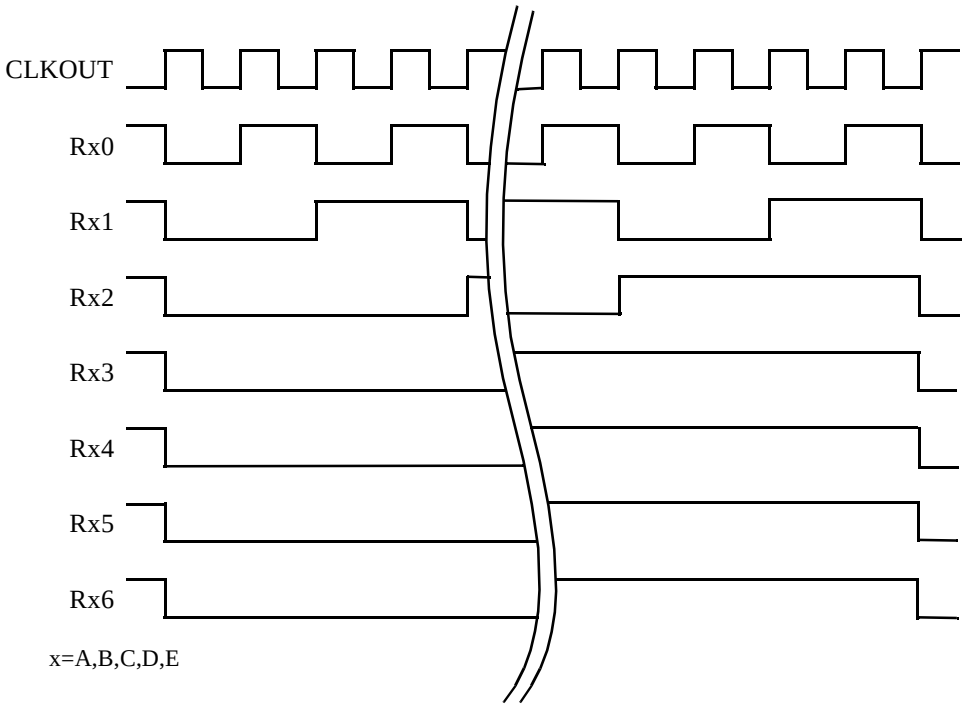
1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Supply Current

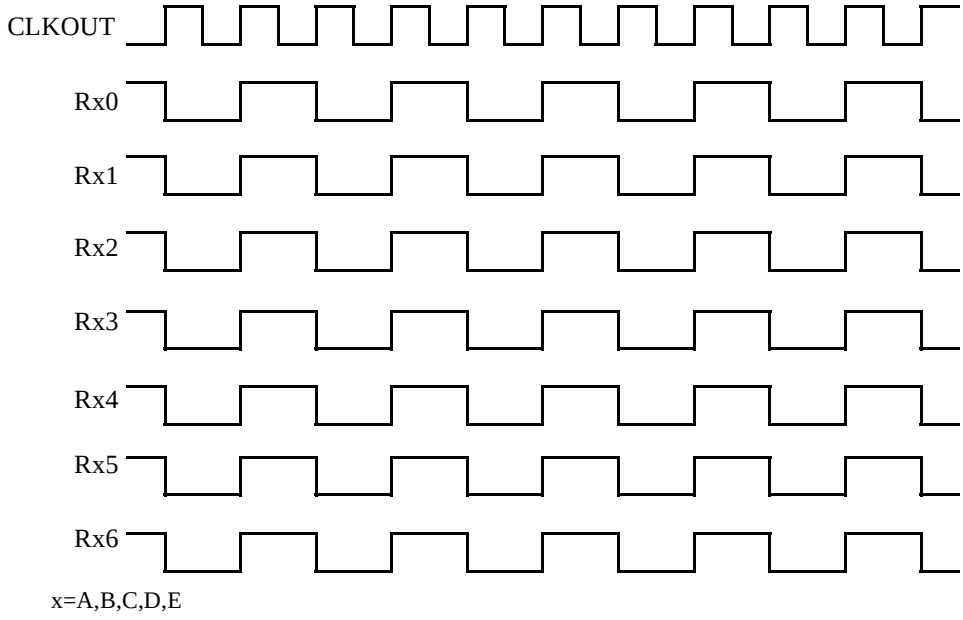
V_{CC} = 3.0V ~ 3.6V, Ta = 0 °C ~ +70 °C

Symbol	Parameter	Conditions		Typ.	Max.	Units
I_{RCCG}	Receiver Supply Current (Gray Scale Pattern)	f_{CLKOUT} = 90MHz	CL=8pF, Vcc=3.3V	70		mA
I_{RCCW}	Receiver Supply Current (Checker Pattern)	f_{CLKOUT} = 90MHz	CL=8pF, Vcc=3.3V	112		mA
I_{RCCS}	Receiver Power Down Supply Current	PD = L			10	µA

Incremental Pattern(Gray Scale)



Toggle Pattern(Checker)



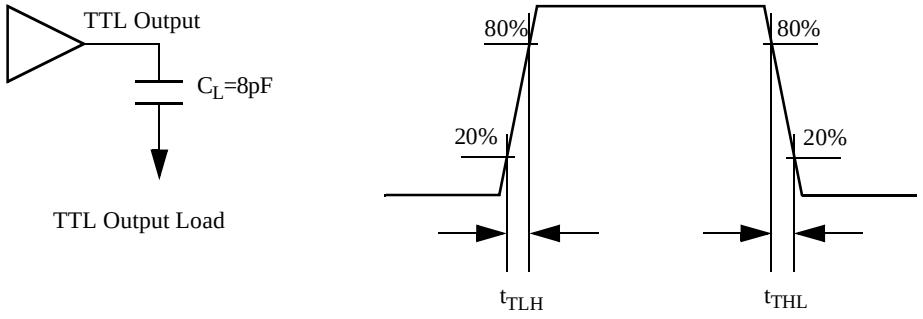
Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = 0 °C ~ +70 °C

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RCP}	CLKOUT Period	11.1	T	125.0	ns
t_{RCH}	CLKOUT High Time		$\frac{T-1}{2}$		ns
t_{RCL}	CLKOUT Low Time		$\frac{T-1}{2}$		ns
t_{RS}	TTL Data Setup to CLKOUT	t_{RCP} - 7.0			ns
t_{RH}	TTL Data Hold from CLKOUT	1.0			ns
t_{TLH}	TTL Low to High Transition Time		1.0	2.0	ns
t_{THL}	TTL High to Low Transition Time		1.0	2.0	ns
t_{RIP1}	Input Data Position0	-0.25	0.0	+0.25	ns
t_{RIP0}	Input Data Position1	$\frac{t_{RCIP}}{7} - 0.25$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP6}	Input Data Position2	$2\frac{t_{RCIP}}{7} - 0.25$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP5}	Input Data Position3	$3\frac{t_{RCIP}}{7} - 0.25$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP4}	Input Data Position4	$4\frac{t_{RCIP}}{7} - 0.25$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP3}	Input Data Position5	$5\frac{t_{RCIP}}{7} - 0.25$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP2}	Input Data Position6	$6\frac{t_{RCIP}}{7} - 0.25$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RPLL}	Phase Lock Loop Set			10.0	ms
t_{RCIP}	CLKIN Period	11.1		125.0	ns

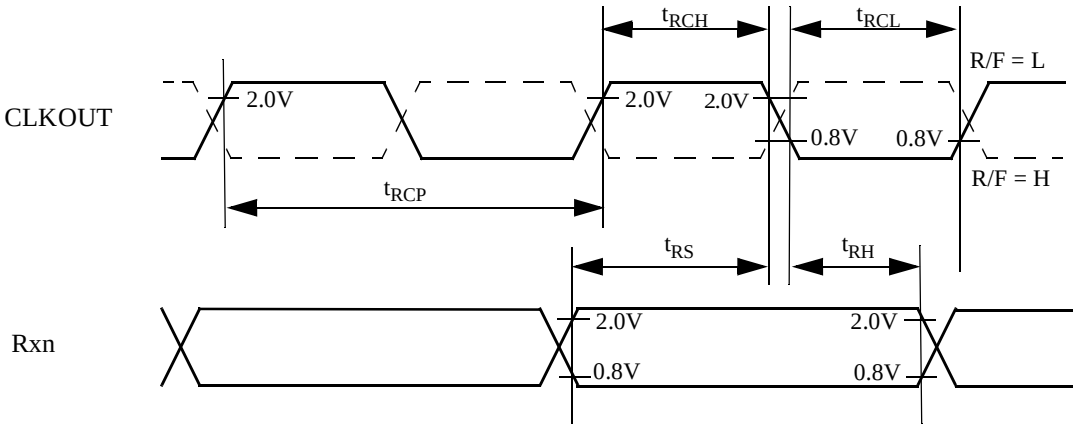
AC Timing Diagrams

TTL Outputs



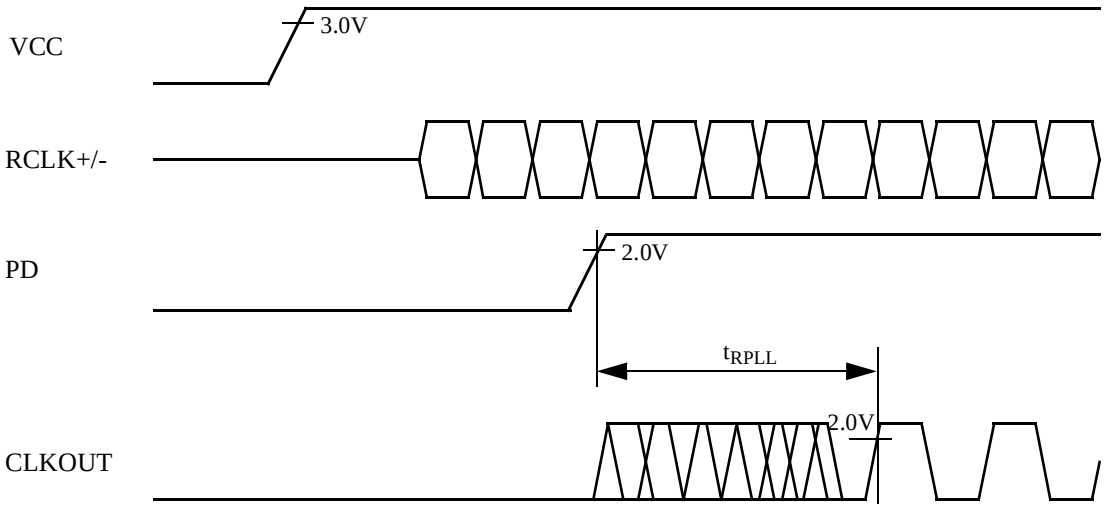
AC Timing Diagrams

TTL Outputs



x = A,B,C,D,E
n = 0,1,2,3,4,5,6

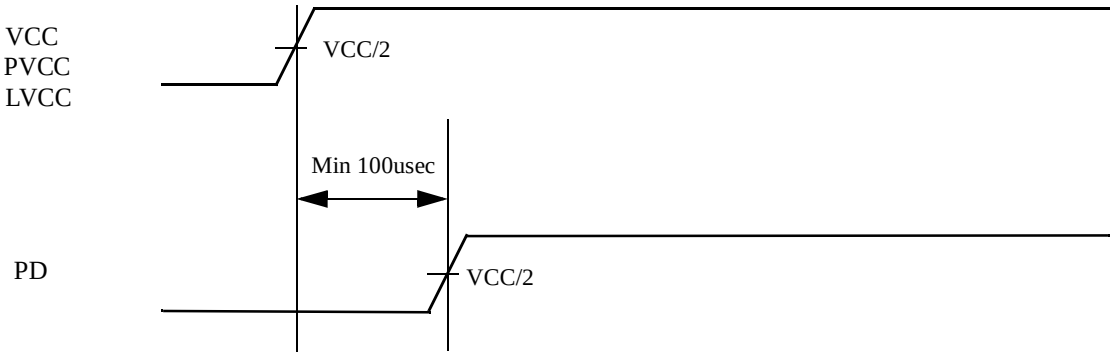
Phase Lock Loop Set Time



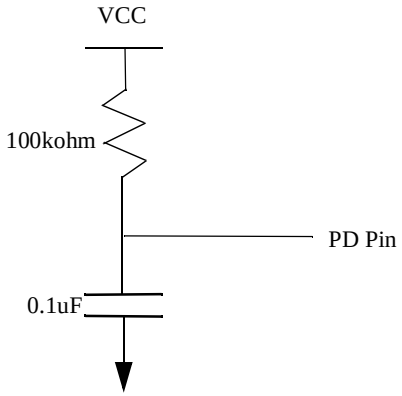
Power Up Sequence

Power Up Sequence must be Sequence1 or Sequence2.

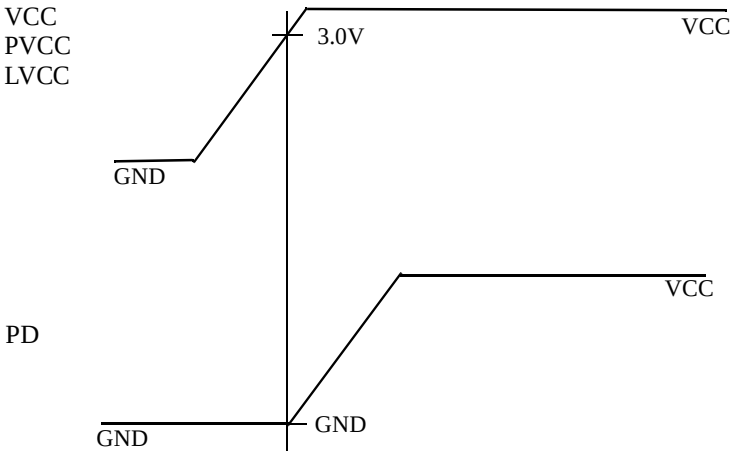
1)Sequence1



Recommended PD Pin Circuit



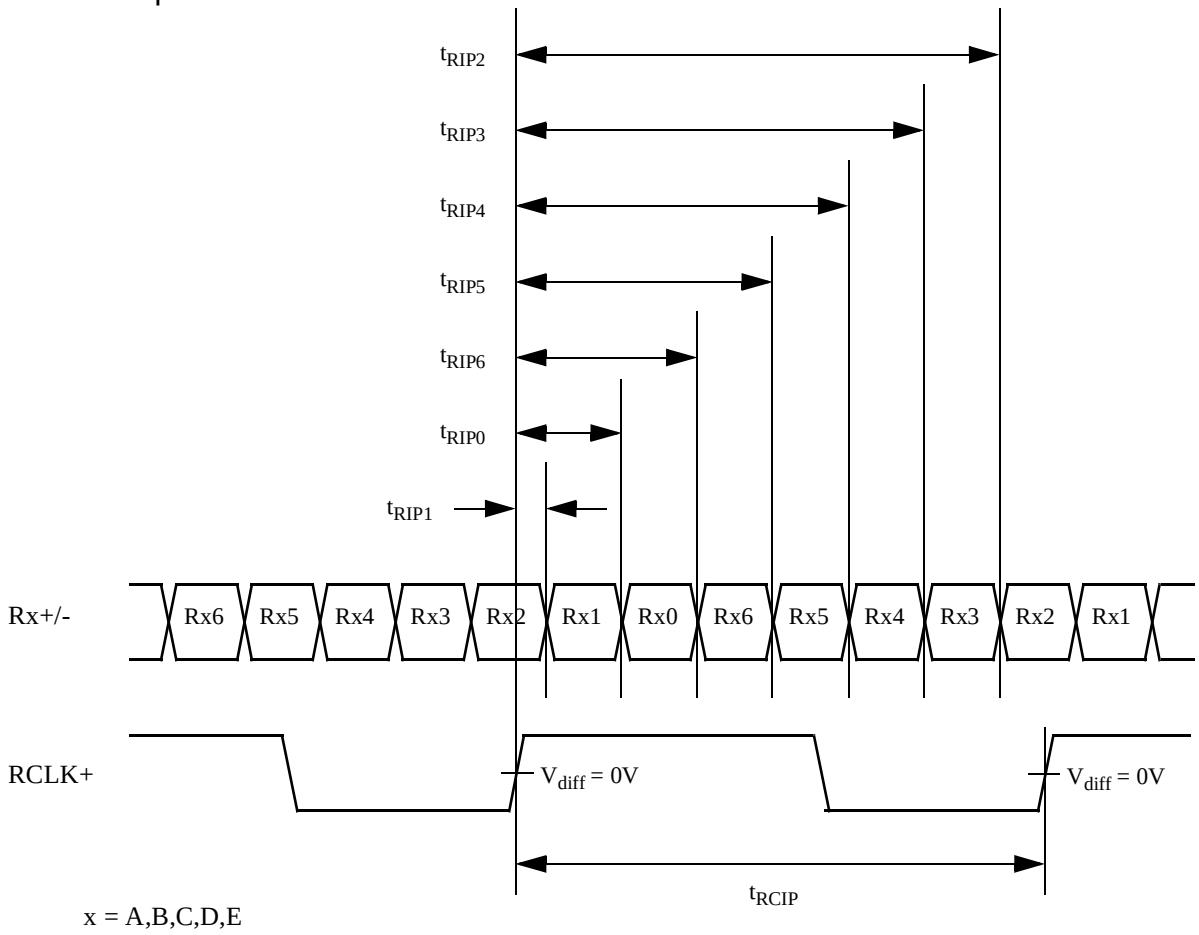
2)Sequence2



PD pin must be High after VCC voltage is 3.0V.

AC Timing Diagrams

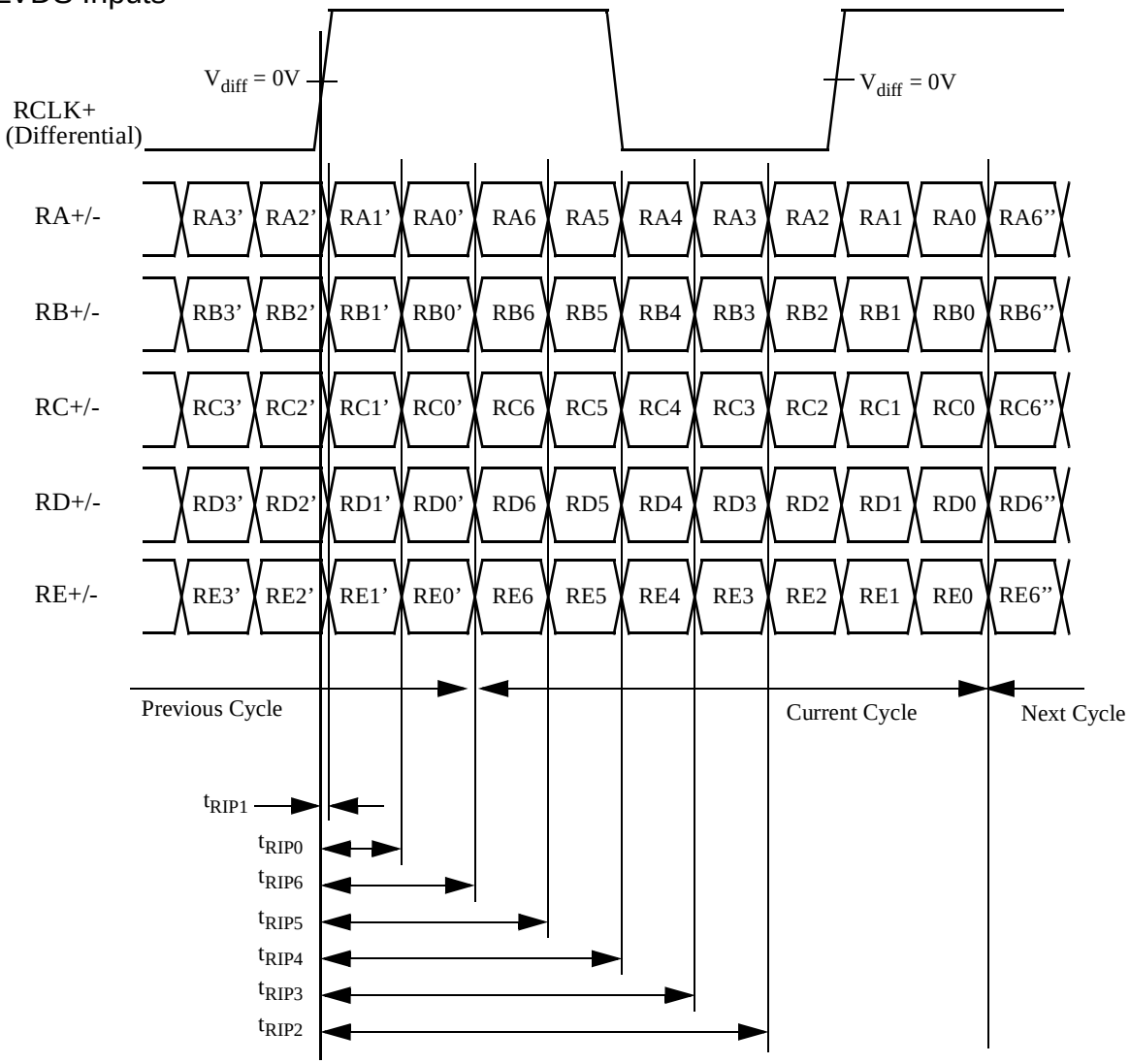
LVDS Inputs



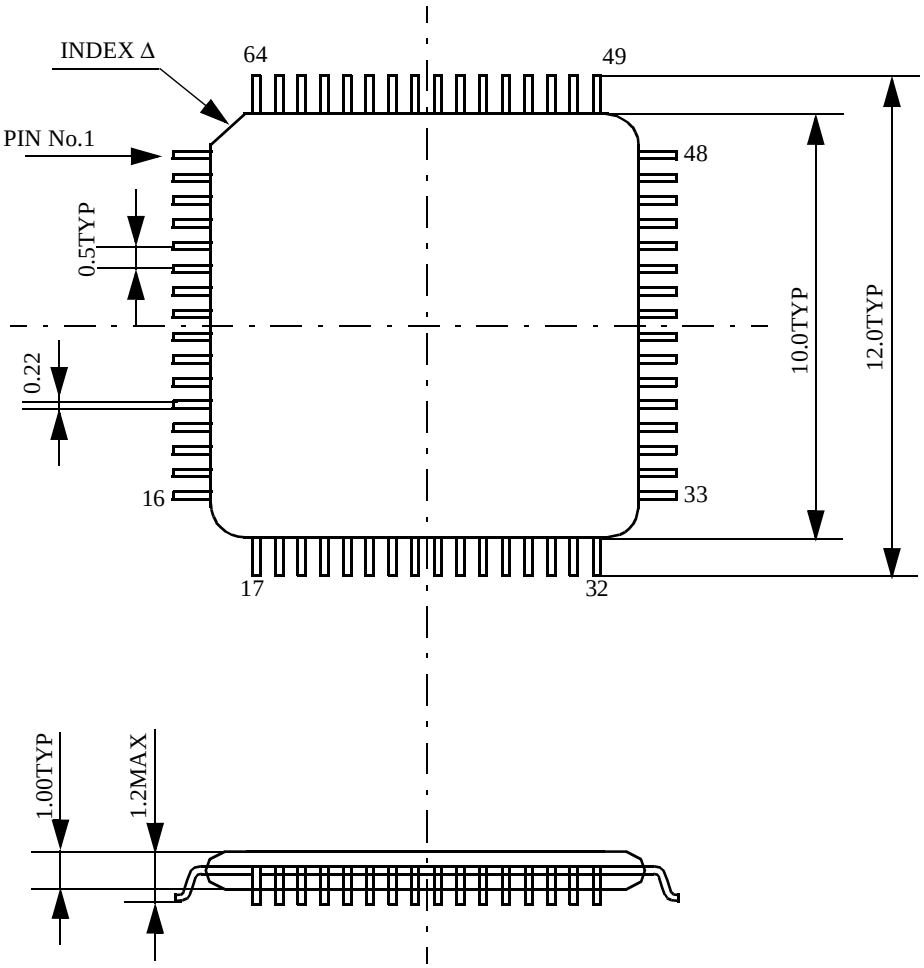
x = A,B,C,D,E

AC Timing Diagrams

LVDS Inputs



Package



UNITS: mm

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6. No radiation-hardened design is incorporated in THC63LVD104A.
7. Judgment on whether THC63LVD104A comes under strategic products prescribed by the Foreign Exchange and Foreign Trade Control Law is the user's responsibility.
8. This technical document was provisionally created during development of THC63LVD104A, so there is a possibility of differences between it and the product's final specifications. When designing circuits using THC63LVD104A, be sure to refer to the final technical documents.

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