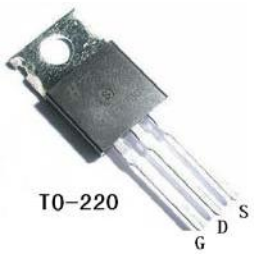
SAMWIN SW50N06

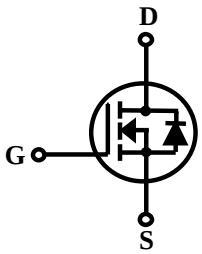
Features

- N-Channel MOSFET
- BV_{DSS} (Minimum) : 60 V
- $R_{DS(ON)}$ (Maximum) : 0.023ohm
- I_D : 50 A
- Qg (Typical) : 30 nc
- P_D (@TC=25 ℃) : 130 W

General Description

This power MOSFET is produced in CHMC with advanced VDMOS process, planar stripe. This technology enable power MOSFET to have better characteristics, such as fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics. It is mainly suitable for half bridge or full bridge resonant topology like a electronic ballast, and also low power switching mode power appliances.





Absolute Maximum Ratings

Symbol	Parameter		Value	Units
V_{DSS}	Drain to Source Voltage		60	V
I_D	Continuous Drain Current (@Tc=25℃)		50	A
	Continuous Drain Current (@Tc=100℃)		35	A
I_{DM}	Drain Current Pulsed	(Note 1)	200	A
V_{GS}	Gate to Source Voltage		±20	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	480	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7	V/ns
P_D	Total Power Dissipation (@Tc=25℃)		130	W
	Derating Factor above 25℃		0.9	W/℃
T_{STG},T_J	Operating junction temperature &Storage temperature		-55 ~ +150	℃
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	℃

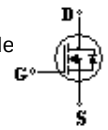
Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	-	1.15	℃/ W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	-	0.5	-	℃/ W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	62.5	℃/ W

Electrical Characteristics (Tc=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Value			Units
			Min	Typ	Max	
Off Characteristics						
BV_{DSS}	Drain- Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	60	-	-	V
△BV_{DSS}/△Tj	Breakdown Voltage Temperature coefficient	I_D=250uA,referenced to 25℃	-	0.07	-	V/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=60V, V_{GS}=0V	-	-	1	uA
		V_{DS}=48V, Tc=125℃				
I_{GSS}	Gate-Source Leakage Current	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
	Gate-Source Leakage Reverse	V_{GS}=-20V, V_{DS}=0V	-	-	-100	nA
On Characteristics						
V_{GS}(th)	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250uA	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-state Resistance	V_{GS}=10V,I_D=25A	-	0.018	0.023	ohm
Dynamic Characteristics						
Ciss	Input Capacitance	V_{GS}=0V,V_{DS}=25V, f=1MHz	-	900	1220	pF
Coss	Output Capacitance		-	430	550	
Crss	Reverse Transfer Capacitance		-	80	100	
Dynamic Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=30V,I_D=25A R_G=50ohm (Note4,5)	-	40	60	ns
t_r	Rise Time		-	100	200	
$t_{d(off)}$	Turn-off Delay Time		-	90	180	
t_f	Fall Time		-	80	160	
Q_g	Total Gate Charge	V_{DS}=48V,V_{GS}=10V, I_D=50A (Note4,5)	-	30	40	nc
Q_{gs}	Gate-Source Charge		-	9.6	-	
Q_{gd}	Gate-Drain Charge (Miller Charge)		-	10	-	

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
I_S	Continuous Source Current	Integral Reverse p-n Junction Diode in the MOSFET 	-	-	50	A
I_{SM}	Pulsed Source Current		-	-	200	
V_{SD}	Diode Forward Voltage	I_S=50A,V_{GS}=0V	-	-	1.5	V
t_{rr}	Reverse Recovery Time	I_S=50A,V_{GS}=0V, dI_F/dt=100A/us	-	54	-	ns
Q_{rr}	Reverse Recovery Charge		-	81	-	uc

※NOTES

1. Repeativity rating: pulse width limited by junction temperature
2. L=5.6mH,I_{AS}=50A,V_{DD}=25V,RG=0ohm, Starting TJ=25℃
3. I_{SD}≤50A,di/dt≤300A/us,V_{DD}≤BV_{DSS}, Starting TJ=25℃
4. Pulse Test: Pulse Width≤300us,Duty Cycle≤2%
5. Essentially independent of operating temperature.

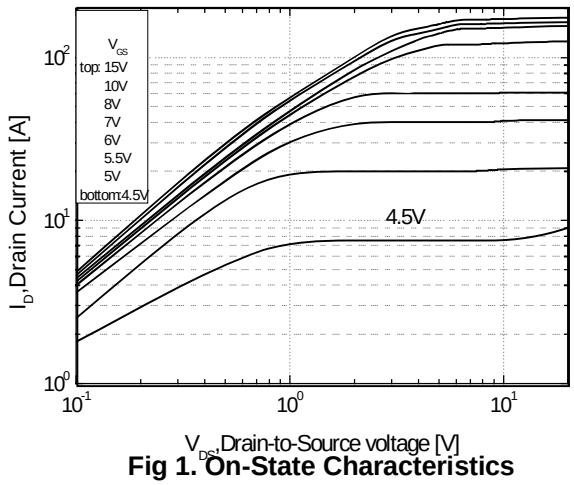


Fig 1. On-State Characteristics

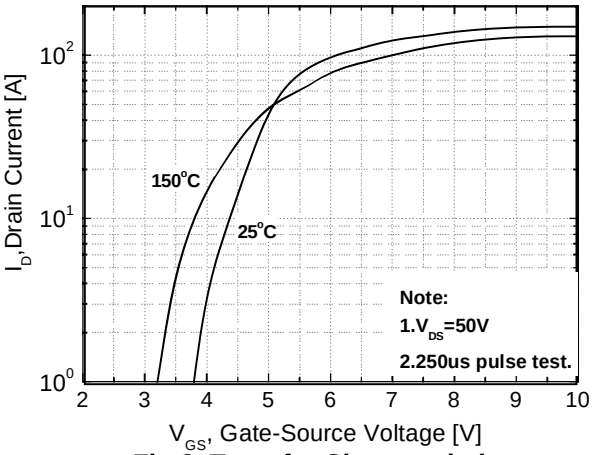


Fig 2. Transfer Characteristics

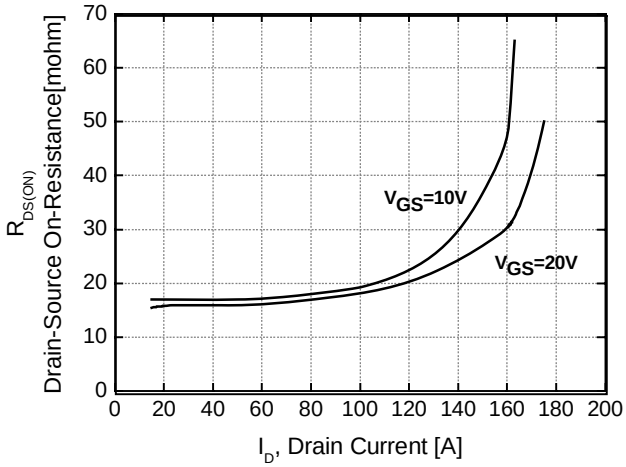


Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage

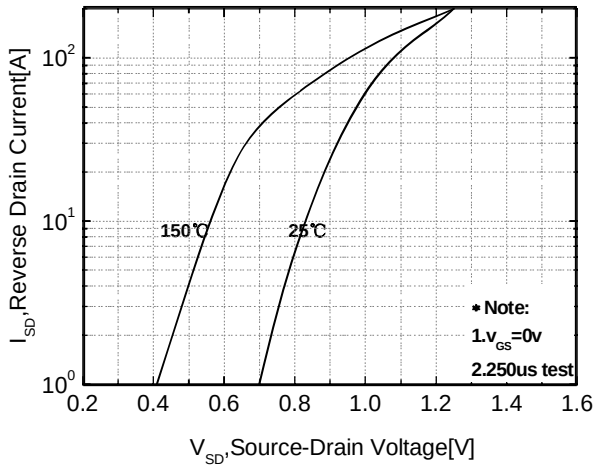


Fig 4. On State Current vs. Allowable Case Temperature

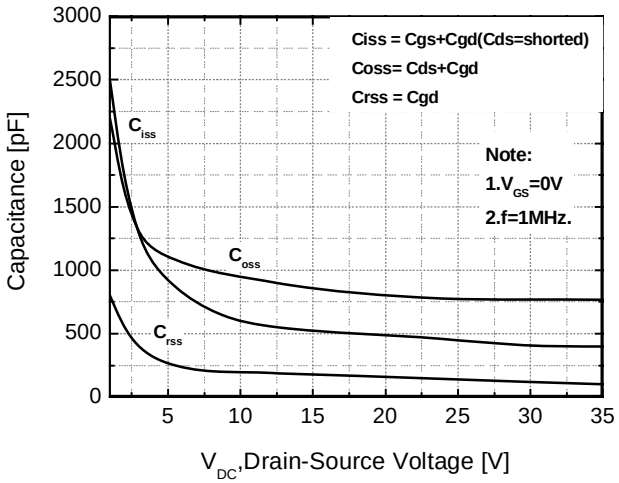


Fig 5. Capacitance Characteristics (Non-Repetitive)

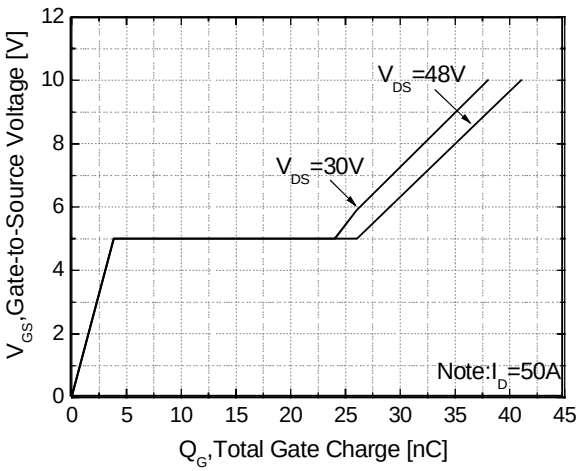


Fig 6. Gate Charge Characteristics

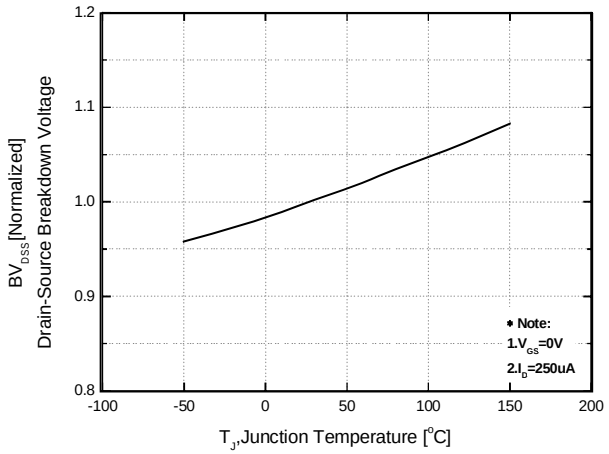


Fig 7. Breakdown Voltage Variation vs. Junction Temperature

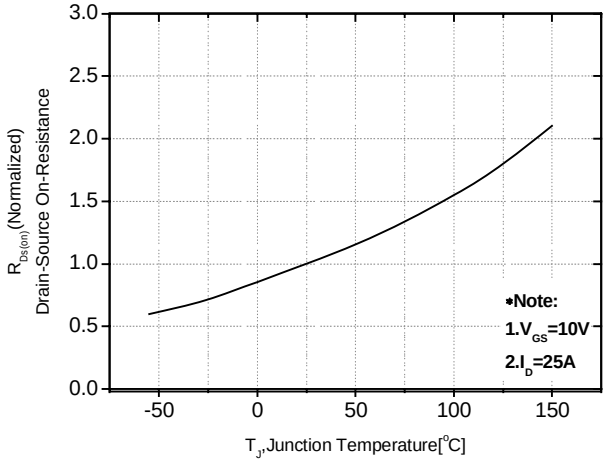


Fig 8. On-Resistance Variation vs. Junction Temperature

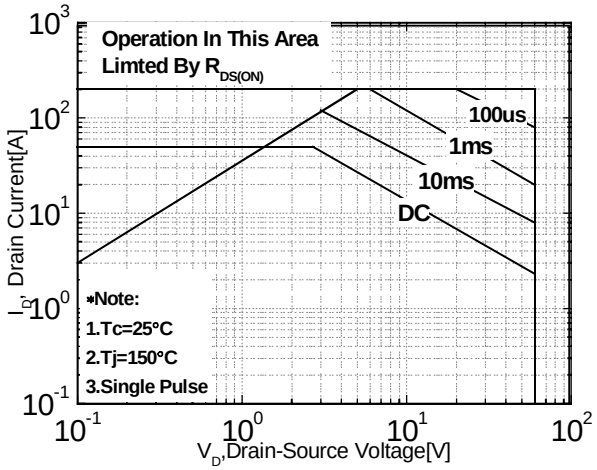


Fig9. Maximum Safe Operating

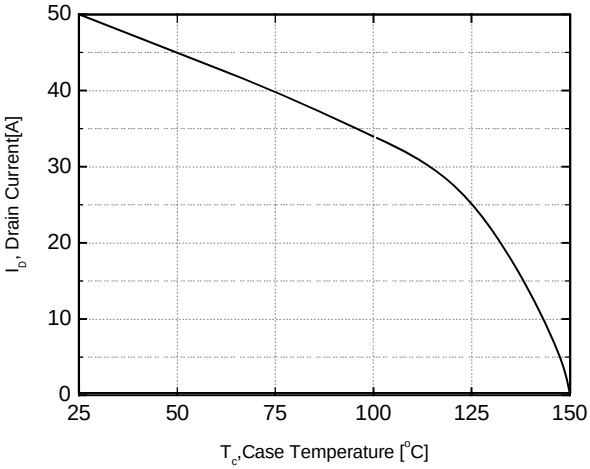


Fig 10. Maximum Drain Current Vs. Case Temperature

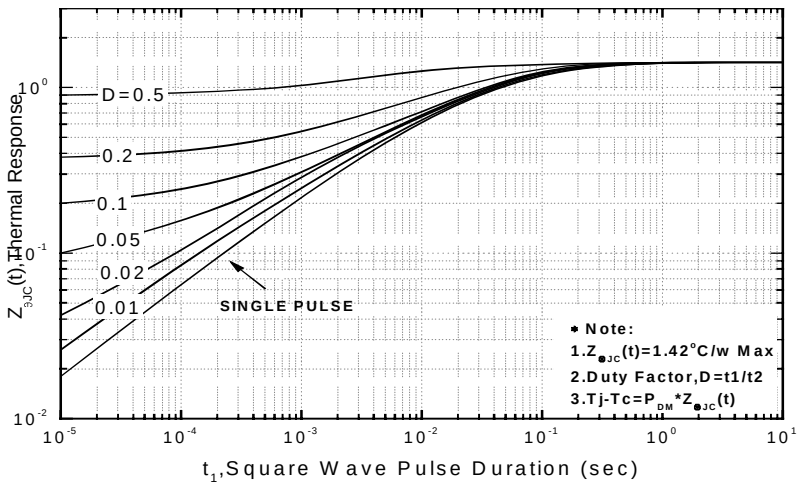


Fig 11. Transient Thermal Response Curve

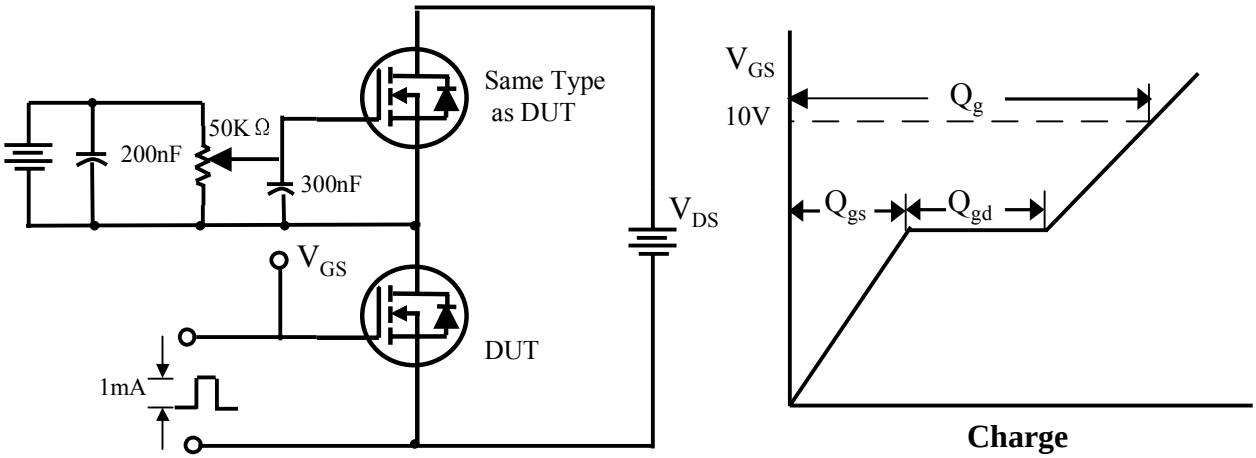


Fig 12. Gate Charge test Circuit & Waveforms

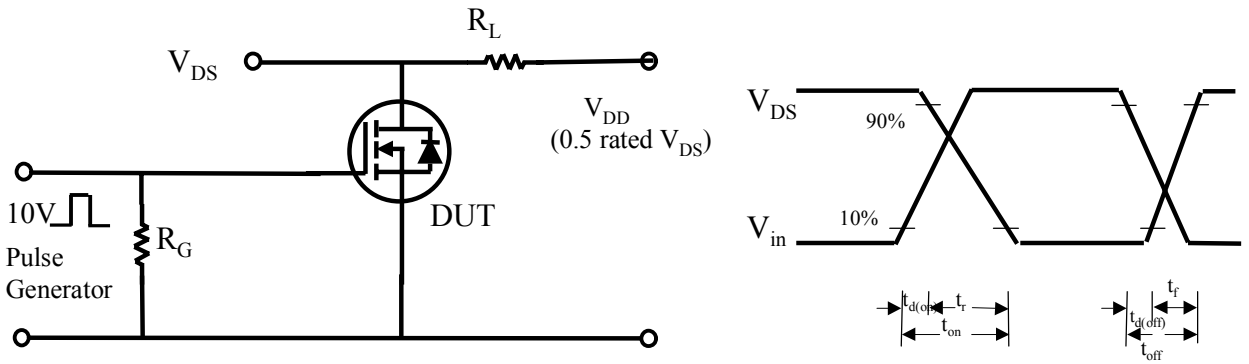


Fig 13. Switching test Circuit & Waveforms

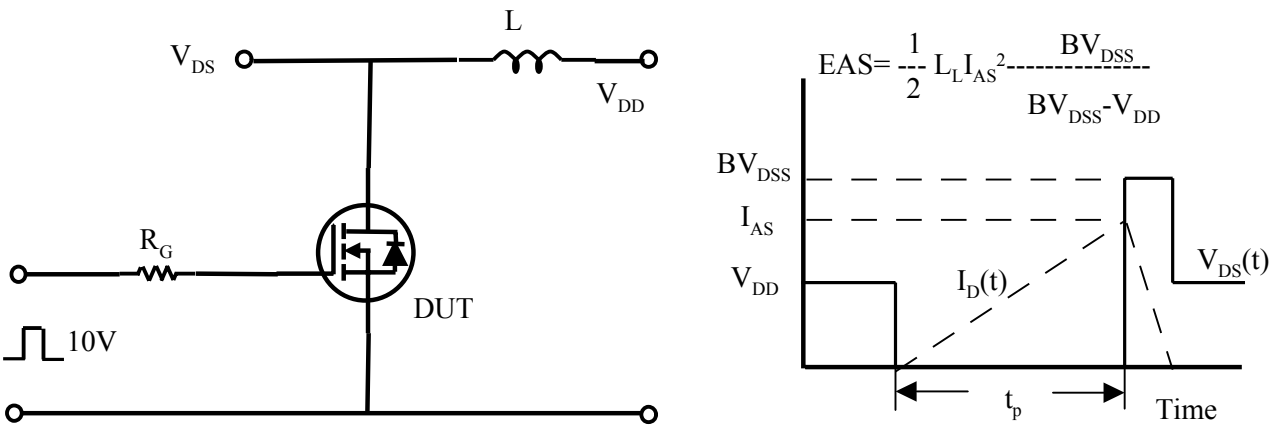


Fig 14. Unclamped Inductive Switching test Circuit & Waveforms

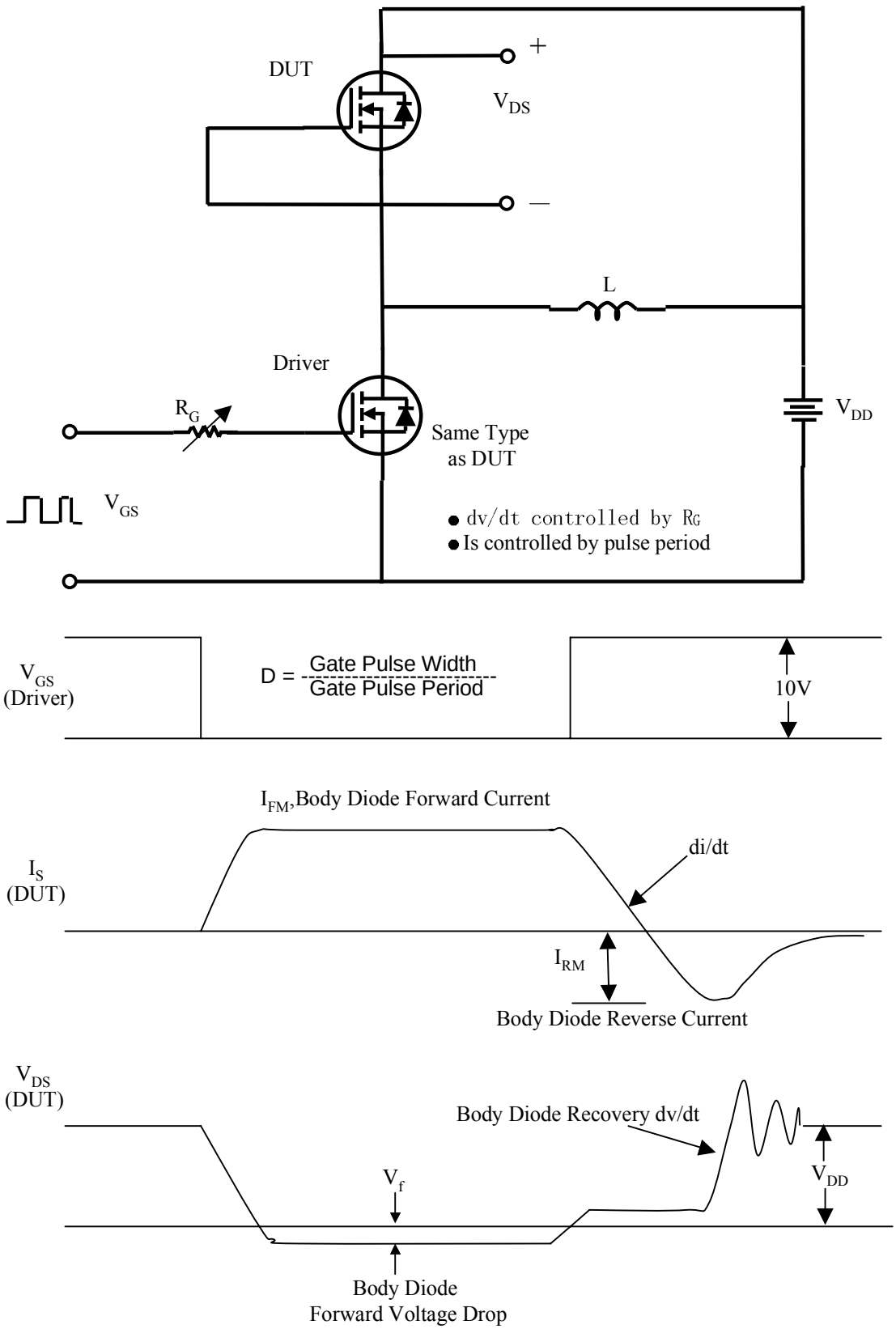


Fig 15. Peak Diode Recovery dv/dt test Circuit & Waveforms