4 Megabit Flash + 1 Megabit SRAM ComboMemory

SST31LH041

Advance Information

FEATURES:

- **Organized as 512K x 8 Flash + 128K x 8 SRAM**
- **Single 3.0-3.6V Read and Write Operations**
- **Concurrent Operation**
  - Read from or write to SRAM while erase/ program Flash
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 10 mA (typical) for Flash or SRAM Read
  - Standby Current: 10 µA (typical)
- **Sector Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Times:**
  - Flash: 70 ns
  - SRAM: 25 ns
- **Latched Address and Data for Flash**
- **Flash Fast Sector Erase and Byte Program:**
  - Sector Erase Time: 18 ms typical
  - Bank Erase Time: 70 ms typical
  - Byte Program Time: 14 µs typical
  - Bank Rewrite Time: 8 seconds typical
- **Flash Automatic Erase and Program Timing**
  - Internal V_{PP} Generation
- **Flash End of Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
  - 32-Pin TSOP (8mm x 14mm)
  - 40-Pin TSOP (10mm x 14mm)

PRODUCT DESCRIPTION

The SST31LH041 is a 512K x 8 CMOS flash memory bank combined with a 128K x 8 CMOS SRAM memory bank manufactured with SST's proprietary, high performance SuperFlash technology. The SST31LH041 device writes (SRAM or programs or erases flash) with a 3.0-3.6V power supply. The monolithic SST31LH041 device conforms to JEDEC standard pinouts and Software Data Protect (SDP) commands for x8 EEPROMs in TSOP packages.

Featuring high performance byte program, the flash memory bank provides a maximum byte program time of 20 µsec. The entire flash memory bank can be erased and programmed byte-by-byte in typically 8 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST31LH041 device has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST31LH041 device is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST31LH041 operates as two independent memory banks with respective bank enable signals. The SRAM and Flash memory banks are superimposed in the same memory address space. Both memory banks share common address lines, data lines, WE# and OE#. The memory bank selection is done by memory bank enable signals. The SRAM bank enable signal, BES# selects the SRAM bank and the flash memory bank enable signal, BEF# selects the flash memory bank. The WE# signal has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The SDP command sequence protects the data stored in the flash memory bank from accidental alteration.

The SST31LH041 provides the added functionality of being able to simultaneously read from or write to the SRAM bank while erasing or programming in the flash memory bank. The SRAM memory bank can be read or written while the flash memory bank performs Sector Erase, Bank Erase, or Byte Program concurrently. All flash memory Erase and Program operations will automatically latch the input address and data signals and complete the operation in background without further input stimulus requirement. Once the internally controlled erase or program cycle in the flash bank has commenced, the SRAM bank can be accessed for read or write.

The SST31LH041 device is suited for applications that use both nonvolatile flash memory and volatile SRAM memory to store code or data. For all system applications, the SST31LH041 device significantly improves performance and reliability, while lowering power consumption, when compared with multiple chip solutions. The SST31LH041 inherently uses less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any

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given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The monolithic ComboMemory eliminates redundant functions when using two separate memories of similar architecture; therefore, reducing the total power consumption.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

The SST31LH041 device also improves flexibility by using a single package and a common set of signals to perform functions previously requiring two separate devices. To meet high density, surface mount requirements, the SST31LH041 device is offered in 32-pin and 40-pin TSOP packages. See Figure 1 for the pinouts.

Device Operation

The ComboMemory uses BES# and BEF# to control operation of either the SRAM or the flash memory bank. Bus contention is eliminated as the monolithic device will not recognize both bank enables as being simultaneously active. If both bank enables are asserted (i.e., BEF# and BES# are both low), the BEF# will dominate while the BES# is ignored and the appropriate operation will be executed in the flash memory bank. SST does not recommend that both bank enables be simultaneously asserted. All other address, data, and control lines are shared; which minimizes power consumption and area. The device goes into standby when both bank enables are raised to V_{IHC}.

SRAM Operation

With BES# low and BEF# high, the SST31LH041 operates as a 128K x8 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. The SRAM is mapped into the first 128 KByte address space of the device. Read and Write cycle times are equal.

SRAM Read

The SRAM Read operation of the SST31LH041 is controlled by OE# and BES#, both have to be low with WE# high, for the system to obtain data from the outputs. BES# is used for SRAM bank selection. When BES# and BEF# are high, both memory banks are deselected. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 2, for further details.

SRAM Write

The SRAM Write operation of the SST31LH041 is controlled by WE# and BES#, both have to be low for the system to write to the SRAM. BES# is used for SRAM bank selection. During the Byte Write operation, the addresses and data are referenced to the rising edge of either BES# or WE#, whichever occurs first. The write time is measured from the last falling edge to the first rising edge of BES# and WE#. Refer to the Write cycle timing diagram, Figure 3, for further details.

Flash Operation

With BEF# active, the SST31LH041 operates as a 512K x 8 flash memory. The flash memory bank is read using the common address lines, data lines, WE# and OE#. Erase and Program operations are initiated with the JEDEC standard SDP command sequences. Address and data are latched during the SDP commands and internally timed Erase and Program operations.

Flash Read

The Read operation of the SST31LH041 device is controlled by BEF# and OE#, both have to be low, with WE# high, for the system to obtain data from the outputs. BEF# is used for flash memory bank selection. When BEF# and BES# are high, both banks are deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram (Figure 4) for further details.

Flash Erase/Program Operation

SDP commands are used to initiate the flash memory bank Program and Erase operations of the SST31LH041. SDP commands are loaded to the flash memory bank using standard microprocessor write sequences. A command is loaded by asserting WE# low while keeping BEF# low and OE# high. The address is latched on the falling edge of WE# or BEF#, whichever occurs last. The data is latched on the rising edge of WE# or BEF#, whichever occurs first.

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Flash Byte Program Operation

The flash memory bank of the SST31LH041 device is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 5 and 6 for WE# and BEF# controlled Program operation timing diagrams and Figure 15 for flowcharts. During the Program operation, the only valid Flash Read operations are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any SDP commands loaded during the internal Program operation will be ignored.

Flash Sector Erase Operation

The Sector Erase operation allows the system to erase the flash memory bank on a sector by sector basis. The sector architecture is based on uniform sector size of 4 KBytes. The Sector Erase operation is initiated by executing a six-byte-command load sequence for software data protection with sector erase command (30H) and sector address (SA) in the last bus cycle. The address lines A12-A18 will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The end of Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 9 for timing waveforms. Any SDP commands loaded during the Sector Erase operation will be ignored.

Flash Bank Erase Operation

The SST31LH041 flash memory bank provides a Bank Erase operation, which allows the user to erase the entire flash memory bank array to the “1’s” state. This is useful when the entire bank must be quickly erased. The Bank Erase operation is initiated by executing a six-byte software data protection command sequence with Bank Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or BEF# pulse, whichever occurs first. During the internal Erase operation, the only valid Flash Read operations are Toggle Bit and Data# Polling. See Table 4 for the command sequence, Figure 10 for timing diagram, and Figure 18 for the flowchart. Any SDP commands loaded during the Bank Erase operation will be ignored.

Flash Write Operation Status Detection

The SST31LH041 flash memory bank provides two software means to detect the completion of a flash memory bank Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The end of write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Flash Data# Polling (DQ7)

When the SST31LH041 flash memory bank is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. The flash memory bank is then ready for the next operation. During internal Erase operation, any attempt to read DQ7 will produce a ‘0’. Once the internal Erase operation is completed, DQ7 will produce a ‘1’. The Data# Polling is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operation. For Sector or Bank Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 16 for a flowchart.

Flash Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating 0’s and 1’s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The flash memory bank is then ready for the next operation. The Toggle Bit is valid after the rising edge of the fourth WE# (or BE#) pulse for Program operation. For Sector or Bank Erase, the Toggle Bit is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 16 for a flowchart.

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Flash Memory Data Protection

The SST31LH041 flash memory bank provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Flash Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Flash Write operation. This prevents inadvertent writes during power-up or power-down.

Flash Software Data Protection (SDP)

The SST31LH041 provides the JEDEC approved software data protection scheme for all flash memory bank data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST31LH041 device is shipped with the software data protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid SDP commands will abort the device to the read mode, within TRC.

Concurrent Read and Write Operations

The SST31LH041 provides the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the Flash. The device will ignore all SDP commands when an Erase or Program operation is in progress. This allows data alteration code to be executed from SRAM, while altering the data in Flash. The following table lists all valid states.

CONCURRENT READ/WRITE STATE TABLE

Flash	SRAM
Program/Erase	Read
Program/Erase	Write

Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

Product Identification

The product identification mode identifies the device as the SST31LH041 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware device ID read operation is typically used by a programmer to identify the correct algorithm for the SST31LH041 flash memory bank. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 17 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Address	Data
Manufacturer's Code	0000H	BF H
Device Code	0001H	17 H

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Product Identification Mode Exit/Reset

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software-reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 17 for a flowchart.

Design Considerations

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS}, e.g., less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 5 cm of the V_{DD} pin.

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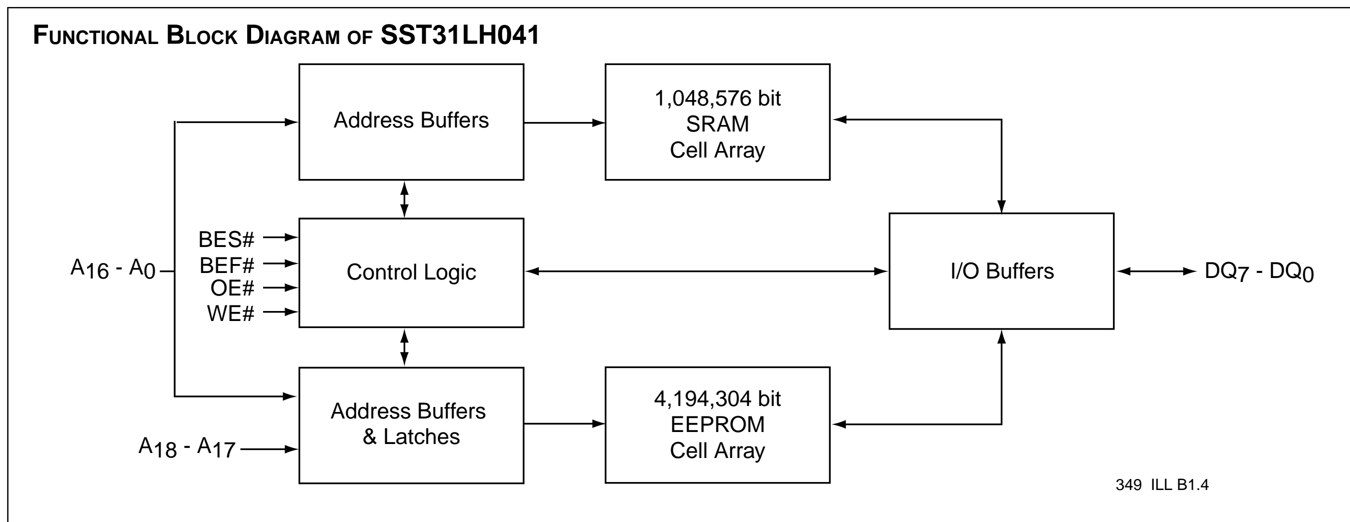
Advance Information



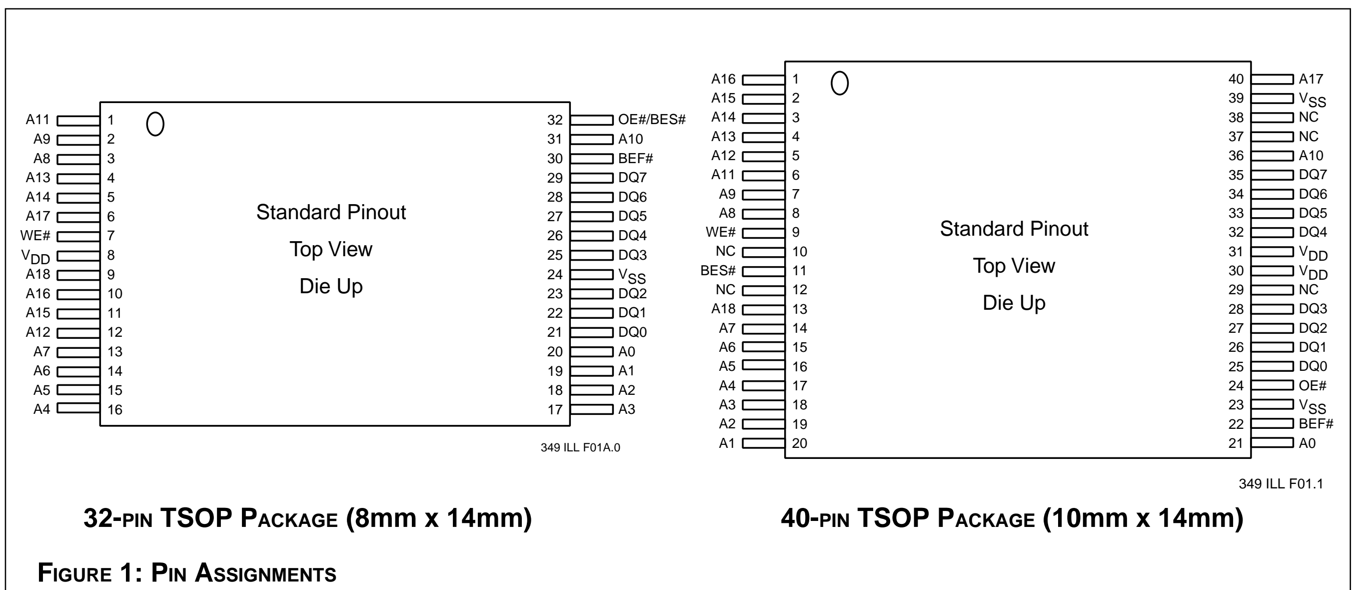


FIGURE 1: PIN ASSIGNMENTS

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{18}-A_0	Address Inputs	To provide memory addresses. During Flash Sector Erase A_{18}-A_{12} address lines will select the sector. A_{18}-A_0 to provide flash address, A_{16}-A_0 to provide SRAM addresses.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a Flash Erase/Program cycle. The outputs are in tri-state when OE# or BES# and BEF# are high.
BES#	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES# is low.
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low.
OE#	Output Enable	To gate the data output buffers. (Shared with BES# for 32-pin TSOP)
WE#	Write Enable	To control the write operations.
V_{DD}	Power Supply	To provide 3.0-3.6V supply
Vss	Ground	

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TABLE 3: OPERATION MODES SELECTION

Mode	BES#	BEF#	OE#	WE#	A9	DQ	Address
Flash Read	X	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Flash Program	X	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Flash Erase	X	V_{IL}	V_{IH}	V_{IL}	X	X	Sector address, XXh for Bank Erase
SRAM Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
SRAM Write	V_{IL}	V_{IH}	X	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Standby	V_{IHC}	V_{IHC}	X	X	X	High Z	X
Flash Write Inhibit	X X X	X X V_{IH}	V_{IL} X X	X V_{IH} X	X X X	High Z/D_{OUT} High Z/D_{OUT} High Z/D_{OUT}	X X X
Product Identification Hardware Mode	X	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer Code (BF) Device Code (17)	A_{18} - A_1 = V_{IL}, A_0 = V_{IL} A_{18} - A_1 = V_{IL}, A_0 = V_{IH}
Software Mode	X	V_{IL}	V_{IL}	V_{IH}	A_{IN}	ID Code	See Table 4

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TABLE 4: SOFTWARE COMMAND SEQUENCE FOR FLASH MEMORY BANK

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA(3)	Data				
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_x(2)	30H
Bank Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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Notes:

(1) Address format A_{14}-A_0 (Hex), Addresses A_{15}, A_{16}, A_{17} and A_{18} are a "Don't Care" for the Command sequence.
(2) SA_x for Sector Erase; uses A_{18}-A_{12} address lines
(3) BA = Program Byte address

Notes for Software ID Entry Command Sequence

1. With A_{18} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0, 31LH041 Device Code = 17H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias .... -55°C to +125°C
Storage Temperature .... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential .... -0.5V to V_{DD}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential .... -1.0V to V_{DD}+ 1.0V
Voltage on A_9 Pin to Ground Potential .... -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) .... 240°C
Output Short Circuit Current(1) .... 50 mA

Note: (1) Outputs shorted for no more than one second. No more than one output shorted at a time.

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OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0 °C to +70 °C	3.0-3.6V
Industrial	-40 °C to +85 °C	3.0-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time .... 5 ns
Output Load .... C_L = 30 pF
See Figures 13 and 14

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 3.0-3.6V

Symbol	Parameter	Limits Min	Limits Max	Units	Test Conditions
I_{DD}	Power Supply Current				$V_{DD} = V_{DD}$ Max, all DQs open, Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min.
	Read				OE# = V_{IL}, WE# = V_{IH}
	Flash		12	mA	BEF# = V_{IL}, BES# = V_{IH}
	SRAM		20	mA	BEF# = V_{IH}, BES# = V_{IL}
	Concurrent Operation		35	mA	BEF# = V_{IH}, BES# = V_{IL}
	Write				OE# = V_{IH}, WE# = V_{IL}
	Flash		15	mA	BEF# = V_{IL}, BES# = V_{IH}
	SRAM		20	mA	BEF# = V_{IH}, BES# = V_{IL}
I_{SB}	Standby V_{DD} Current		30	µA	$V_{DD} = V_{DD}$ Max. BEF# = BES# = V_{IHC}
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, $V_{DD} = V_{DD}$ Max.
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, $V_{DD} = V_{DD}$ Max.
V_{IL}	Input Low Voltage		0.8	V	$V_{DD} = V_{DD}$ Min.
V_{IH}	Input High Voltage	0.7V_{DD}		V	$V_{DD} = V_{DD}$ Max.
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	$V_{DD} = V_{DD}$ Max.
V_{OL}	Output Low Voltage		0.2	V	I_{OL} = 100 µA, $V_{DD} = V_{DD}$ Min.
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH} = -100µA, $V_{DD} = V_{DD}$ Min.
V_H	Supervoltage for A_9 pin	11.4	12.6	V	BEF# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9 pin		200	µA	BEF# = OE# = V_{IL}, WE# = V_{IH}, $A_9 = V_H$ Max.

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$(1)	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$(1)	Power-up to Write Operation	100	µs

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TABLE 7: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$(1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

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Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}(1)	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}(1)	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: SRAM MEMORY BANK READ CYCLE TIMING PARAMETERS V_{DD} = 3.0-3.6V

Symbol	Parameter	Min	Max	Unit
T_{RC}	Read Cycle Time	25		ns
T_{AA}	Address Access Time		25	ns
T_{BE}	Bank Enable Access Time		25	ns
T_{OE}	Output Enable Access Time		12	ns
T_{BLZ}(1)	BES# to Active Output	0		ns
T_{OLZ}(1)	Output Enable to Active Output	0		ns
T_{BHZ}(1)	BES# to High-Z Output		10	ns
T_{OHZ}(1)	Output Disable to High-Z Output		10	ns
T_{OH}	Output Hold from Address Change	0		ns

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Note: (1) This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

TABLE 10: SRAM MEMORY BANK WRITE CYCLE TIMING PARAMETERS V_{DD} = 3.0-3.6V

Symbol	Parameter	Min	Max	Unit
T_{WC}	Write Cycle Time	25		ns
T_{BW}	Bank Enable to End of Write	12		ns
T_{AW}	Address Valid to End of Write	12		ns
T_{AS}	Address Set-up Time	0		ns
T_{WP}	Write Pulse Width	12		ns
T_{WR}	Write recovery Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{DS}	Data Set-up Time	12		ns
T_{DH}	Data Hold from Write Time	0		ns

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AC CHARACTERISTICS

TABLE 11: FLASH READ CYCLE TIMING PARAMETERS V_{DD} = 3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle time	70		ns
T_{BE}	Bank Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		35	ns
T_{BLZ}(1)	BEF# Low to Active Output	0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		ns
T_{BHZ}(1)	BEF# High to High-Z Output		15	ns
T_{OHZ}(1)	OE# High to High-Z Output		15	ns
T_{OH}(1)	Output Hold from Address Change	0		ns

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Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

TABLE 12: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS V_{DD} = 3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{BP}	Byte Program time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{BS}	WE# and BEF# Setup Time	0		ns
T_{BH}	WE# and BEF# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{BP}	BEF# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}	WE# Pulse Width High	30		ns
T_{BPH}	BEF# Pulse Width High	30		ns
T_{DS}	Data Setup Time	40		ns
T_{DH}	Data Hold Time	0		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{SE}	Sector Erase		25	ms
T_{SBE}	Bank Erase		100	ms

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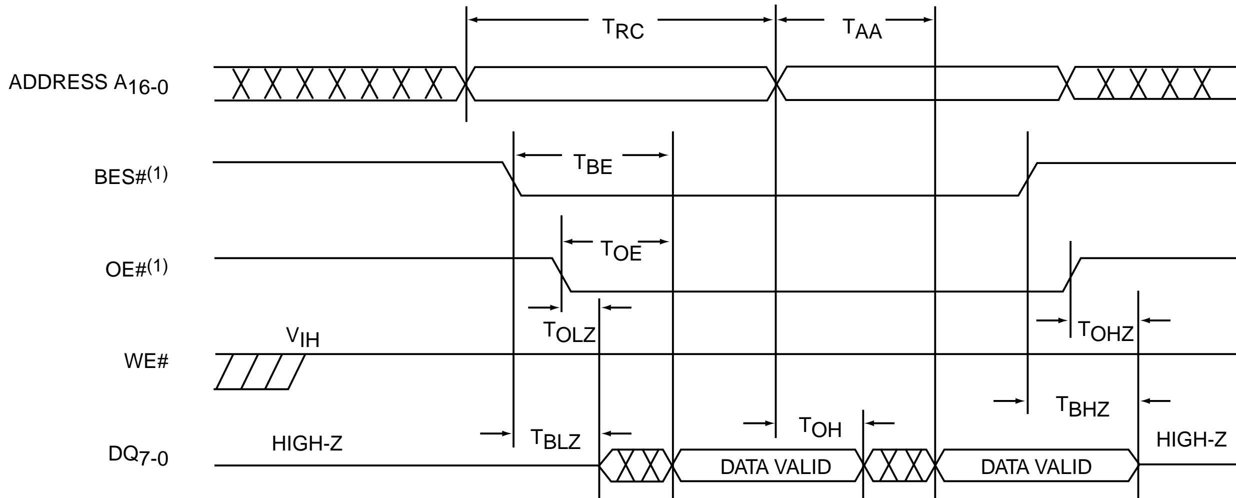
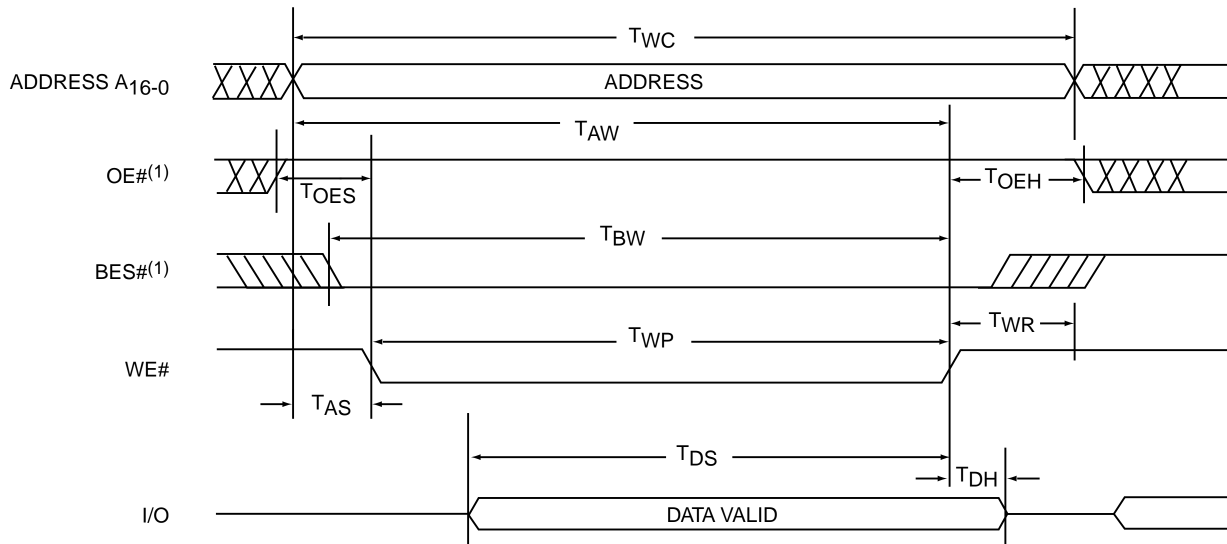


Note 1: For 32-pin TSOP, BES# and OE# are the same signal.

FIGURE 2: SRAM READ CYCLE TIMING DIAGRAM



Note 1: For 32-pin TSOP, BES# and OE# are the same signal.

FIGURE 3: SRAM WRITE CYCLE TIMING DIAGRAM

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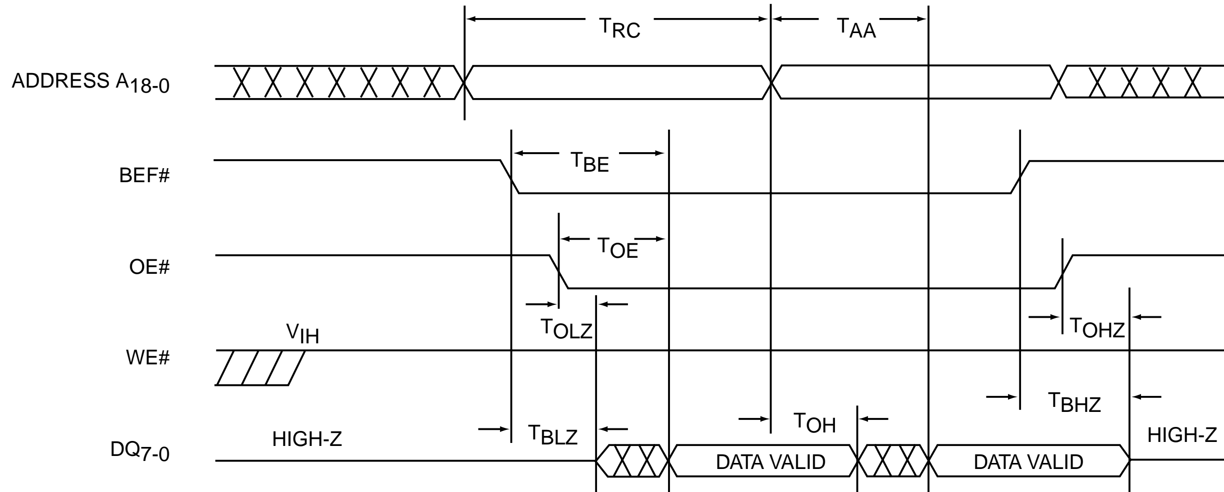

Figure 4: Flash Read Cycle Timing Diagram

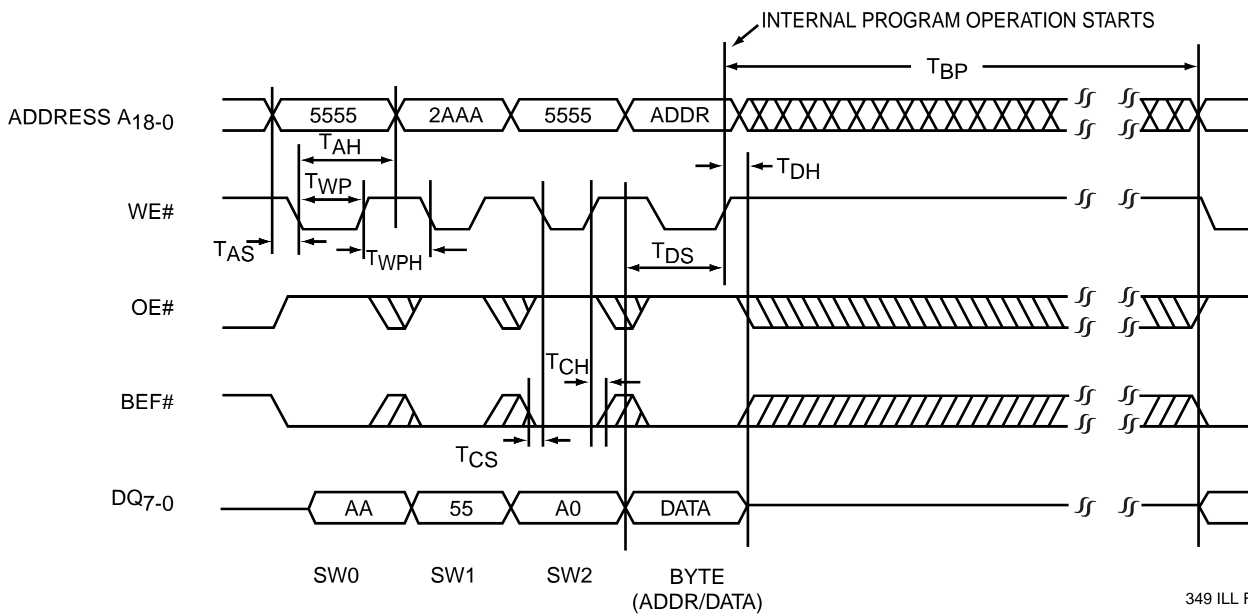

Figure 5: WE# Controlled Program Cycle Timing Diagram

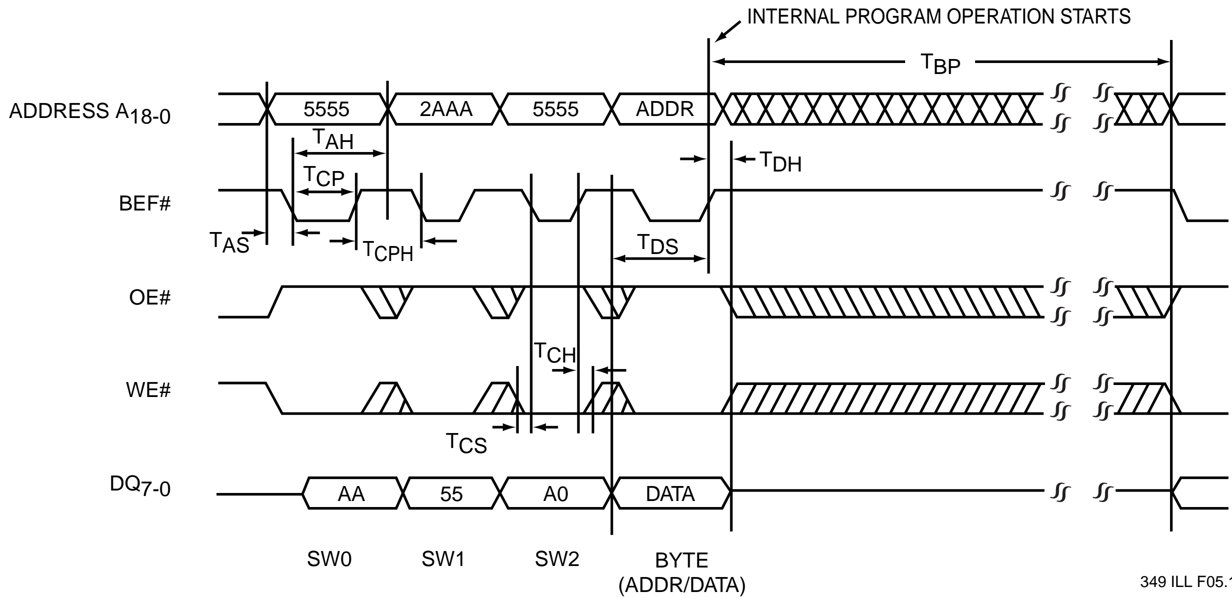

Figure 6: BEF# Controlled Program Cycle Timing Diagram

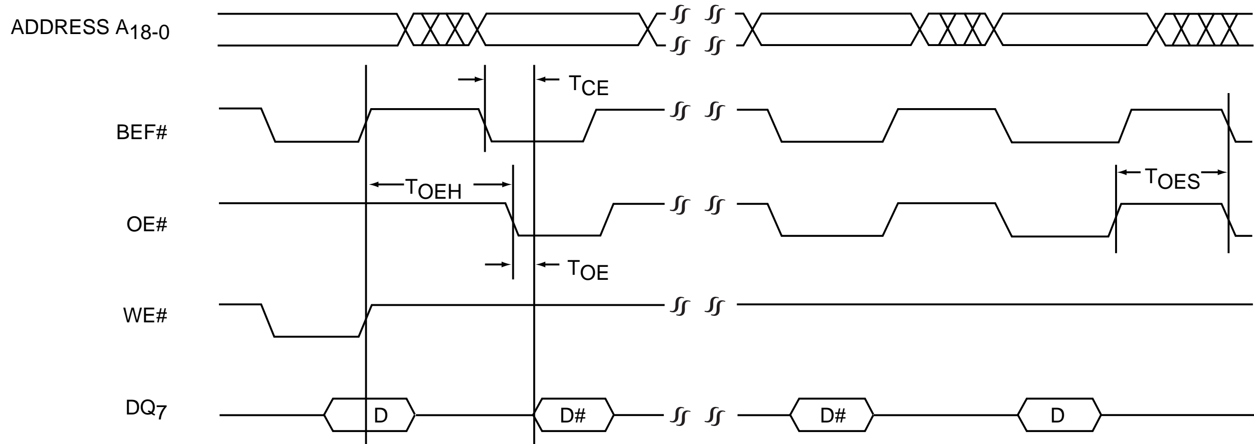

Figure 7: Data# Polling Timing Diagram

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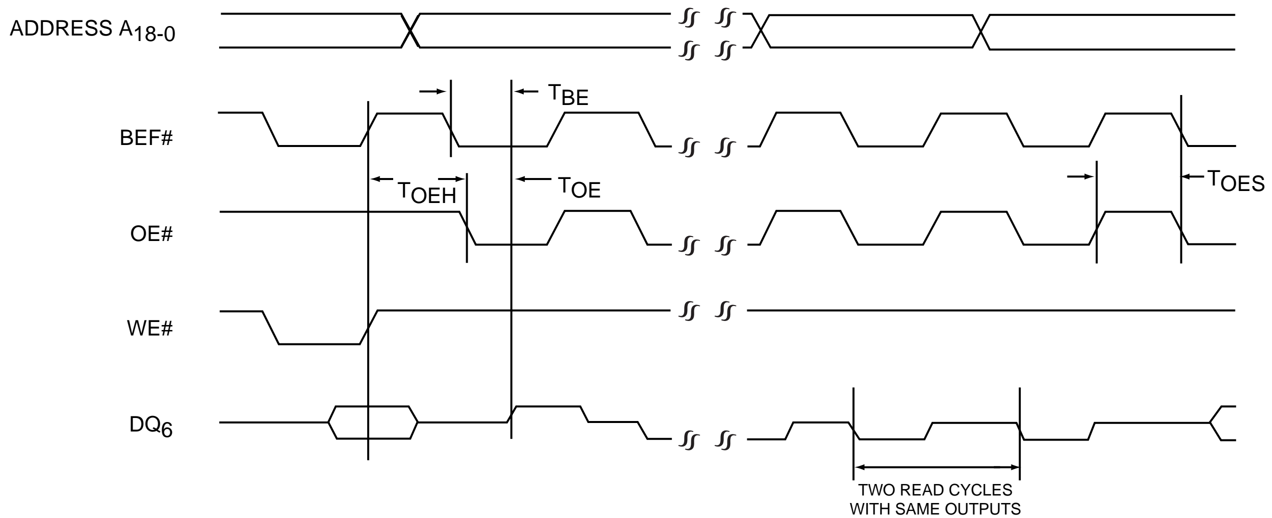
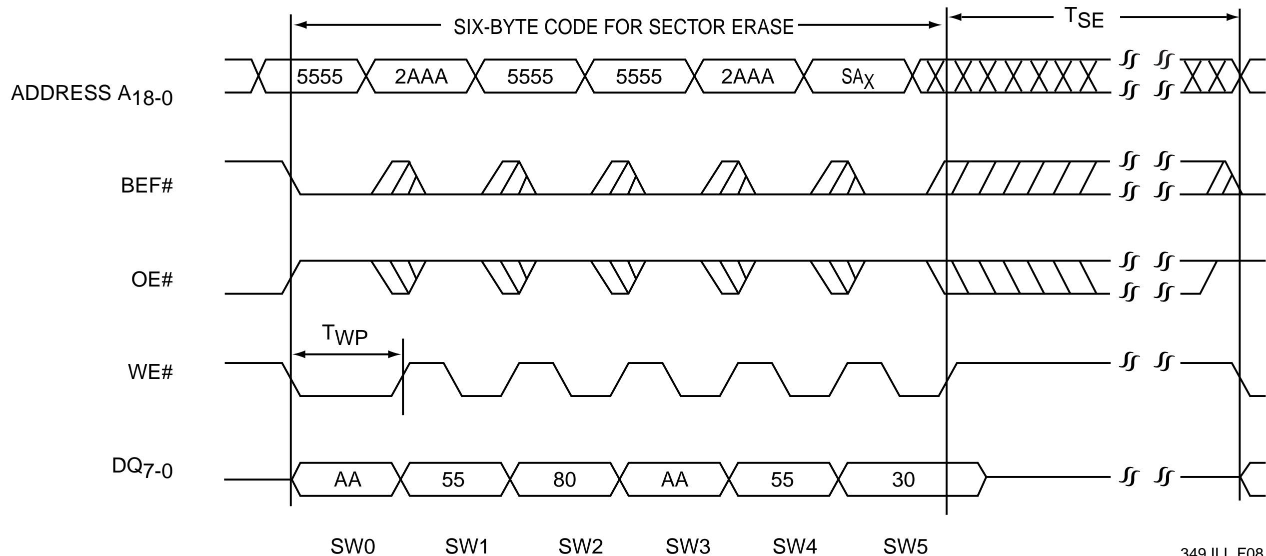


FIGURE 8: TOGGLE BIT TIMING DIAGRAM



Note: The device also supports BE# controlled Sector Erase operation. The WE# and BE# signals are interchangeable as long as minimum timings are met. (See table 10)
SA_X = Sector Address

FIGURE 9: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM

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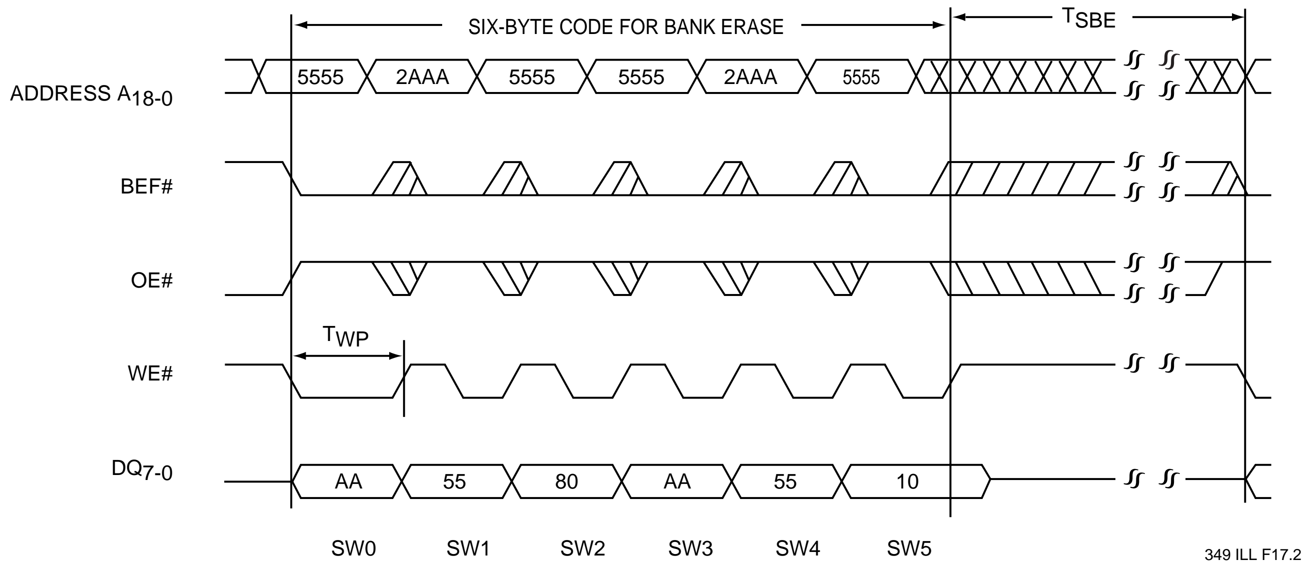

Note: The device also supports BE# controlled Bank Erase operation. The WE# and BE# signals are interchangeable as long as minimum timings are met. (See table 10)

FIGURE 10: WE# CONTROLLED BANK ERASE TIMING DIAGRAM

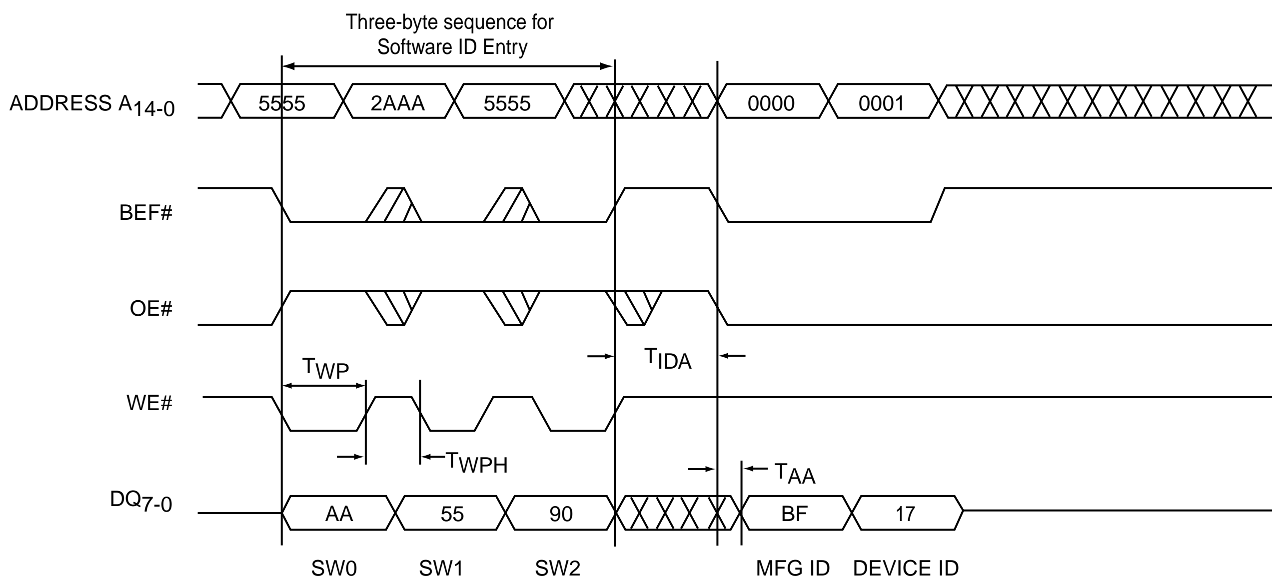

FIGURE 11: SOFTWARE ID ENTRY AND READ

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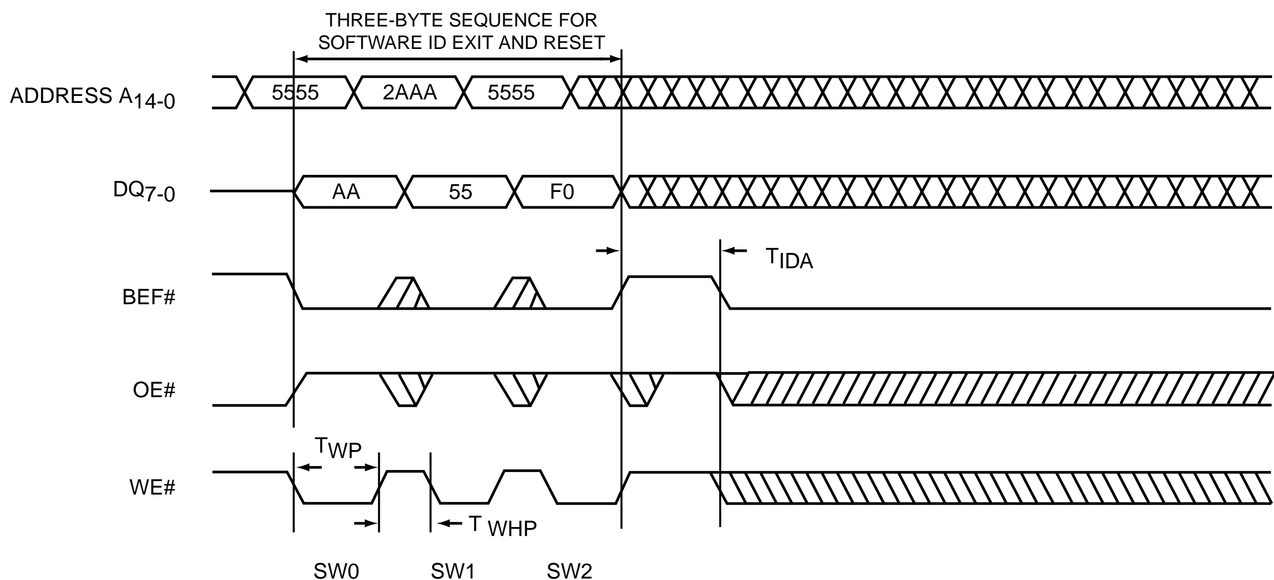
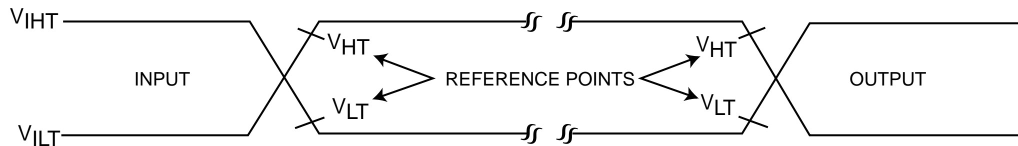


FIGURE 12: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic “1” and V_{ILT} (0.1 V_{DD}) for a logic “0”.
Measurement reference points for inputs and outputs are at V_{HT} (0.7 V_{DD}) and V_{LT} (0.8 V)
Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{HT}–V_{HIGH} Test
V_{LT}–V_{LOW} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 13: AC INPUT/OUTPUT REFERENCE WAVEFORMS

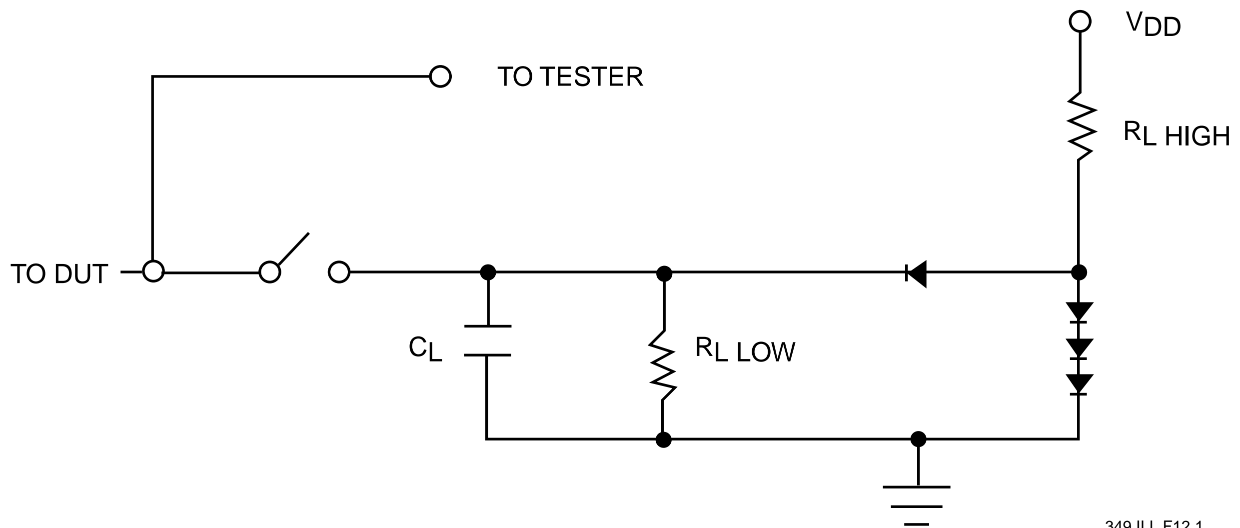


FIGURE 14: A TEST LOAD EXAMPLE

FIGURE 15: BYTE PROGRAM ALGORITHM

Internal Timer

Byte Program/Erase Initiated

Wait T_{BP}, T_{SBE}, or T_{SE}

Program/Erase Completed

Toggle Bit

Byte Program/Erase Initiated

Read byte

Read same byte

Does DQ_6 match?

No

Yes

Program/Erase Completed

Data# Polling

Byte Program/Erase Initiated

Read DQ_7

Is DQ_7 = true data?

No

Yes

Program/Erase Completed

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FIGURE 16: WAIT OPTIONS

Software Product ID Entry Command Sequence

Write data: AA, Address: 5555 → Write data: 55, Address: 2AAA → Write data: 90, Address: 5555 → Wait T_{IDA} → Read Software ID

Software Product ID Exit & Reset Command Sequence

Write data: AA, Address: 5555 → Write data: 55, Address: 2AAA → Write data: F0, Address: 5555 → Wait T_{IDA} → Return to normal operation

Write data: F0, Address: XX → Wait T_{IDA} → Return to normal operation

349 ILL F15.0

FIGURE 17: SOFTWARE PRODUCT COMMAND FLOWCHARTS

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Chip Erase Command Sequence

Write data: AA
Address: 5555

Write data: 55
Address: 2AAA

Write data: 80
Address: 5555

Write data: AA
Address: 5555

Write data: 55
Address: 2AAA

Write data: 10
Address: 5555

Wait T_{SCE}

Chip erased to FFH

Sector Erase Command Sequence

Write data: AA
Address: 5555

Write data: 55
Address: 2AAA

Write data: 80
Address: 5555

Write data: AA
Address: 5555

Write data: 55
Address: 2AAA

Write data: 30
Address: SA_X

Wait T_{SE}

Sector erased to FFH

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FIGURE 18: ERASE COMMAND SEQUENCE

Concurrent Operation

Load SDP Command Sequence

Flash Program/Erase Initiated

Wait for End of Write Indication

Read or Write SRAM

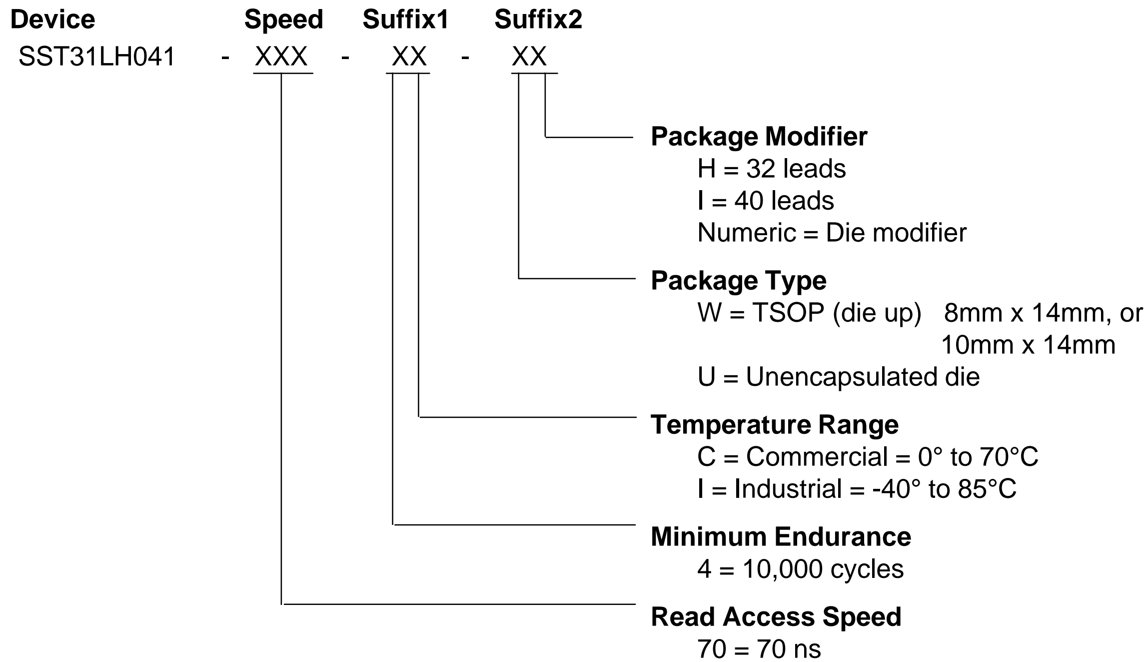
End Wait

Flash Operation Completed

End Concurrent Operation

349 ILL F19.0

FIGURE 19: CONCURRENT OPERATION FLOWCHART



SST31LH041 Valid combinations

SST31LH041-70-4C-WI
SST31LH041-70-4C-U1
SST31LH041-70-4C-WH

SST31LH041-70-4I-WI
SST31LH041-70-4I-WH

Example : Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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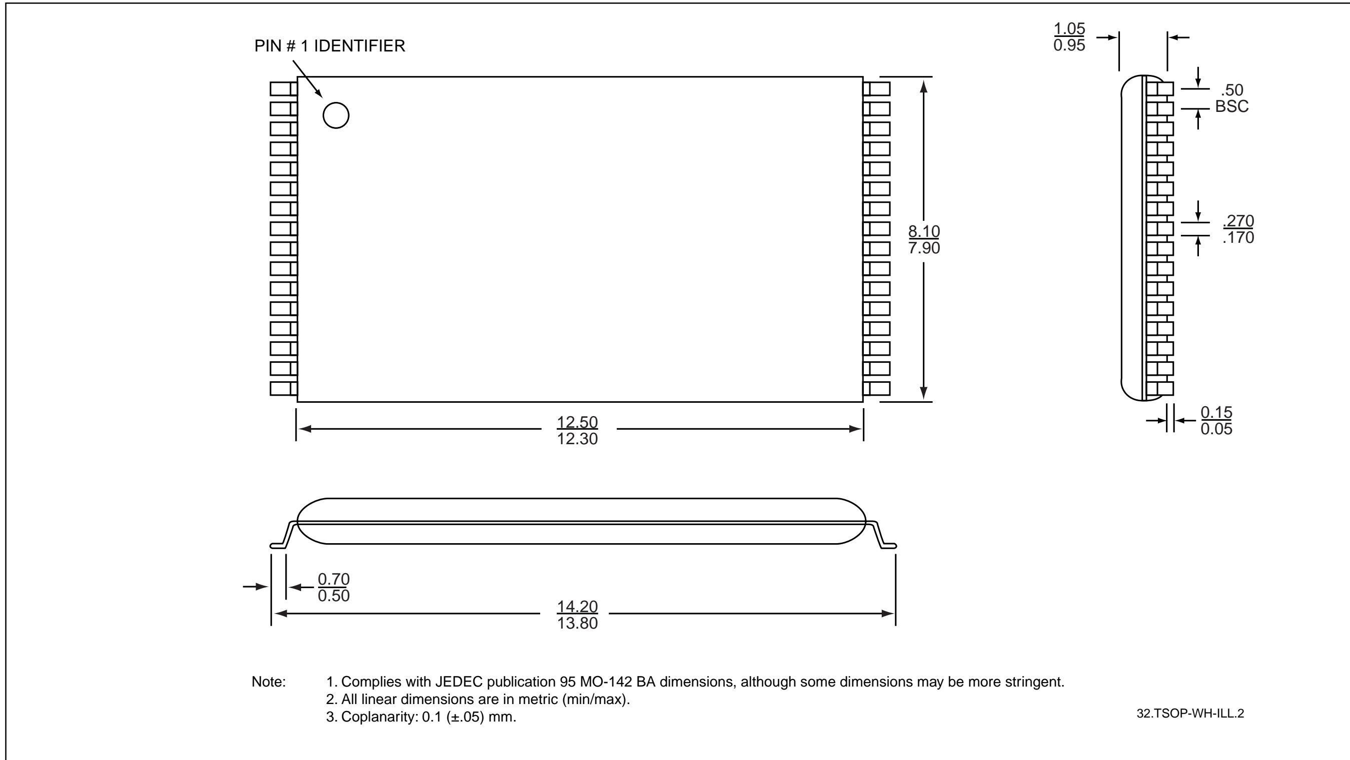
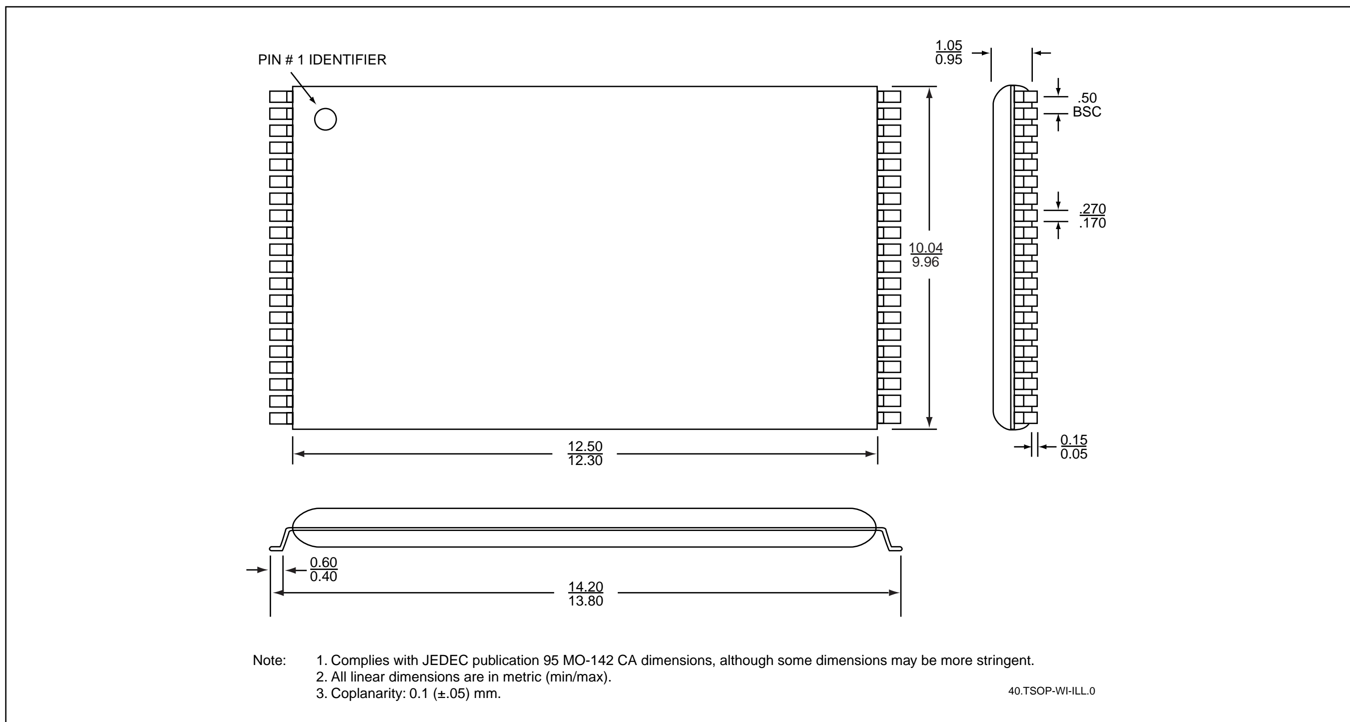
PACKAGING DIAGRAMS



32-Pin Thin Small Outline Package (TSOP) 8mm x 14mm
SST Package Code: WH



40-Pin Thin Small Outline Package (TSOP) 10mm x 14mm
SST Package Code: WI

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