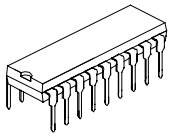
Silan
Semiconductors

# SC9270C/D

## DTMF RECEIVER

### DESCRIPTION

The SC9270C/D is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high- and low-group filters and dial-tone rejection. Digital counting techniques are employed in the decoder to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on-chip provision of a differential input amplifier, clock-oscillator and latched 3-state bus interface.



DIP-18

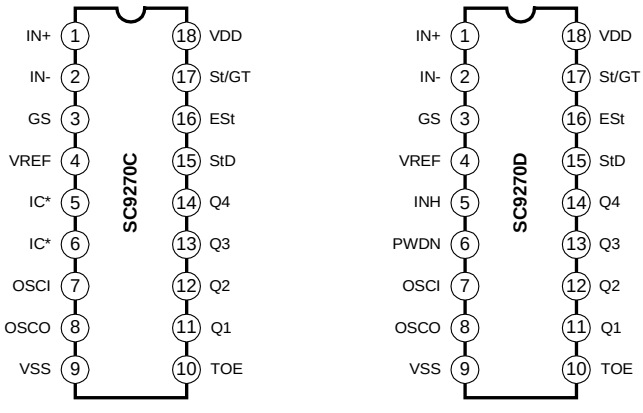
### FEATURES

*Complete receiver in an 18-pin package
*Excellent performance
*CMOS, single 5 volt operation,
*Widely operating voltage: 1.2V ~ 5.25V
*Minimum board area
*Central office quality
*Low power consumption
*Power-Down mode (SC9270D only)
*Inhibit-mode (SC9270D only)

### APPLICATIONS

*Paging systems
*Repeater systems / Mobile radio
*Credit card systems
*Remote control
*Personal computers

### PIN CONFIGURATIONS




* Connect to VSS

## BLOCK DIAGRAM

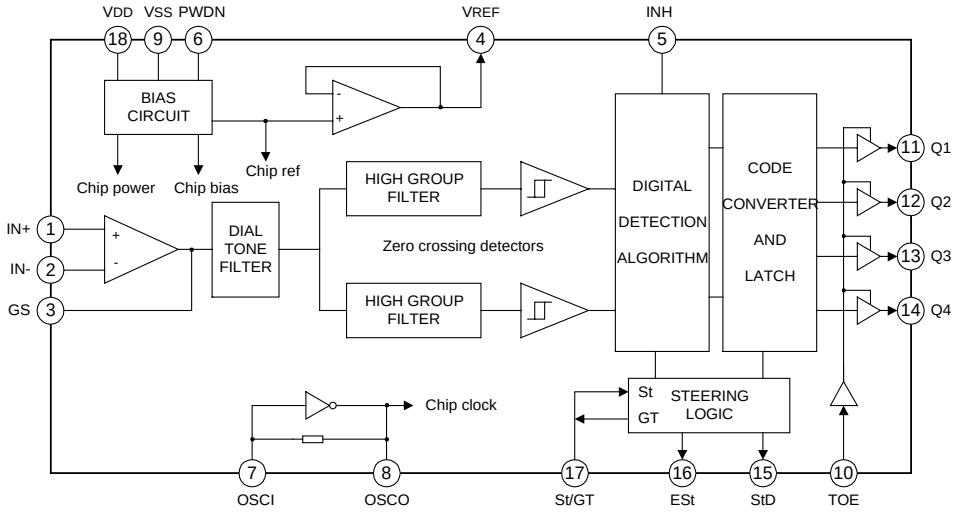



Figure 1. block diagram

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{DD}$-$V_{SS}$ | 6 | V |
| Voltage on any pin | -- | $V_{SS}$-0.3 ~ $V_{DD}$+0.3 | V |
| Current at any pin | -- | 10 | mA |
| Operating temperature | Topr | -40~+85 | °C |
| Storage Temperature | Tstg | -65~+150 | °C |
| Package power dissipation | | 500 | mW |

Note: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.

2. Unless otherwise specified, all voltages are referenced to ground.

3. Power dissipation temperature derating: -12 mV / from 65°C to 85°C

## RECOMMENDED OPERATING CONDITIONS (Note 1)

| Parameter | Symbol | Conditions | Min | Typ(Note 2) | Max | Unit |
|---|---|---|---|---|---|---|
| Positive Supply Voltages | $V_{DD}$ | $V_{SS}$=0V | 1.2 | 5 | -- | V |
| Oscillator Clock Frequency | fc | -- | -- | 3.579545 | -- | MHz |
| Oscillator Frequency Tolerance | $\Delta$fc | -- | -- | ±0.1 | -- | % |

Note: 1. Voltages are with respect to ground(Vss), unless otherwise stated.

2 .Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

## DC ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***SUPPLY*** | | | | | | |
| Operating Supply Voltage | $V_{DD}$ | -- | 1.2 | -- | 5.25 | V |
| Operating Supply Current | $I_{CC}$ | -- | -- | 3.0 | 7.0 | mA |
| Power Consumption | $P_O$ | f=3.579MHz; $V_{DD}$=5V | -- | 15 | 35 | mW |
| Standby Current | $I_S$ | PWDN pin = $V_{DD}$ | -- | -- | 100 | μA |
| ***INPUTS*** | | | | | | |
| Low Level Input Voltage | $V_{IL}$ | -- | -- | -- | 1.5 | V |
| High Level Input Voltage | $V_{IH}$ | -- | 3.5 | -- | -- | V |
| Input Leakage Current | $I_{IH}/I_{IL}$ | $V_{IN}$= $V_{SS}$ or $V_{DD}$ | -- | 0.1 | -- | μA |
| Pull up(Source) Current | $I_{SO}$ | TOE(Pin 10)=0V | -- | 7.5 | 15 | μA |
| Input Impedance (IN+, IN-) | $R_{IN}$ | @1kHz | -- | 10 | -- | MΩ |
| Steering Threshold Voltage | $V_{TSt}$ | -- | -- | 2.35 | -- | V |
| ***OUTPUTS*** | | | | | | |
| Low Level Output Voltage | $V_{OL}$ | No load | -- | 0.03 | -- | V |
| High Level Output Voltage | $V_{OH}$ | No load | -- | 4.97 | -- | μA |
| Output Low(Sink) Current | $I_{OL}$ | $V_{OUT}$=0.4V | 1.0 | 2.5 | -- | mA |
| Output High(Source) Current | $I_{OH}$ | $V_{OUT}$=4.6V | 0.4 | 0.8 | -- | mA |
| $V_{REF}$ Output Voltage | $V_{REF}$ | No load | 2.4 | -- | 2.7 | V |
| $V_{REF}$ Output Resistance | $R_{OR}$ | -- | -- | 10 | -- | kΩ |

## OPERATING CHARACTERISTICS

### Gain Setting Amplifier

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IN}$ | $V_{SS}$ < $V_{IN}$ < $V_{DD}$ | -- | ±100 | -- | nA |
| Input Resistance | $R_{IN}$ | -- | -- | 10 | -- | MΩ |
| Input Offset Voltage | $V_{OS}$ | -- | -- | ±25 | -- | mV |
| Power Supply Rejection | PSRR | 1kHz | -- | 60 | -- | dB |
| Common Mode Rejection | CMRR | -3.0V < $V_{IN}$ < 3.0V | -- | 60 | -- | dB |
| DC Open Loop Voltage Gain | $A_{VOL}$ | -- | -- | 65 | -- | dB |
| Open Loop Unity Gain Bandwidth | $f_C$ | -- | -- | 1.5 | -- | MHz |
| Output Voltage Swing | $V_O$ | $R_L$≥100kΩ to $V_{SS}$ | -- | 4.5 | -- | $V_{PP}$ |
| Tolerable capacitive load(GS) | $C_L$ | -- | -- | 100 | -- | PF |
| Tolerable resistive load(GS) | $R_L$ | -- | -- | 50 | -- | kΩ |
| Common Mode Range | $V_{CM}$ | No load | -- | 3.0 | -- | $V_{PP}$ |

Notes : 1. All voltages referenced to $V_{DD}$ unless otherwise noted.

2. $V_{DD}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = 25°C .

**AC CHARACTERISTICS** (All voltage referenced to Vss otherwise noted; $V_{DD}$=5.0V, $V_{SS}$=0V, $T_A$=25°C, $f_{CLK}$=3.579545 MHz, using test circuit of figure 2 & 3. Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ***SIGNAL CONDITIONS*** | | | | | | |
| Valid Input Signal Levels (each tone of composite signal) | -- | Note:1,2,3,5,6,9,11 | -- | -- | -40 | dBm |
| | -- | Note:1,2,3,5,6,9,11 | -- | -- | 7.75 | $mV_{RMS}$ |
| | -- | Note:1,2,3,5,6,9,11 | +1 | -- | -- | dBm |
| | -- | Note:1,2,3,5,6,9,11 | 883 | -- | -- | $mV_{RMS}$ |
| Positive Twist Accept | -- | Note:2,3,6,9,11 | -- | 10 | -- | dB |
| Negative Twist Accept | -- | Note:2,3,6,9,11 | -- | 10 | -- | dB |
| Frequency Deviation Accept Limit | -- | Note:2,3,5,9,11 | -- | ±1.5%±2Hz | -- | |
| Frequency Deviation Reject Limit | -- | Note:2,3,5,11 | ±3.5 | -- | -- | |
| Thrid Tone Tolerance | -- | Note:2,3,4,5,9,13 | -18.5 | | -- | dB |
| Noise Tolerance | -- | Note:2,3,4,5,7,9,10 | -- | -12 | | dB |
| Dial Tone Tolerance | -- | Note:2,3,4,5,8,9,11 | -- | +18 | -- | dB |
| ***TIMING*** | | | | | | |
| Tone Present Detection Time | $t_{DP}$ | Refer to Fig. 4. Note:12 | 5 | 14 | 16 | ms |
| Tone Absent Detection Time | $t_{DA}$ | Refer to Fig. 4. Note:12 | 0.5 | 4 | 8.5 | ms |
| Tone Duration Accept | $t_{REC}$ | User adjustable | -- | -- | 40 | ms |
| Tone Duration Reject | $t_{REC}$ | User adjustable | 20 | -- | -- | ms |
| Interdigit Pause Accept | $t_{ID}$ | User adjustable | -- | -- | 40 | ms |
| Interdigit Pause Reject | $t_{DO}$ | User adjustable | 20 | -- | -- | ms |
| ***OUTPUTS*** | | | | | | |
| Propagation Delay (St to Q) | $t_{PQ}$ | TOE=$V_{DD}$ | -- | 8 | 11 | μs |
| Propagation Delay (St to StD) | $t_{PSED}$ | TOE=$V_{DD}$ | -- | 12 | -- | μs |
| Output Data Set Up (Q to Std) | $t_{QSED}$ | TOE=$V_{DD}$ | -- | 4.5 | -- | μs |
| Propagation Delay (TOE to Q Enable) | $t_{PTE}$ | $R_L$=10kΩ, $C_L$=50pf | -- | 50 | -- | ns |
| Propagation Delay (TOE to Q Disable) | $t_{PTD}$ | $R_L$=10kΩ, $C_L$=50pf | -- | 300 | -- | ns |
| ***CLOCK*** | | | | | | |
| Crystal/Clock Frequency | $f_C$ | -- | 3.5759 | 3.5759 | 3.581 | MHz |
| Clock Input Rise Time | $t_{LHCL}$ | Ext. clock | -- | -- | 110 | ns |
| Clock Input Fall Time | $t_{HLCL}$ | Ext. clock | -- | -- | 110 | ns |
| Clock Input Duty Time | $DC_{CL}$ | Ext. clock | 40 | 50 | 60 | % |
| Capacitive Load (OSCO) | $C_{LO}$ | -- | -- | -- | 30 | pf |

Notes: 1. dBm = decibels above or below a reference power of 1mW into a 600 Ohm load.

2. Digit sequences consists of all 16 DTMF tones.

3. Tone duration = 40mS Tone pause = 40mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2Hz.
7. Bandwidth limited (3kHz) Gaussian Noise.
8. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept.
12. For guard time calculation purpose.
13. Referenced to Fig.10 Input DTMF Tone level at –25dBm(-28dBm at GS Pin) interference Frequency Range between 480—3400Hz.

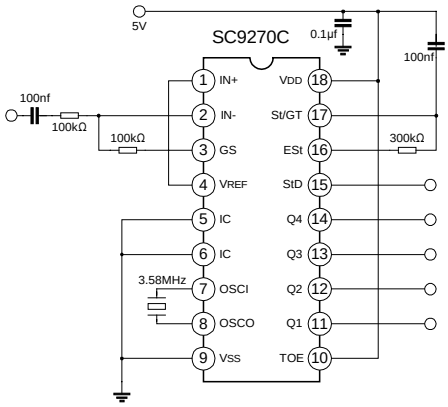



Figure 2. Single ended input cofiguration

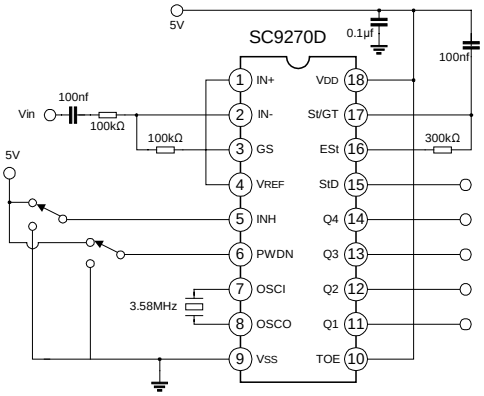



Figure 3. Single ended input cofiguration

## PIN DESCRIPTION

| Pin No. | Pin Name | I/O | Description | |
|---|---|---|---|---|
| 1 | IN+ | I | Non-Inverting input | Connections to the front-end differential amplifier. |
| 2 | IN- | I | Inverting input | |
| 3 | GS | -- | Gain select. Gives access to output of front-end differential amplifier for connection of feedback resistor. | |
| 4 | $V_{REF}$ | O | Reference voltage output, nominally $V_{DD}/2$. May be used to bias the inputs at mid-rail (see application diagram). | |
| 5 | INH | I | Inhibit (input) logic high inhibit the detection of 1633Hz internal built-in pull down resistor. (SC9270D only). (For SC9270C, this pin must be tied to $V_{SS}$ ) | |
| 6 | PWDN | I | Power down (input). Active high power down the device and inhibit the oscillator internal built-in pull down resistor. (SC9270D only). (For SC9270C, this pin must be tied to $V_{SS}$ ) | |
| 7 | OSC1 | I | Clock Input | 3.579545MHz crystal connected between these pins completes internal oscillator. |
| 8 | OSC2 | O | Clock Output | |
| 9 | $V_{SS}$ | -- | Negative power supply, normally connected to 0V. | |
| 10 | TOE | I | 3-state data output enable. Logic high enables the outputs Q1-Q4. This pin is Internally pulled up. | |
| 11~14 | Q1 ~ Q4 | O | 3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance. | |
| 15 | StD | O | Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below $V_{TSt}$. | |
| 16 | ESt | O | Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low. | |
| 17 | St/GT | I/O | Steering input/guard time output (bi-directional). A voltage greater than $V_{TSt}$ detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than $V_{TSt}$ frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St. | |
| 18 | $V_{DD}$ | -- | Positive power supply. | |

## TIMING DIAGRAM

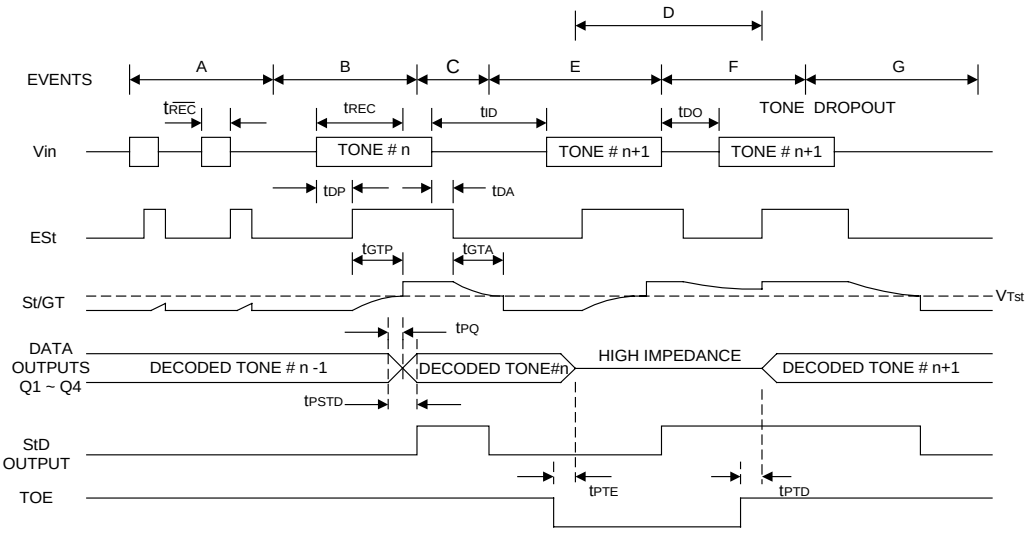



Figure 4. Timing diagram

| EXPLANATION OF EVENTS | EXPLANATIONN OF SYMBOLS |
|---|---|
| A. Short tone bursts: detected. Tone duration is invalid.<br>B. Tone #n is detected. Tone duration is valid. Decoded to outputs.<br>C. End of tone #n is detected and validated.<br>D. 3 State outputs disabled (high impedance).<br>E. Tone #n + 1 is detected. Tone duration is valid. Decoded to outputs.<br>F. Tristate outputs are enabled. Acceptable drop out of tone #n + 1 does not negister at outputs.<br>G. End of tone #n + 1 is detected and validated. | Vin: DTMF composite input signal.<br>$t_{\overline{REC}}$ :Maximum DTMF signal duration not detected as valid.<br>tREC: Minimum DTMF Signal duration required for valid recognition.<br>tID: Minimum time between valid DTMF signals.<br>tDO: Maximum allowable dropout during valid DTMF signal<br>tDP: Time to detect the presence of valid DTMF signals.<br>tDP: Time to detect the absence of valid DTMF signals.<br>tGTP: Guard Time, Tone present.<br>tGTP: Guard Time, Tone absent. |

## FUNCTION DESCRIPTIONS

The SC9270C/D monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tones of receiver pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

### 1. FILTER SECTION

Separation of the low-group and high-group tones is achieved by applying the dual tone signal to the inputs of two filters a sixth order for the high group and an eighth order for the low group. The bandwidths of which correspond to the bands enclosing the low-group and high-group tones (see table 1). The filter section also in corporates notches at 350Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a second-order switched-capacitor section which smooth the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

| Flow | Fhigh | KEY | TOE | Q4 | Q3 | Q2 | Q1 |
|---|---|---|---|---|---|---|---|
| 697 | 1209 | 1 | H | 0 | 0 | 0 | 1 |
| 697 | 1336 | 2 | H | 0 | 0 | 1 | 0 |
| 697 | 1477 | 3 | H | 0 | 0 | 1 | 1 |
| 770 | 1209 | 4 | H | 0 | 1 | 0 | 0 |
| 770 | 1336 | 5 | H | 0 | 1 | 0 | 1 |
| 770 | 1477 | 6 | H | 0 | 1 | 1 | 0 |
| 852 | 1209 | 7 | H | 0 | 1 | 1 | 1 |
| 852 | 1336 | 8 | H | 1 | 0 | 0 | 0 |
| 852 | 1477 | 9 | H | 1 | 0 | 0 | 1 |
| 941 | 1336 | 0 | H | 1 | 0 | 1 | 0 |
| 941 | 1209 | * | H | 1 | 0 | 1 | 1 |
| 941 | 1477 | # | H | 1 | 1 | 0 | 0 |
| 697 | 1633 | A | H | 1 | 1 | 0 | 1 |
| 770 | 1633 | B | H | 1 | 1 | 1 | 0 |
| 852 | 1633 | C | H | 1 | 1 | 1 | 1 |
| 941 | 1633 | D | H | 0 | 0 | 0 | 0 |
| -- | -- | ANY | L | Z | Z | Z | Z |
| L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE | | | | | | | |

Table 1: Function decode table

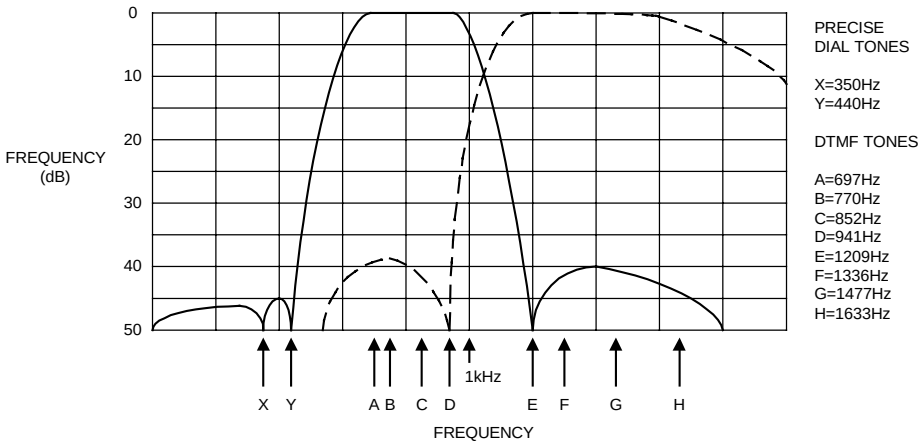



Figure 5. Filter Response

**2. DECODER SECTION**

The decoder used digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm(protects) against tone simulation by extraneous signals, such as voice, while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to “talk-off” and tolerance to the presence of interfering signals (“third tones”) and noise. When the detector recognizes the simultaneous presence of two valid tones (referred to as “signal condition” in some industry specifications), it raises the “early steering” flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

**3. STEERING CIRCUIT**

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as “character- recognition-condition”). This check is performed by an external RC time-constant driven by ESt. A logic high on ESt causes $V_C$ (see Fig.4) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period ($t_{GTP}$), Vc reaches the threshold ($V_{TSt}$) of the steering logic to register the tone-pair, latching its corresponding 4-bit code (see Fig.3) into the output latch. At this point, the GT output is activated and drives $V_C$ to $V_{DD}$. GT

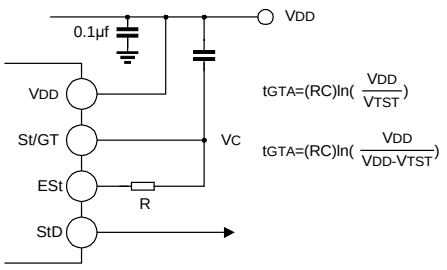



Figure 6. Basic steering Circuit

continues to drive high as long as ESt remains high. Finally after a short delay to allow the output latch to settle, the "delayed-steering" output flag, StD, goes high, signaling that a received tone-pair has been registered.The contents of the output latch are made available on the 4-bit output bus by raising the 3-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions ("drop-out") too short to be considered a valid pause. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

**4. GUARD TIME ADJUSTMENT**

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Fig.6 is applicable. Component values are chosen according to the following formulae:

$t_{REC} = t_{DP} + t_{GTP}$ $t_{ID} = t_{DA} + t_{GTA}$

The value of $t_{DP}$ is a parameter of the device (see table) and $t_{REC}$ is the minimum signal duration to be recognized by the receiver. A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a $t_{REC}$ of 40mS would be 300k. Different steering arrangements may be used to select independently the guard-times for tone-present ($t_{GTP}$ ) and tone-absent ($t_{GTA}$ ). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard-time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing $t_{REC}$ improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short $t_{REC}$ with a long $t_{DO}$ would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop - outs would be required. Design information for guard-time adjustment is shown in Fig.7.

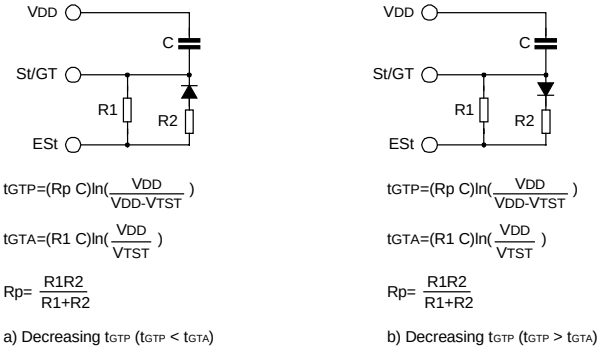


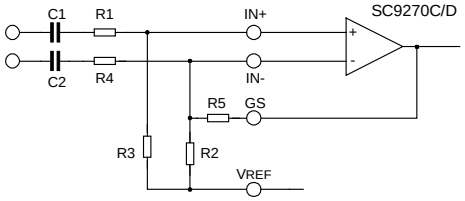

Figure 7. Guard time adjustment

**5. INPUT CONFIGURATION**

The input arrangement of the SC9270C/D provides a differential-input operational amplifier as well as a bias source ($V_{REF}$ ) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Fig.2 with the op-amp connected for unity gain and $V_{REF}$ biasing the input at 1/2$V_{DD}$.

Fig.8 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.




DIFFERENTIAL INPUT AMPLIFIER

C1=C2=10nF

R1=R4=R5=100k All resistors are +/- 1% tolerance

R2=60k, R3=37.5k All capacitors are +/- 5% tolerance

$R3=\frac{R2*R5}{R2+R5}$

VOLTAGE GAIN (Av diff)=$\frac{R5}{R1}$

INPUT IMPEDANCE(Zi diff)=$2\sqrt{R1^2+\left(\frac{1}{\omega C}\right)^2}$

Figure 8. Differential input configuration

**6. POWER – DOWN AND INHIBIT MODE**

A logic high applied to pin 6 (PWDN) will power the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of 1633 Hz. The output code will remain the same as the previous detected code (see table 2).

| fLOW | Fhigh | KEY | TOE | Q4 | Q3 | Q2 | Q1 |
|---|---|---|---|---|---|---|---|
| 697 | 1209 | 1 | H | L | L | L | H |
| 697 | 1336 | 2 | H | L | L | H | L |
| 697 | 1477 | 3 | H | L | L | H | H |
| 770 | 1209 | 4 | H | L | H | L | L |
| 770 | 1336 | 5 | H | L | H | L | H |
| 770 | 1477 | 6 | H | L | H | H | L |
| 852 | 1209 | 7 | H | L | H | H | H |
| 852 | 1336 | 8 | H | H | L | L | L |
| 852 | 1477 | 9 | H | H | L | L | H |
| 941 | 1336 | 0 | H | H | L | H | L |
| 941 | 1209 | * | H | H | L | H | H |
| 941 | 1477 | # | H | H | H | L | L |
| 697 | 1633 | A | H | H | H | L | H |
| 770 | 1633 | B | H | H | H | H | L |
| 852 | 1633 | C | H | H | H | H | H |
| 941 | 1633 | D | H | L | L | L | L |
| -- | -- | ANY | L | Z | Z | Z | Z |

| fLOW | Fhigh | KEY | TOE | Q4 | Q3 | Q2 | Q1 |
|---|---|---|---|---|---|---|---|
| 697 | 1209 | 1 | H | L | L | L | H |
| 697 | 1336 | 2 | H | L | L | H | L |
| 697 | 1477 | 3 | H | L | L | H | H |
| 770 | 1209 | 4 | H | L | H | L | L |
| 770 | 1336 | 5 | H | L | H | L | H |
| 770 | 1477 | 6 | H | L | H | H | L |
| 852 | 1209 | 7 | H | L | H | H | H |
| 852 | 1336 | 8 | H | H | L | L | L |
| 852 | 1477 | 9 | H | H | L | L | H |
| 941 | 1336 | 0 | H | H | L | H | L |
| 941 | 1209 | * | H | H | L | H | H |
| 941 | 1477 | # | H | H | H | L | L |
| 697 | 1633 | A | H | PREVIOUS DATA | | | |
| 770 | 1633 | B | H | | | | |
| 852 | 1633 | C | H | | | | |
| 941 | 1633 | D | H | | | | |
| -- | -- | ANY | L | Z | Z | Z | Z |

Table 2: Truth table

INH = $V_{SS}$ (Z: high impedance) INH = $V_{DD}$

**6. CRYSTAL OSCILLATOR**

The internal clock circuit is completed with the addition of an external 3.579545MHz crystal and is normally connected as shown in Figure 2. However, it is possible to configure several SC9270C/D devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30pF capacitor to the oscillator input (OSCI) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 9 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie: precision balancing capacitors are not required.

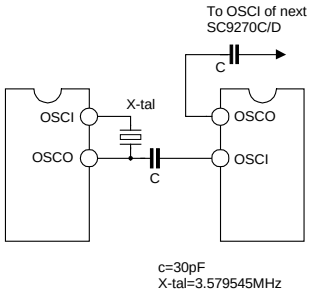
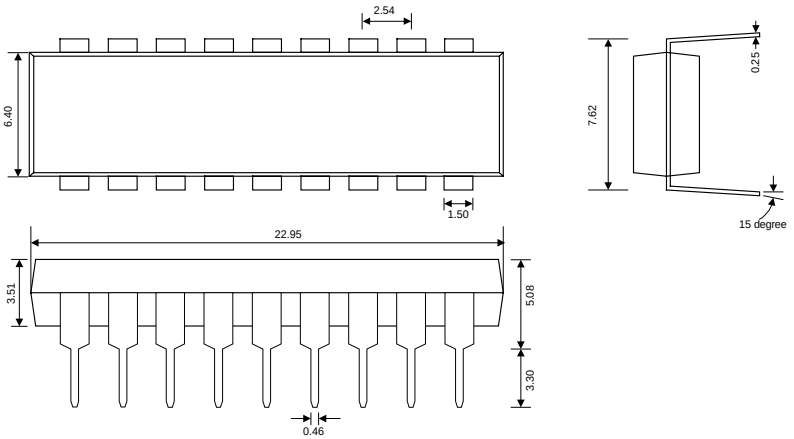



Figure 9 Oscillator Connection

**PACKAGE OUTLINE**

DIP-18-300-2.54 UNIT: mm



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