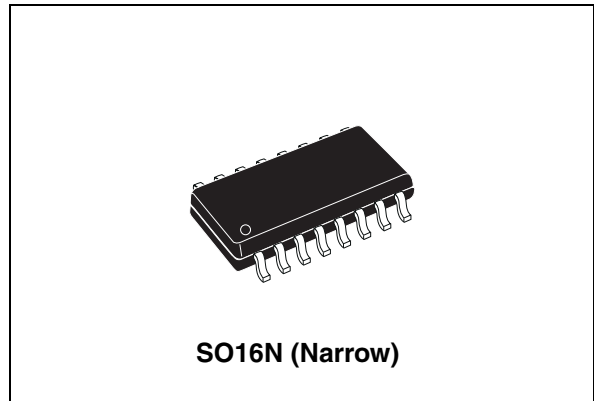# L6725

Low cost adjustable step-down controller

Features

- Input voltage range from 1.8V to 14V
- Supply voltage range from 4.5V to 14V
- Adjustable output voltage down to 0.6V with ±0.8% accuracy over line voltage and temperature (0°C~125°C)
- Fixed frequency voltage mode control
- 0% to 100% duty cycle
- External input voltage reference
- Soft-start and inhibit
- High current embedded drivers
- Predictive anti-cross conduction control
- Programmable high-side and low-side $R_{DS(on)}$ sense over-current-protection
- Sink current capability
- Selectable switching frequency 250KHz/500KHz
- Pre-bias start up capability
- Over voltage protection
- Thermal shut-down
- Package: SO16N

SO16N (Narrow)

Applications

- Low voltage distributed DC-DC
- Graphic cards

Order Codes

| Part number	Package	Packing
L6725	SO16N	Tube
L6725TR	SO16N	Tape & Reel

Contents

1 Summary description

The device is a low cost pwm controller dedicated for low voltage distributed DC-DC. The input voltage can range from 1.8V to 14V, while the supply voltage can range from 4.5V to 14V. The output voltage is adjustable down to 0.6V.

High peak current gate drivers provide for fast switching to the external power section, and the output current can be in excess of 20A. The device is capable to manage minimum on-times (T_{ON}) shorter than 100ns making possible conversions with very low duty cycle and very high switching frequency. In order to guarantee a real overcurrent protection, also with very narrow T_{ON}, the current sense is realized both on the high-side and low-side MOSFETs. When necessary, two different current limit protections can be externally set through an external resistor. The device can sink current after the soft-start phase while, during the soft-start, the sink mode capability is disabled in order to allow a proper start-up also in pre-biased output voltage conditions. Other features are over-voltage-protection and thermal shutdown.

1.1 Functional description

Figure 1. Block diagram
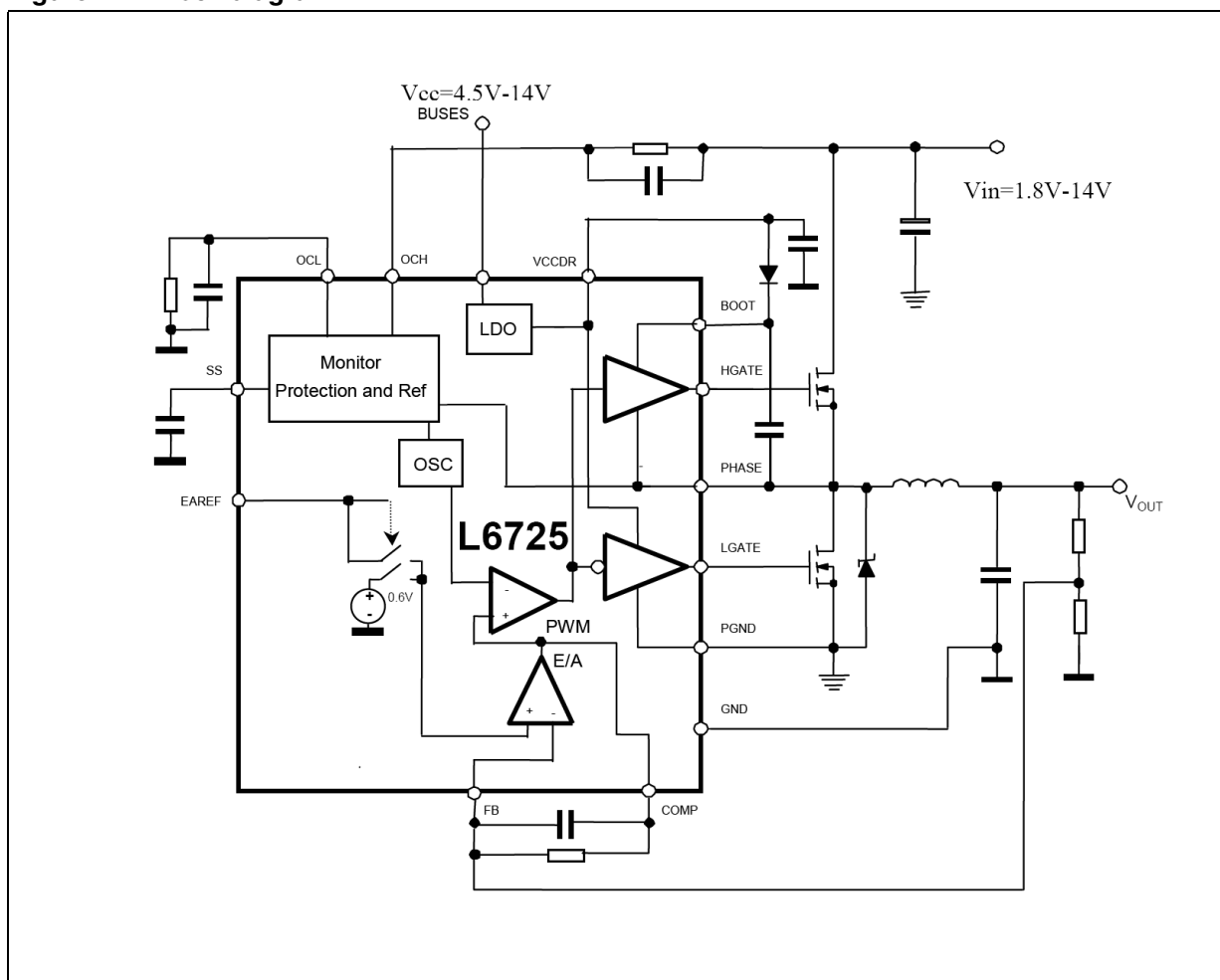
2 Electrical data

2.1 Maximum rating

Table 1.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND and PGND, OCH	-0.3 to 18	V
V_{BOOT} - V_{PHASE}	Boot Voltage	0 to 6	\
V_{HGATE} - V_{PHASE}		0 to V_{BOOT} - V_{PHASE}	V
V_{BOOT}	BOOT	-0.3 to 24	V
V_{PHASE}	PHASE	-1 to 18	V
	PHASE Spike, transient < 50ns (F_{SW} = 500KHz)	-3	
		+24	
	SS, FB, EAREF, OCL, LGATE, COMP, V_{CCDR}	-0.3 to 6	V
OCH Pin	Maximum Withstanding Voltage Range	±1500	V
OTHER PINS	Test Condition: CDF-AEC-Q100-002 "Human Body Model" Acceptance Criteria: "Normal Performance"	±2000	

2.2 Thermal data

Table 2.   Thermal data

Symbol	Description	Value	Unit
R_{thJA}[1]	Max. Thermal Resistance Junction to ambient	50	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Ambient operating temperature range	-40 to +85	°C

1. Package mounted on demoboard

3   Pin connections and functions
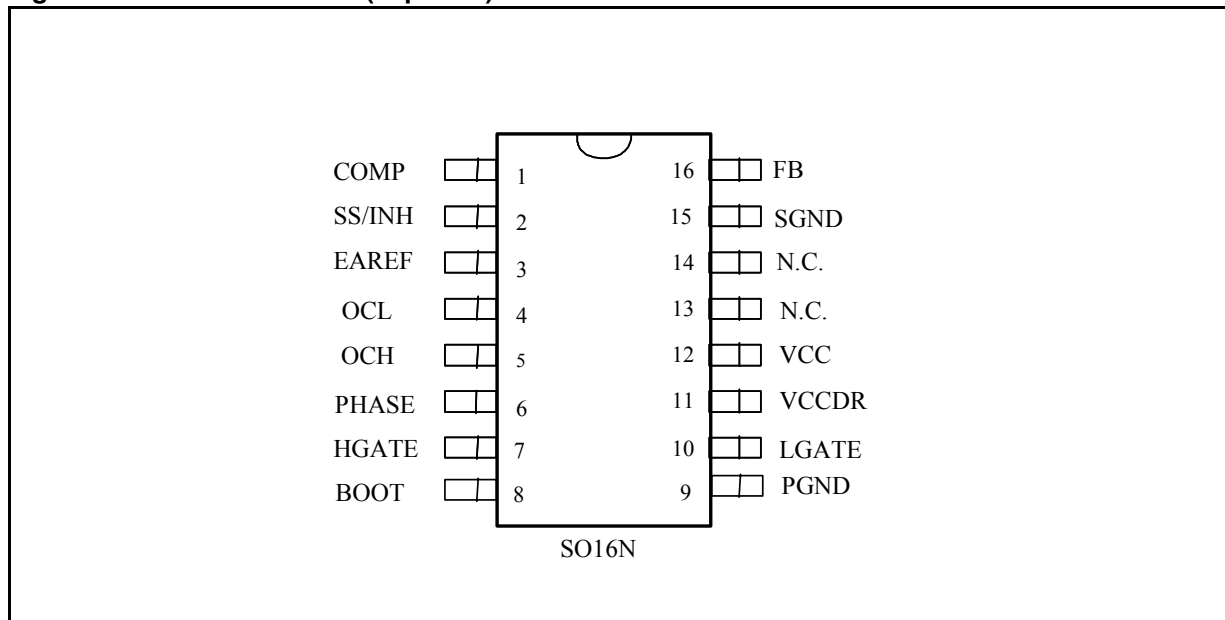
Figure 2.   Pins connection (Top view)


```
              COMP  ⊏⊐  1          16  ⊏⊐  FB
            SS/INH  ⊏⊐  2          15  ⊏⊐  SGND
             EAREF  ⊏⊐  3          14  ⊏⊐  N.C.
               OCL  ⊏⊐  4          13  ⊏⊐  N.C.
               OCH  ⊏⊐  5          12  ⊏⊐  VCC
             PHASE  ⊏⊐  6          11  ⊏⊐  VCCDR
             HGATE  ⊏⊐  7          10  ⊏⊐  LGATE
              BOOT  ⊏⊐  8           9  ⊏⊐  PGND
```

                            SO16N

Table 3.   Pin functions

Pin n.	Name	Function
15	SGND	All the internal references are referred to this pin.
16	FB	This pin is connected to the error amplifier inverting input. Connect it to V_{OUT} through the compensation network. This pin is also used to sense the output voltage in order to manage the over voltage protection.
1	COMP	This pin is connected to the error amplifier output and is used to compensate the voltage control feedback loop.
2	SS/INH	The soft-start time is programmed connecting an external capacitor from this pin to GND. The internal current generator forces a current of 10µA through the capacitor. When the voltage at this pin is lower than 0.5V the device is disabled.
3	EAREF	By setting the voltage at this pin is possible to select the internal/external reference and the switching frequency: V_{EAREF} 0-80% of V_{CCDR} -> External Reference/F_{SW} = 250KHz V_{EAREF} = 80% - 95% of V_{CCDR} -> V_{REF} = 0.6V/F_{SW} = 500KHz V_{EAREF} = 95% - 100% of V_{CCDR} -> V_{REF} = 0.6V/F_{SW} = 250KHz An internal clamp limits the maximum V_{EAREF} at 2.5V (typ.). The device captures the analog value present at this pin at the start-up when V_{CC} meets the UVLO threshold.

Table 3.   Pin functions

4	OCL	A resistor connected from this pin to ground sets the valley- current-limit. The valley current is sensed through the low-side MOSFET(s). The internal current generator sources a current of 100μA (I_{OCL}) from this pin to ground through the external resistor (R_{OCL}). The over-current threshold is given by the following equation: $$I_{VALLEY} = \frac{I_{OCL} \cdot R_{OCL}}{2 \cdot R_{DSonLS}}$$
5	OCH	A resistor connected from this pin and the high-side MOSFET(s) drain sets the peak-current-limit. The peak current is sensed through the high-side MOSFET(s). The internal 100μA current generator (I_{OCH}) sinks a current from the drain through the external resistor (R_{OCH}). The over-current threshold is given by the following equation: $$I_{PEAK} = \frac{I_{OCH} \cdot R_{OCH}}{R_{DSonHS}}$$
6	PHASE	This pin is connected to the source of the high-side MOSFET(s) and provides the return path for the high-side driver. This pin monitors the drop across both the upper and lower MOSFET(s) for the current limit together with OCH and OCL.
7	HGATE	This pin is connected to the high-side MOSFET(s) gate.
8	BOOT	Through this pin is supplied the high-side driver. Connect a capacitor from this pin to the PHASE pin and a diode from V_{CCDR} to this pin (cathode versus BOOT).
9	PGND	This pin has to be connected closely to the low-side MOSFET(s) source in order to reduce the noise injection into the device.
10	LGATE	This pin is connected to the low-side MOSFET(s) gate.
11	V_{CCDR}	5V internally regulated voltage. It is used to supply the internal drivers. Filter it to ground with a 1uF ceramic cap.
12	V_{CC}	Supply voltage pin. The operative supply voltage range is from 4.5V to 14V.

4 Electrical characteristics

V_{CC} = 12V, T_A = 25°C unless otherwise specified.

Table 4.   Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} SUPPLY CURRENT						
I_{CC}	V_{CC} Stand By current	SS to GND		7	9	mA
	V_{CC} quiescent current	HG = open, LG = open, PH=open		8.5	10	
Power-ON						
V_{CC}	Turn-ON V_{CC} threshold	V_{OCH} = 1.7V	4.0	4.2	4.4	V
	Turn-OFF V_{CC} threshold	V_{OCH} = 1.7V	3.6	3.8	4.0	V
$V_{IN\ OK}$	Turn-ON V_{OCH} threshold		1.1	1.25	1.47	V
	Turn-OFF V_{OCH} threshold		0.9	1.05	1.27	V
V_{CCDR} Regulation						
	V_{CCDR} voltage	V_{CC} =5.5V to 14V I_{DR} = 1mA to 100mA	4.5	5	5.5	V
Soft Start and Inhibit						
I_{SS}	Soft Start Current	SS = 2V	7	10	13	µA
		SS = 0 to 0.5V	20	30	45	
Oscillator						
f_{OSC}	Accuracy		237	250	263	KHz
			450	500	550	KHz
ΔV_{OSC}	Ramp Amplitude			2.1		V
Output Voltage						
V_{FB}	Output Voltage		0.597	0.6	0.603	V

Table 4.   Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Error Amplifier						
R_{EAREF}	EAREF Input Resistance	Vs. GND	70	100	150	kΩ
I_{FB}	I.I. bias current	$V_{FB} = 0V$		0.290	0.5	μA
Ext Ref Clamp			2.3			V
V_{OFFSET}	Error amplifier offset	Vref = 0.6V	-5		+5	mV
G_V	Open Loop Voltage Gain	Guaranteed by design		100		dB
GBWP	Gain-Bandwidth Product	Guaranteed by design		10		MHz
SR	Slew-Rate	COMP = 10pF Guaranteed by design		5		V/μs
Gate Drivers						
R_{HGATE_ON}	High Side Source Resistance	$V_{BOOT} - V_{PHASE} = 5V$		1.7		Ω
R_{HGATE_OFF}	High Side Sink Resistance	$V_{BOOT} - V_{PHASE} = 5V$		1.12		Ω
R_{LGATE_ON}	Low Side Source Resistance	$V_{CCDR} = 5V$		1.15		Ω
R_{LGATE_OFF}	Low Side Sink Resistance	$V_{CCDR} = 5V$		0.6		Ω
Protections						
I_{OCH}	OCH Current Source	$V_{OCH} = 1.7V$	90	100	110	μA
I_{OCL}	OCL Current Source		90	100	110	μA
OVP	Over Voltage Trip (V_{FB} / V_{EAREF})	V_{FB} Rising $V_{EAREF} = 0.6V$		120		%
		V_{FB} Falling $V_{EAREF} = 0.6V$		117		%

5   Device description

The controller provides complete control logic and protection for flexible and cost-effective DC-DC converters. It is designed to drive N-Channel MOSFETs in a synchronous rectified buck topology. The output voltage of the converter can be precisely regulated down to 600mV with a maximum tolerance of ±0.8%, when the internal reference is used. The device allows also using an external reference (0V to 2.5V) for the regulation. The device provides voltage-mode control. The switching frequency can be set at two different values: 250KHz or 500KHz. The error amplifier features a 10MHz gain-bandwidth-product and 5V/µs slew-rate that permits to realize high converter bandwidth for fast transient response. The PWM duty cycle can range from 0% to 100%. The device protects against over current conditions providing a constant-current-protection during the soft-start phase and entering in HICCUP mode in all the other conditions. The device monitors the current by using the $R_{DS(ON)}$ of both the high-side and low-side MOSFET(s), eliminating the need for a current sensing resistor and guaranteeing an effective over-current-protection in all the application conditions. Other features are over-voltage-protection and thermal shutdown. The device is available in SO16N package.

5.1   Oscillator

The switching frequency can be fixed to two values: 250KHz or 500KHz by setting the proper voltage at the EAREF pin (see *Table 3.* Pins function and section 4.3 Internal and external reference).

5.2   Internal LDO

An internal LDO supplies the internal circuitry of the device. The input of this stage is the V_{CC} pin and the output (5V) is the V_{CCDR} pin. The LDO can be by-passed, providing directly a 5V voltage to V_{CCDR}. In this case V_{CC} and V_{CCDR} pins must be shorted together as shown in *Figure 3*. V_{CCDR} pin must be filtered with a 1uF capacitor to sustain the internal LDO during the recharge of the bootstrap capacitor.

5.3   Bypassing the LDO to avoid the voltage drop with low Vcc

If $V_{CC} \approx$ 5V the internal LDO works in dropout with an output resistance of about 1Ω The maximum LDO output current is about 100mA and so the output voltage drop is 100mV, to avoid this the LDO can be bypassed.

Figure 3.   Bypassing the LDO
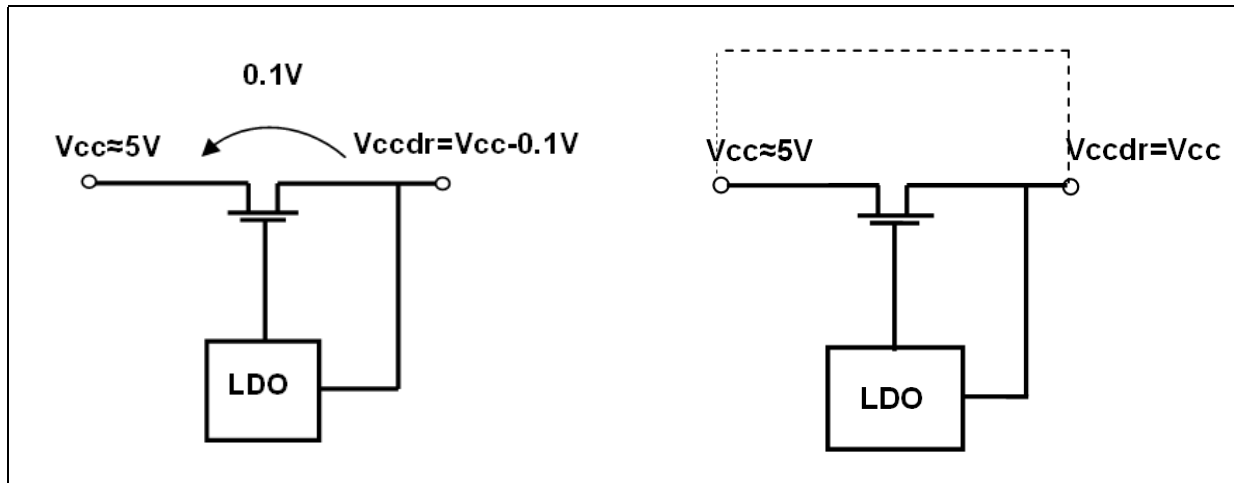
5.4   Internal and external references

It is possible to set the internal/external reference and the switching frequency by setting the proper voltage at the EAREF pin. The maximum value of the external reference depends on the V_{CC}: with V_{CC} = 4V the clamp operates at about 2V (typ.), while with V_{CC} greater than 5V the maximum external reference is 2.5V (typ.).

● V_{EAREF} from 0% to 80% of V_{CCDR} -> External reference/Fsw=250KHz

● V_{EAREF} from 80% to 95% of V_{CCDR} -> V_{REF} = 0.6V/Fsw=500KHz

● V_{EAREF} from 95% to 100% of V_{CCDR} -> V_{REF} = 0.6V/Fsw=250KHz

Providing an external reference from 0V to 450mV the output voltage will be regulated but some restrictions must be considered:

● The minimum OVP threshold is set at 300mV;

● The under-voltage-protection doesn't work;

To set the resistor divider it must be considered that a 100K pull-down resistor is integrated into the device (see *Figure 4.*). Finally it must be taken into account that the voltage at the EAREF pin is captured by the device at the start-up when V_{CC} is about 4V.

5.5 Error amplifier

Figure 4.   Error amplifier reference
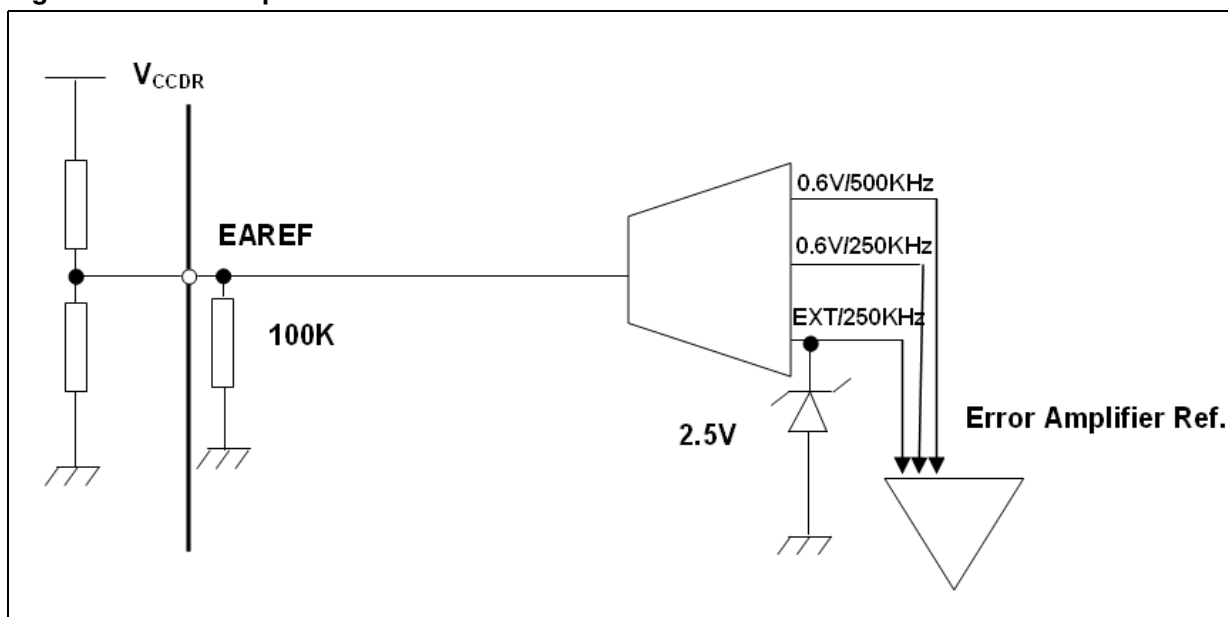
5.6 Soft start

When both V_{CC} and V_{IN} are above their turn-ON thresholds (V_{IN} is monitored by the OCH pin) the start-up phase takes place. Otherwise the SS pin is internally shorted to GND. At start-up, a ramp is generated charging the external capacitor C_{SS} with an internal current generator. The initial value for this current is 35µA and charges the capacitor up to 0.5V. After that it becomes 10µA until the final charge value of approximately 4V (see *Figure 5*.).

Figure 5.   Soft-Start phase.
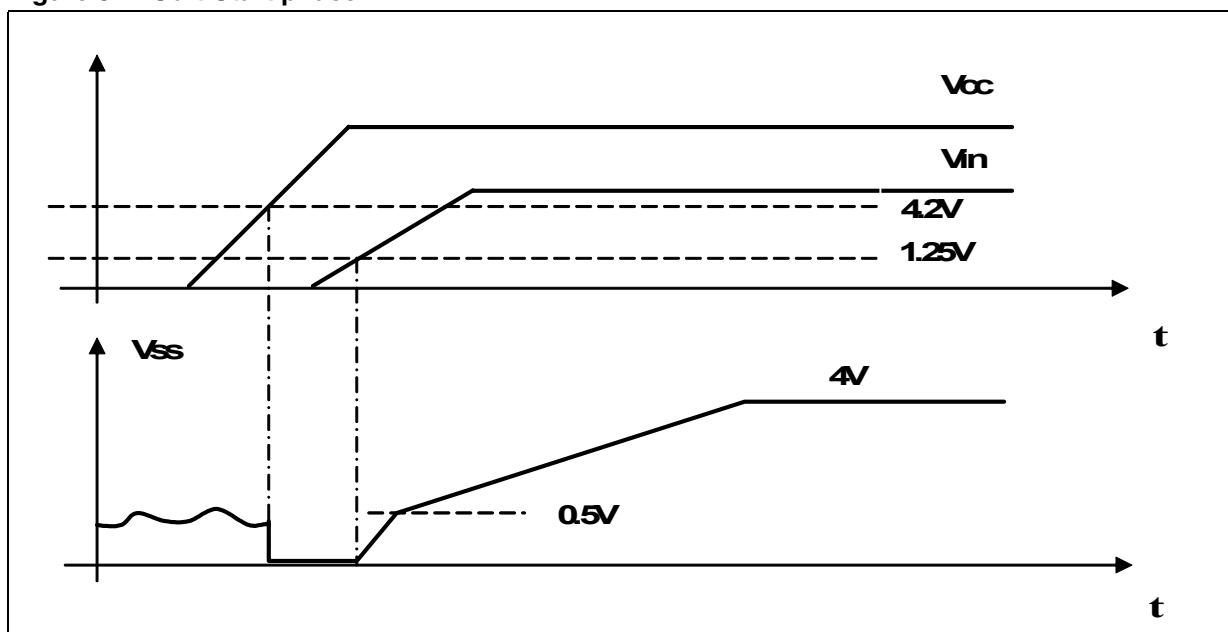
The output of the error amplifier is clamped with this voltage (V_{SS}) until it reaches the programmed value. No switching activity is observable if V_{SS} is lower than 0.5V and both MOSFETs are OFF. When V_{SS} is between 0.5V and 1.1V the low-side MOSFET is turned ON. As V_{SS} reaches 1.1V (i.e. the oscillator triangular wave inferior limit) even the high-side MOSFET begins to switch and the output voltage starts to increase. During the soft-start phase the current can't be reversed in order to allow pre-biased start-up (see *Figure 6.* and *Figure 7.*).

Figure 6.   Start-up without pre-bias
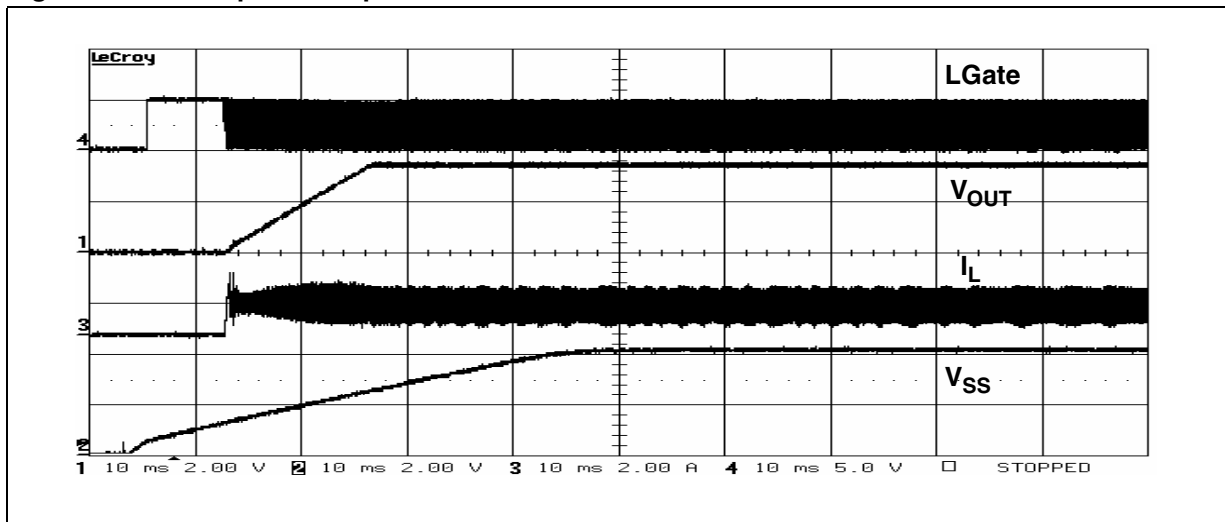
Figure 7.   Start-up with pre-bias
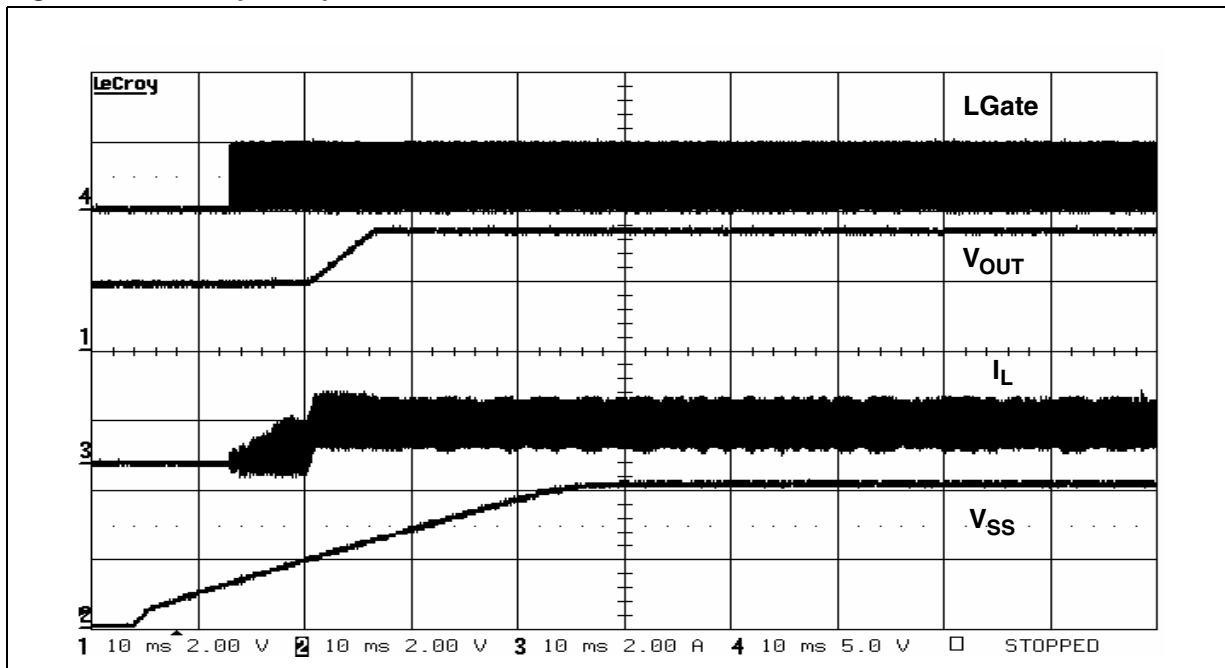
If an over current is detected during the soft-start phase, the device provides a constant-current-protection. In this way, in case of short soft-start time and/or small inductor value and/or high output capacitors value, the converter can start in any case, limiting the current (*Chapter 5.8: Monitoring and protections on page 14*). The soft-start phase ends when Vss reaches 3.5V. After that the over-current-protection triggers the HICCUP mode.

5.7 Driver section

The high-side and low-side drivers allow using different types of power MOSFETs (also multiple MOSFETs to reduce the R_{DSON}), maintaining fast switching transitions. The low-side driver is supplied by V_{CCDR} while the high-side driver is supplied by the BOOT pin. A predictive dead time control avoids MOSFETs cross-conduction maintaining very short dead time duration in the range of 20ns. The control monitors the phase node in order to sense the low-side body diode recirculation. If the phase node voltage is less than a certain threshold (-350mV typ.) during the dead time, it will be reduced in the next PWM cycle. The predictive dead time control doesn't work when the high-side body diode is conducting because the phase node doesn't go negative. This situation happens when the converter is sinking current for example and, in this case, an adaptive dead time control operates.

5.8 Monitoring and protections

The output voltage is monitored by means of pin FB. The device provides over-voltage-protection: when the voltage sensed on FB pin reaches a value 20% (typ.) greater than the reference the low-side driver is turned on as long as the over voltage is detected (see *Figure 8*).

Figure 8. OVP
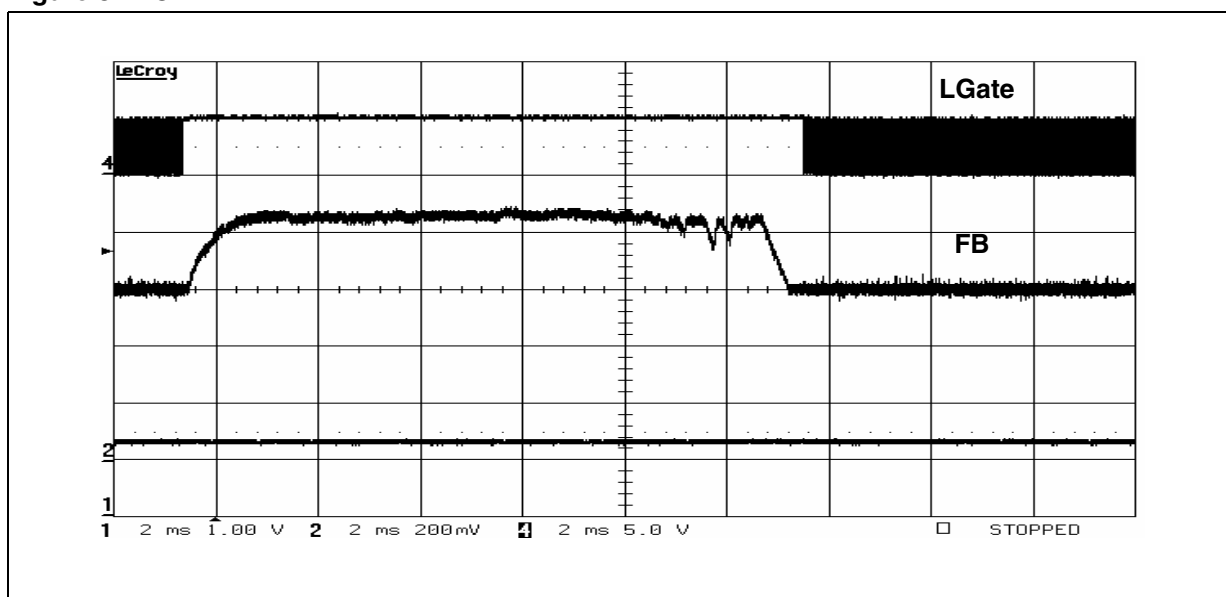
The device realizes the over-current-protection (OCP) sensing the current both on the high-side MOSFET(s) and the low-side MOSFET(s) and so 2 current limit thresholds can be set (see OCH pin and OCL pin in *Table 3: Pin functions*):

● Peak Current Limit
● Valley Current Limit

The Peak Current Protection is active when the high-side MOSFET(s) is turned on, after a masking time of 100ns. The valley-current-protection is enabled when the low-side MOSFET(s) is turned on after a masking time of 500ns. If, when the soft-start phase is completed, an over current event occurs during the on time (peak-current-protection) or during the off time (valley-current-protection) the device enters in HICCUP mode: the high-side and low-side MOSFET(s) are turned off, the soft-start capacitor is discharged with a constant current of 10µA and when the voltage at the SS pin reaches 0.5V the soft-start phase restarts (see *Figure 9*).

5.9   Hiccup mode

Figure 9.   Constant current and Hiccup Mode during an OCP.
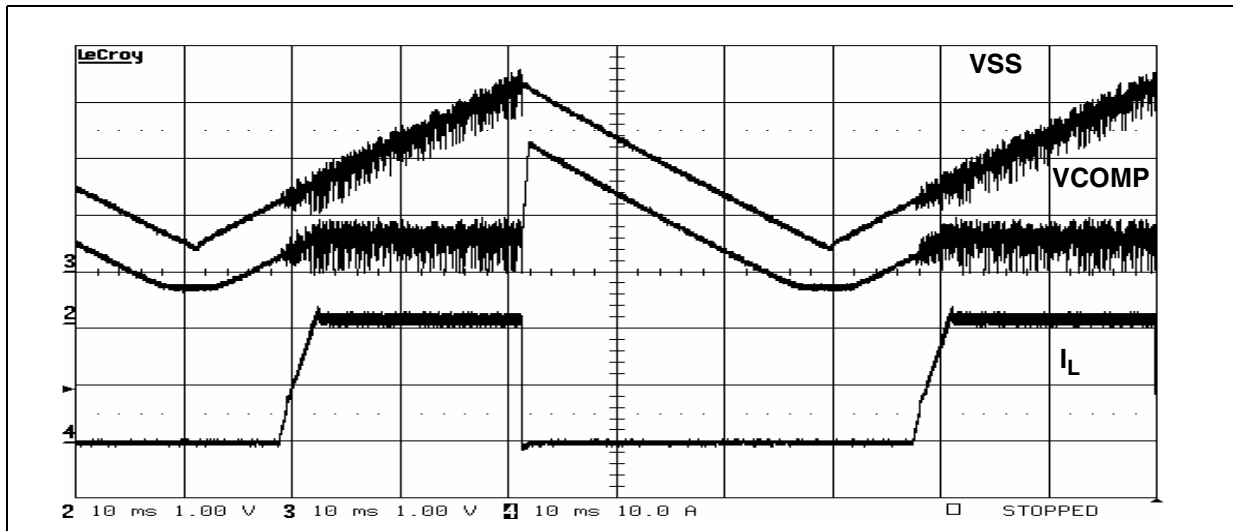
During the soft-start phase the OCP provides a constant-current-protection. If during the T_{ON} the OCH comparator triggers an over current the high-side MOSFET(s) is immediately turned OFF (after the masking time and the internal delay) and returned on at the next pwm cycle. The limit of this protection is that the T_{ON} cannot be less than masking time plus propagation delay, because during the masking time the peak-current-protection is disabled. In case of very hard short circuit, even with this short T_{ON}, the current could escalate. The valley-current-protection is very helpful in this case to limit the current. If during the off-time the OCL comparator triggers an over current, the high-side MOSFET(s) is not turned on until the current is over the valley-current-limit. This implies that, if it is necessary, some pulses of the high-side MOSFET(s) will be skipped, guaranteeing a maximum current due to the following formula:

$$I_{MAX} = I_{VALLEY} + \frac{Vin - Vout}{L} \cdot T_{ON,MIN} \quad (1)$$

5.10   Thermal shutdown

When the junction temperature reaches 150°C ±10°C the device enters in thermal shutdown. Both MOSFETs are turned OFF and the soft-start capacitor is rapidly discharged with an internal switch. The device does not restart until the junction temperature goes down to 120°C and, in any case, until the voltage at the soft-start pin reaches 500mV.

6   Application details

6.1   Inductor design

The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current. The inductance value can be calculated with the following relationship:

$$L \cong \frac{Vin - Vout}{Fsw \cdot \Delta I_L} \cdot \frac{Vout}{Vin} \quad (2)$$

Where F_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage. *Figure 10* shows the ripple current vs. the output voltage for different values of the inductor, with V_{IN} = 5V and V_{IN} = 12V at a switching frequency of 500KHz.

Figure 10.   Inductor current ripple.
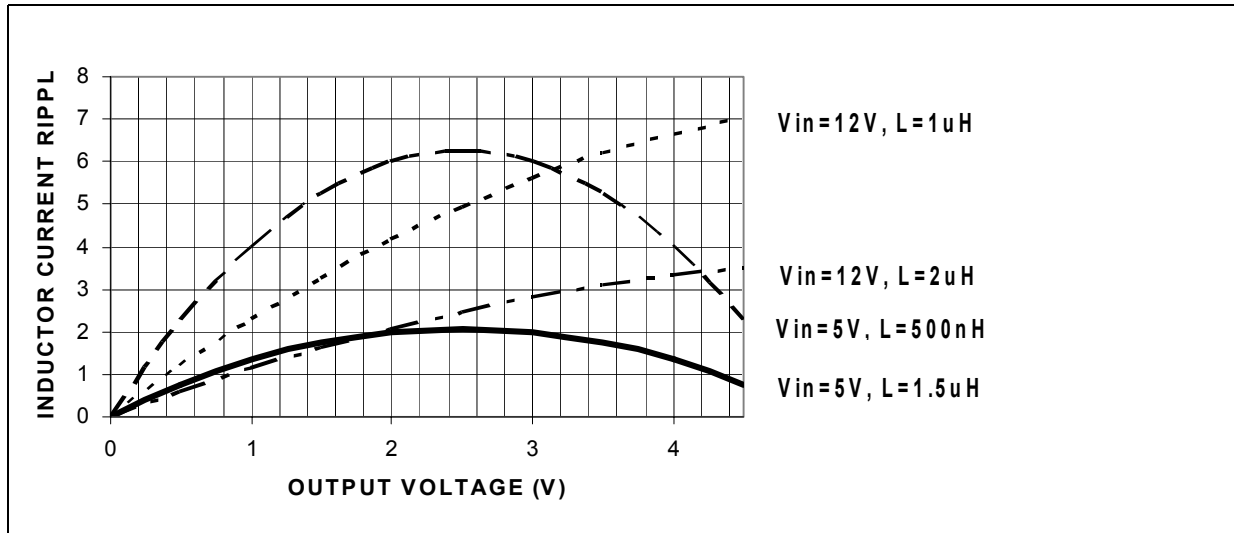
Increasing the value of the inductance reduces the ripple current but, at the same time, increases the converter response time to a load transient. If the compensation network is well designed, during a load transient the device is able to set the duty cycle to 100% or to 0%. When one of these conditions is reached, the response time is limited by the time required to change the inductor current. During this time the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitor size.

6.2 Output capacitors

The output capacitors are basic components for the fast transient response of the power supply. For example, during a positive load transient, they supply the current to the load until the converter reacts. The controller recognizes immediately the load transient and sets the duty cycle at 100%, but the current slope is limited by the inductor value. The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta Vout_{ESR} = \Delta Iout \cdot ESR \quad (3)$$

Moreover, there is an additional drop due to the effective capacitor discharge that is given by:

$$\Delta Vout_{COUT} = \frac{\Delta Iout^2 \cdot L}{2 \cdot Cout \cdot (Vin, \min \cdot D\max - Vout)} \quad (4)$$

Where D_{MAX} is the maximum duty cycle value that in the L6725 is 100%. Usually the voltage drop due to the ESR is the biggest one while the drop due to the capacitor discharge is almost negligible. Moreover the ESR value also affects the voltage static ripple, that is:

$$\Delta Vout = ESR \cdot \Delta I_L \quad (5)$$

6.3 Input capacitors

The input capacitors have to sustain the RMS current flowing through them, that is:

$$Irms = Iout \cdot \sqrt{D \cdot (1-D)} \quad (6)$$

Where D is the duty cycle. The equation reaches its maximum value, $I_{OUT}/2$ with D = 0.5. The losses in worst case are:

$$P = ESR \cdot (0.5 \cdot Iout)^2 \quad (7)$$

6.4   Compensation network

The loop is based on a voltage mode control (*Figure 11*). The output voltage is regulated to the internal/external reference voltage and scaled by the external resistor divider. The error amplifier output V_{COMP} is then compared with the oscillator triangular waveform to provide a pulse-width modulated (PWM) with an amplitude of V_{IN} at the PHASE node. This waveform is filtered by the output filter. The modulator transfer function is the small signal transfer function of V_{OUT}/V_{COMP}. This function has a double pole at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at F_{ESR} depending on the output capacitor's ESR. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage: V_{OSC}.

Figure 11. Compensation Network
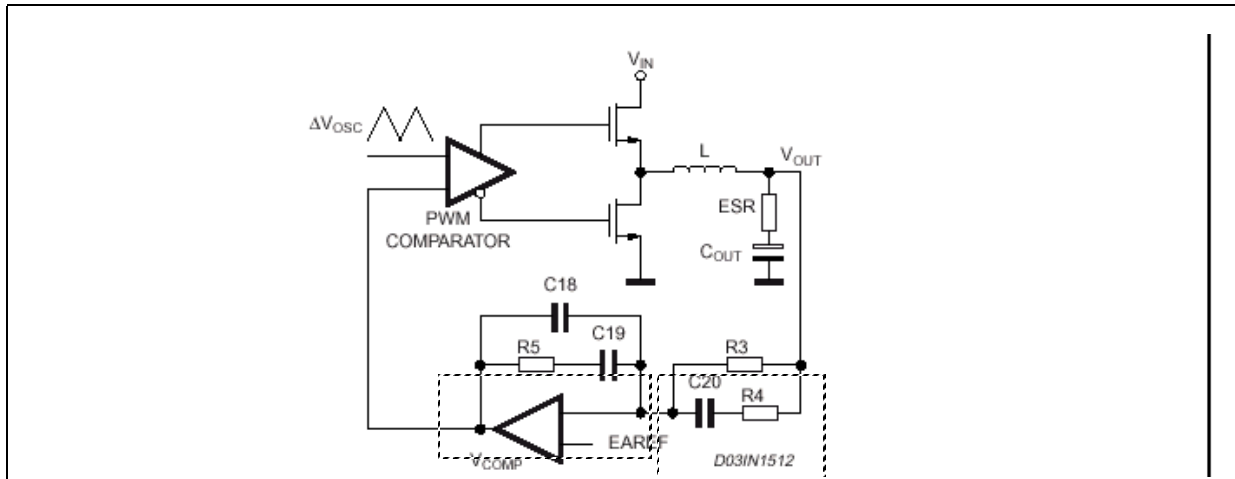
The compensation network consists in the internal error amplifier, the impedance networks Z_{IN} (R3, R4 and C20) and Z_{FB} (R5, C18 and C19). The compensation network has to provide a closed loop transfer function with the highest 0dB crossing frequency to have fastest transient response (but always lower than $f_{SW}/10$) and the highest gain in DC conditions to minimize the load regulation error. A stable control loop has a gain crossing the 0dB axis with -20dB/decade slope and a phase margin greater than 45°. To locate poles and zeroes of the compensation networks, the following suggestions may be used:

● Modulator singularity frequencies:

$$\omega_{LC} = \frac{1}{\sqrt{L \cdot Cout}} \quad (8) \qquad \omega_{ESR} = \frac{1}{ESR \cdot Cout} \quad (9)$$

● Compensation network singularity frequencies:

$$\omega_{P1} = \frac{1}{R_5 \cdot \left(\dfrac{C_{18} \cdot C_{19}}{C_{18} + C_{19}} \right)} \quad (10) \qquad \omega_{P2} = \frac{1}{R_4 \cdot C_{20}} \quad (11)$$

$$\omega_{Z1} = \frac{1}{R_5 \cdot C_{19}} \quad (12) \qquad \omega_{Z2} = \frac{1}{C_{20} \cdot (R_3 + R_4)} \quad (13)$$

● Compensation network design:

    – Put the gain R_5/R_3 in order to obtain the desired converter bandwidth:

$$\varpi_C = \frac{R_5}{R_3} \cdot \frac{Vin}{\Delta Vosc} \cdot \varpi_{LC} \quad (14)$$

    – Place ω_{Z1} before the output filter resonance ω_{LC};

    – Place ω_{Z2} at the output filter resonance ω_{LC};

    – Place ω_{P1} at the output capacitor ESR zero ω_{ESR};

    – Place ω_{P2} at one half of the switching frequency;

    – Check the loop gain considering the error amplifier open loop gain.

Figure 12. Asymptotic Bode plot of Converter's open loop gain
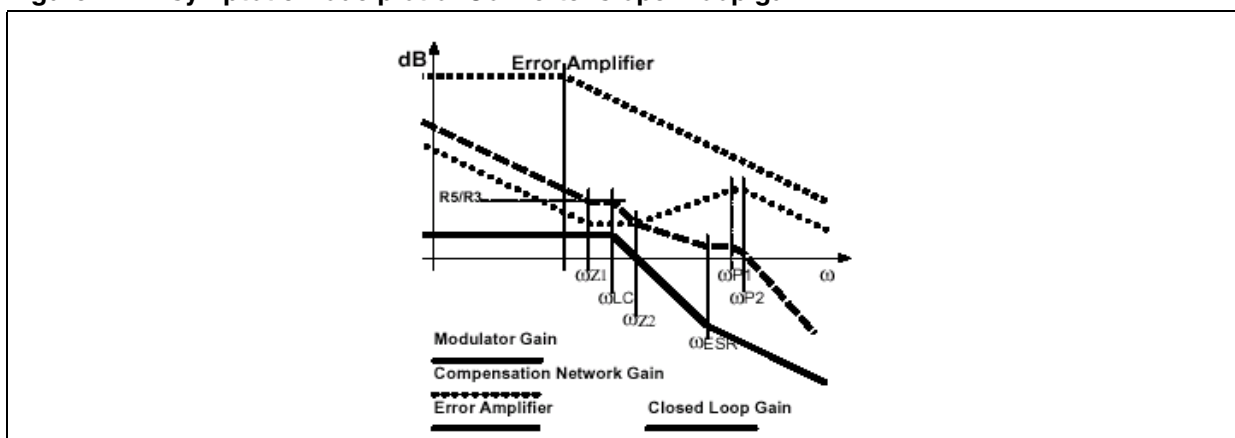
7   L6725 demoboard

7.1   Description

L6725 demoboard realizes in a four layer PCB a step-down DC/DC converter and shows the operation of the device in a general purpose application. The input voltage can range from 4.5V to 14V and the output voltage is at 3.3V. The module can deliver an output current in excess of 20A. The switching frequency is set at 250 KHz (controller free-running F_{SW}) but it can be set to 500KHz acting on the EAREF pin.

Figure 13.   Demoboard schematic
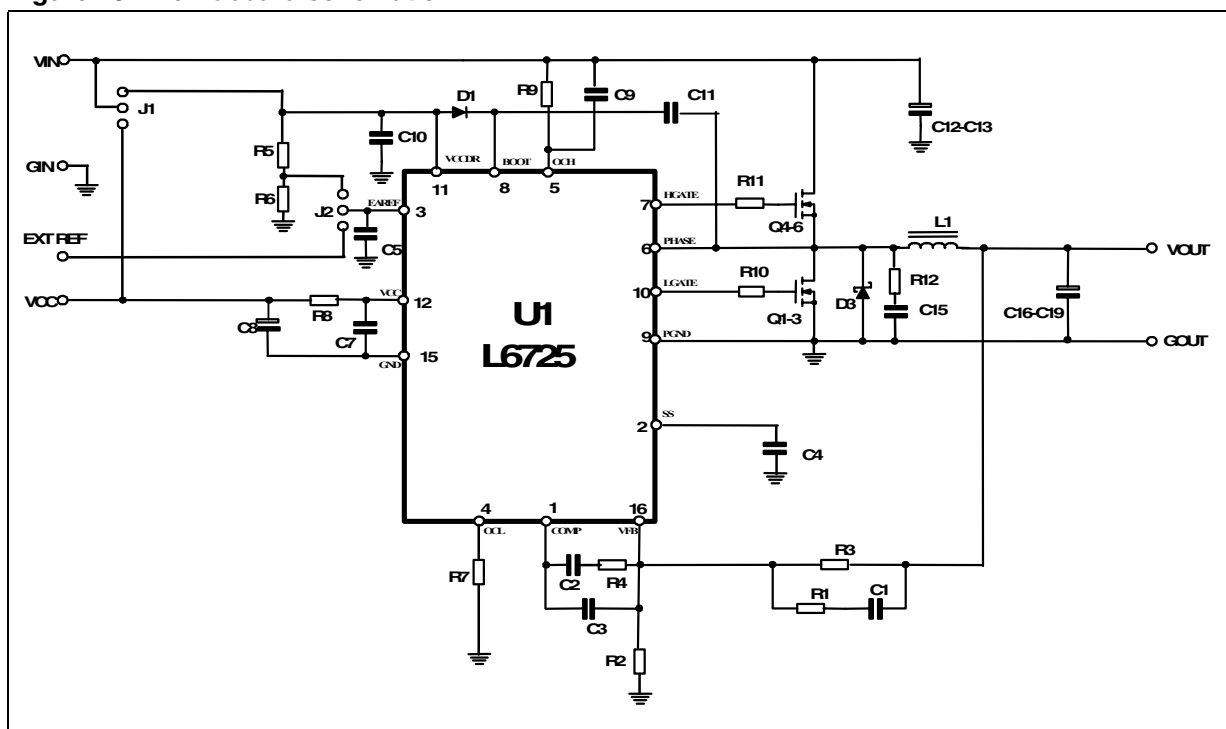
Table 5.   Demoboard part list

Reference	Value	Manufacturer	Package	Supplier
R1	1kΩ	Neohm	SMD 0603	IFARCAD
R2	1kΩ	Neohm	SMD 0603	IFARCAD
R3	4K7			
R4	2k7	Neohm	SMD 0603	IFARCAD
R5	0Ω	Neohm	SMD 0603	IFARCAD
R6	N.C.	Neohm	SMD 0603	IFARCAD
R7	2K	Neohm	SMD 0603	IFARCAD
R8	10Ω	Neohm	SMD 0603	IFARCAD
R9	1K5	Neohm	SMD 0603	IFARCAD
R10	2.2Ω	Neohm	SMD 0603	IFARCAD

Table 5.   Demoboard part list

R11	2.2Ω	Neohm	SMD 0603	IFARCAD
R12	N.C.	Neohm	SMD 0603	IFARCAD
C1	4.7nF	Kemet	SMD 0603	IFARCAD
C2	47nF	Kemet	SMD 0603	IFARCAD
C3	1nF	Kemet	SMD 0603	IFARCAD
C4	100nF	Kemet	SMD 0603	IFARCAD
C5	100nF	Kemet	SMD 0603	IFARCAD
C6	N.C.	/	/	/
C7	100nF	Kemet	SMD 0603	IFARCAD
C8	4.7uF 20V	AVX	SMA6032	IFARCAD
C9	1nF	Kemet	SMD 0603	IFARCAD
C10	1uF	Kemet	SMD 0603	IFARCAD
C11	220nF	Kemet	SMD 0603	IFARCAD
C12-13	3X 15uF	/	/	ST (TDK)
C15	N.C.	/	/	/
C16-19	2X 330μF	/	/	ST (poscap)
L1	1.8μH	Panasonic	SMD	ST
D1	STPS1L30M	ST	DO216AA	ST
D3	N.C.	/	/	/
Q1-Q2	STS12NH3LL	ST	SO8	ST
Q4-Q5	STS25NH3LL	ST	SO8	ST
U1	L6725	ST	SO16N	ST

Table 6.   Other inductor manufacturer

Manufacturer	Series	Inductor Value (μH)	Saturation Current (A)
WURTH ELEKTRONIC	744318180	1.8	20
SUMIDA	CDEP134-2R7MC-H	2.7	15
EPCOS	HPI_13 T640	1.4	22
TDK	SPM12550T-1R0M220	1	22
TOKO	FDA1254	2.2	14
COILTRONICS	HCF1305-1R0	1.15	22
	HC5-1R0	1.3	27

Table 7.   Other capacitor manufacturer

Manufacturer	Series	Capacitor value(μF)	Rated voltage (V)
TDK	C4532X5R1E156M	15	25
	C3225X5R0J107M	100	6.3
NIPPON CHEMI-CON	25PS100MJ12	100	25
PANASONIC	ECJ4YB0J107M	100	6.3

Figure 14.   Demoboard efficiency
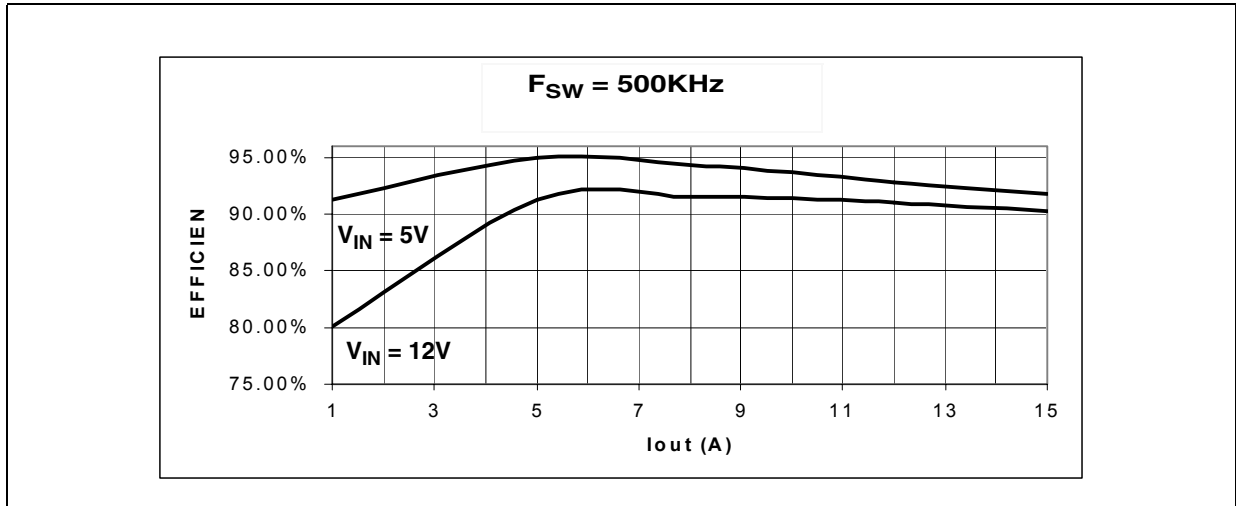
Figure 15.   PCB Layout: Top Layer
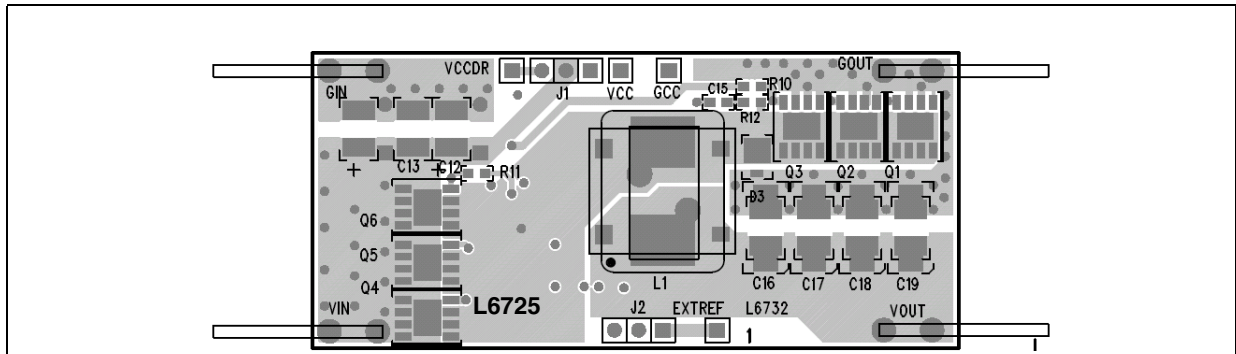
Figure 16.   PCB Layout: Power Ground Layer
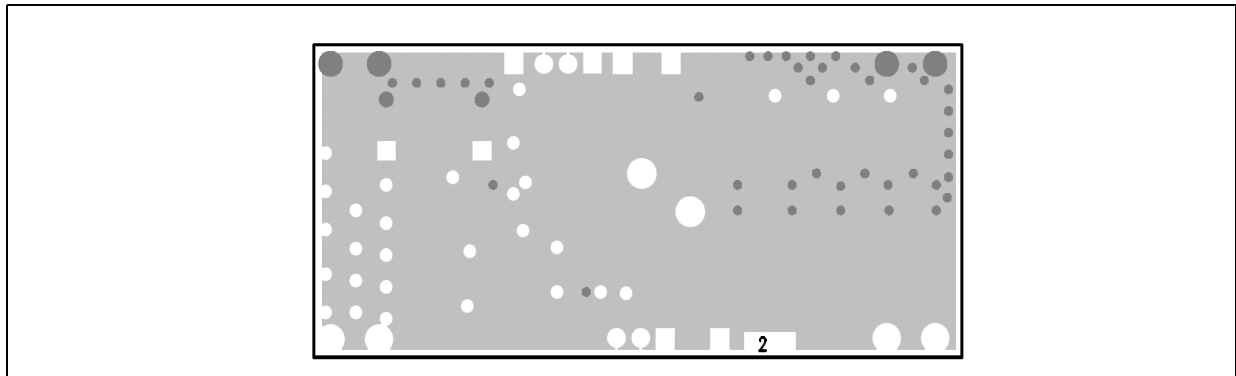
Figure 17. PCB Layout: Signal-Ground Layer
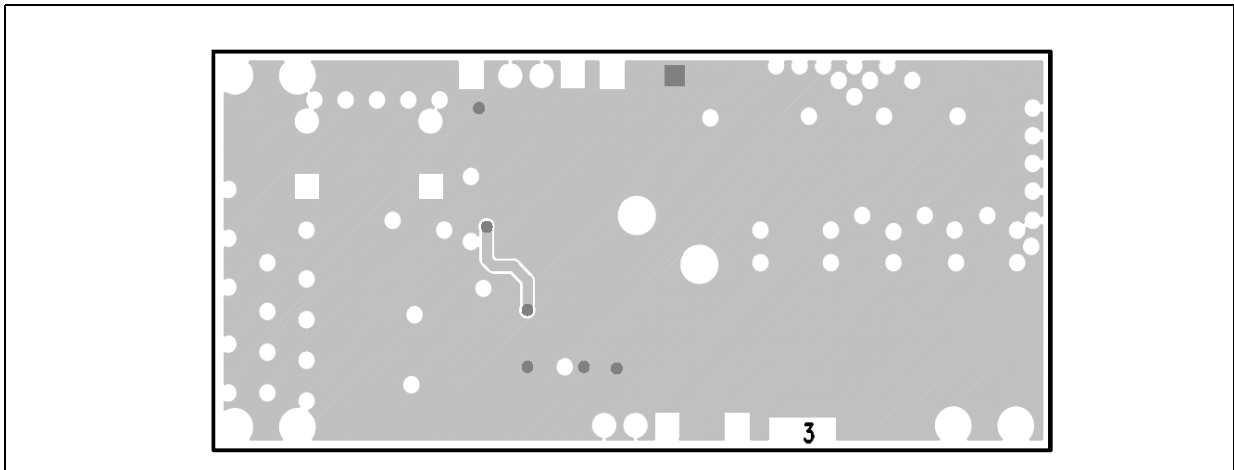
Figure 18. PCB Layout: Bottom Layer
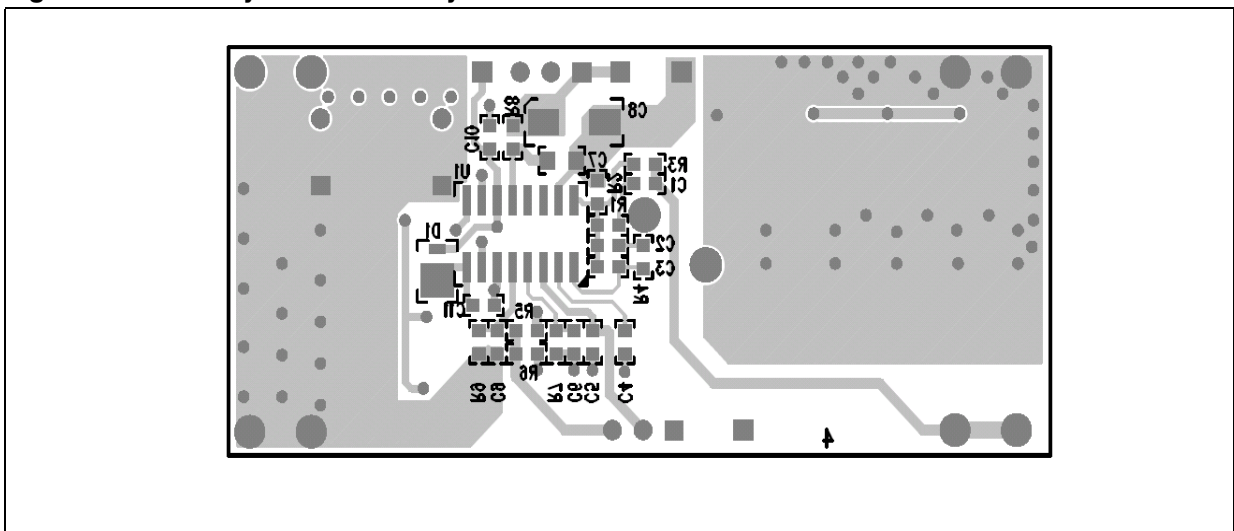
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 8.　SO16N mechanical data

Dim.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D[1]	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F[1]	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 °(max.)					

1. "D" and "F" do not include mold flash or protrusions -Mold flash or protrusions shall not exceed 0.15mm (.006inc.)

Figure 19.　Package dimensions
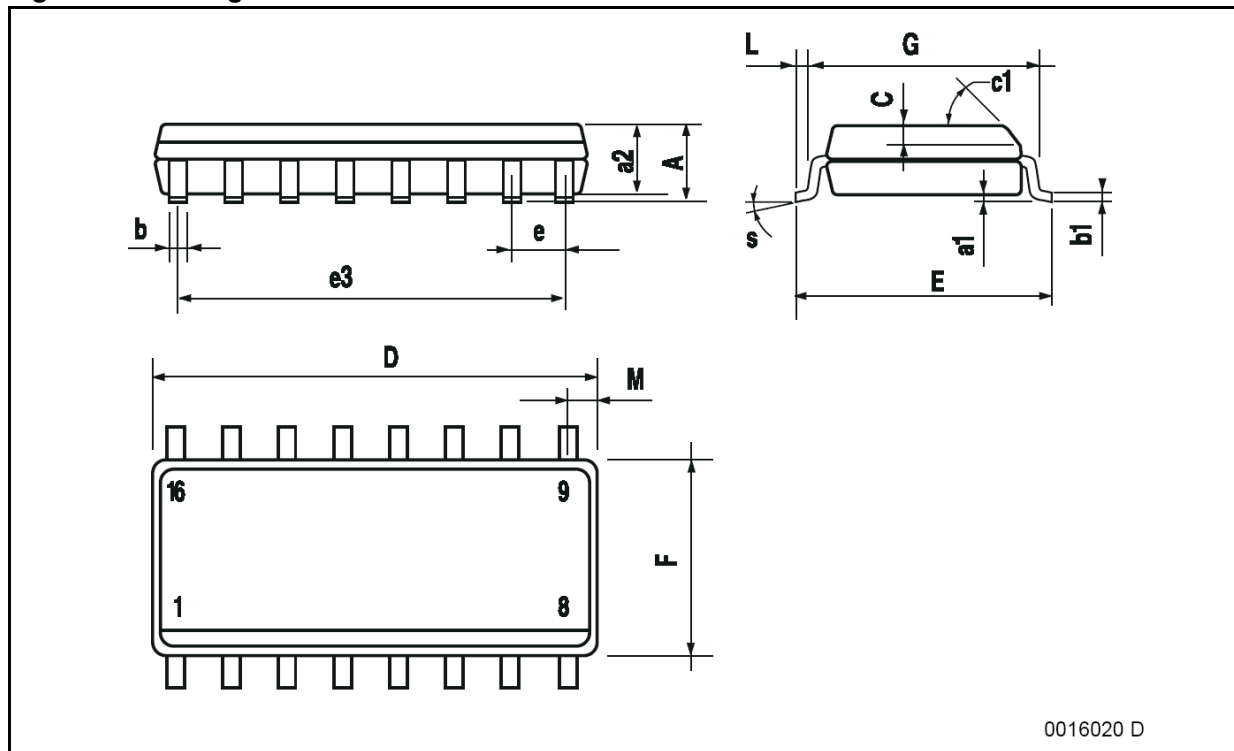
0016020 D

9 Revision history

Table 9. **Revision history**

Date	Revision	Changes
20-Dec-2005	1	Initial release.
30-May-2006	2	New template, thermal data updated
26-Jun-2006	3	Note page 5 deleted

Please Read Carefully: