GS1574A HD-LINX® II Adaptive Cable Equalizer

Features

- SMPTE 292M and SMPTE 259M compliant
- Automatic cable equalization
- Multi-standard operation from 143Mb/s to 1.485Gb/s
- Supports DVB-ASI at 270Mb/s
- Small footprint (4mm x 4mm)
- Pb-free and RoHS compliant
- Manual bypass (useful for low data rates with slow rise/fall times)
- Performance optimized for 270Mb/s and 1.485Gb/s
- Typical maximum equalized length of Belden 1694A cable: 140m at 1.485Gb/s, 350m at 270Mb/s
- 50Ω differential output (with internal 50Ω pull-ups)
- Manual output mute or programmable mute based on max cable length adjust
- Single 3.3V power supply operation
- Operating temperature range: 0°C to +70°C

Applications

- SMPTE 292M and SMPTE 259M Coaxial Cable Serial Digital Interfaces.

Description

The GS1574A is a second-generation high-speed BiCMOS integrated circuit designed to equalize and restore signals received over 75Ω co-axial cable.

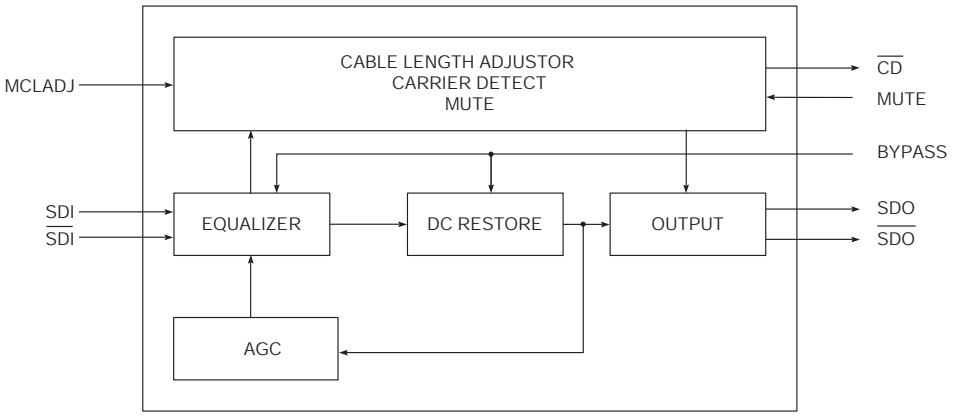
The GS1574A is designed to support SMPTE 292M and SMPTE 259M, and is optimized for performance at 270Mb/s and 1.485Gb/s.

The GS1574A features DC restoration to compensate for the DC content of SMPTE pathological test patterns.

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS1574A output when an approximate selected cable length is reached for SMPTE 259M signals. This feature allows the GS1574A to distinguish between low amplitude SD-SDI signals and noise at the input of the device. The serial digital outputs of the GS1574A may be forced to a mute state by applying a voltage to the MUTE pin.

Power consumption is typically 215mW using a 3.3V power supply. The GS1574A is lead-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



GS1574A Functional Block Diagram

Contents

1. Pin Out

1.1 GS1574A Pin Assignment

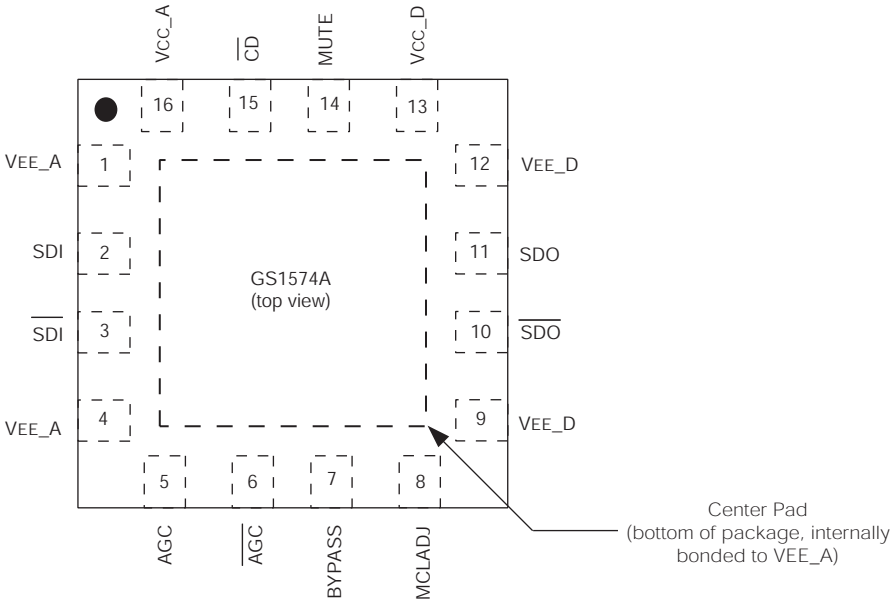


Figure 1-1: 16-Pin QFN

1.2 GS1574A Pin Descriptions

Table 1-1: GS1574A Pin Descriptions

Pin Number	Name	Timing	Type	Description
1, 4	VEE_A	Analog	Power	Most negative power supply for analog circuitry. Connect to GND.
2, 3	SDI, $\overline{SDI}$	Analog	Input	Serial digital differential input.
5, 6	AGC, $\overline{AGC}$	Analog	–	External AGC capacitor. Connect pin 5 and pin 6 together as shown in the Typical Application Circuit on page 13.
7	BYPASS	Not Synchronous	Input	Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode.
8	MCLADJ	Analog	Input	Maximum cable length adjust. Adjusts the approximate maximum amount of cable to be equalized (from 0m to the maximum cable length). The output is muted (latched to the last state) when the maximum cable length is achieved. NOTE: MCLADJ is only recommended for data rates up to 360Mb/s. For data rates above this, MCLADJ should be left floating.

Table 1-1: GS1574A Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
9	VEE_D	Analog	Power	Most negative power supply for the digital circuitry and output buffer. Connect to GND.
10, 11	$\overline{\text{SDO}}$, SDO	Analog	Output	Equalized serial digital differential output.
12	VEE_D	Analog	Power	Most negative power supply for the digital circuitry and output buffer. Connect to GND.
13	VCC_D	Analog	Power	Most positive power supply for the digital I/O pins of the device. Connect to +3.3V DC.
14	MUTE	Not Synchronous	Input	CONTROL SIGNAL INPUT levels are LVCMOS/LVTTL compatible. (3.3V Tolerant) When the MUTE pin is set HIGH by the application interface, the serial digital output of the device will be forced to a steady state. When the MUTE pin is set LOW, the serial digital output of the device will be active. NOTE: This pin may be connected directly to the $\overline{\text{CD}}$ pin to allow mute on loss of carrier.
15	$\overline{\text{CD}}$	Not Synchronous	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence of a good input signal. When the $\overline{\text{CD}}$ pin is LOW, a good input signal has been detected. When this pin is HIGH, the input signal is invalid. This pin will indicate loss of carrier for data rates > 19Mb/s.
16	VCC_A	Analog	Power	Most positive power supply for the analog circuitry of the device. Connect to +3.3V DC.
–	Center Pad	–	Power	Internally bonded to VEE_A.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to +3.6 V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V	±5%
Power Consumption	P_D	T_A = 25°C	–	215	–	mW	–
Supply Current	I_s	T_A = 25°C	–	65	–	mA	–
Output Common Mode Voltage	V_{CMOUT}	T_A = 25°C	–	V_{CC} - ΔV_{SDO}/2	–	V	–
Input Common Mode Voltage	V_{CMIN}	T_A = 25°C	–	1.75	–	V	–
MCLADJ DC Voltage (to mute signal)	–	0m, T_A = 25°C	–	1.3	–	V	–
MCLADJ Range	–	T_A = 25°C	–	0.5	–	V	–
$\overline{CD}$ Output Voltage	$V_{\overline{CD}(OH)}$	Carrier not present	2.4	–	–	V	–
	$V_{\overline{CD}(OL)}$	Carrier present	–	–	0.4	V	–
Mute Input Voltage Required to Force Outputs to Mute	V_{Mute}	Min to Mute	2.0	–	–	V	–
Mute Input Voltage Required to Force Outputs Active	V_{Mute}	Max to Activate	–	–	0.8	V	–

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	143	–	1485	Mb/s	–
Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential	720	800	950	mV_{p-p}	1
Output Voltage Swing	ΔV_{SDO}	100Ω load, T_A =25°C, differential	–	750	–	mV_{p-p}	–
Maximum Equalized Cable Length	–	270Mb/s, Belden 1694A, 350m	–	0.2	–	UI	2
	–	270Mb/s, Belden 8281, 280m	–	0.2	–	UI	2
	–	1.485Gb/s, Belden 1694A, 140m	–	0.25	–	UI	2
	–	1.485Gb/s, Belden 8281, 100m	–	0.25	–	UI	2
Output Rise/Fall time	–	20% - 80%	–	80	220	ps	–
Mismatch in rise/fall time	–	–	–	–	30	ps	–
Duty cycle distortion	–	–	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–
Input Return Loss	–	–	15	–	–	dB	3
Input Resistance	–	single ended	–	1.64	–	kΩ	–
Input Capacitance	–	single ended	–	1	–	pF	–
Output Resistance	–	single ended	–	50	–	Ω	–

NOTES:

1. 0m cable length.
2. Equalizer Pathological.
3. Tested on CB1574A board from 5MHz to 2GHz.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1. The recommended standard Pb reflow profile is shown in Figure 2-2.

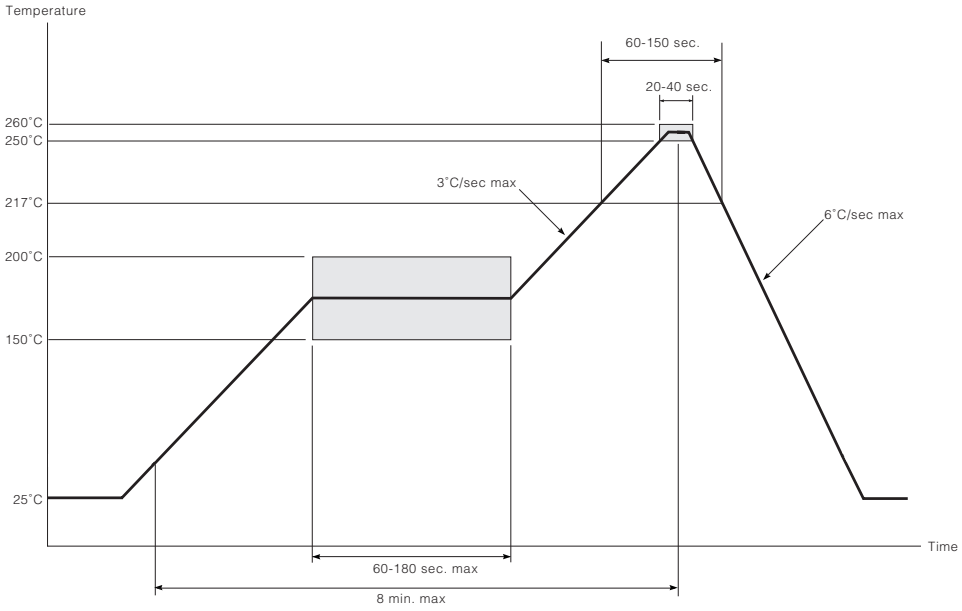


Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

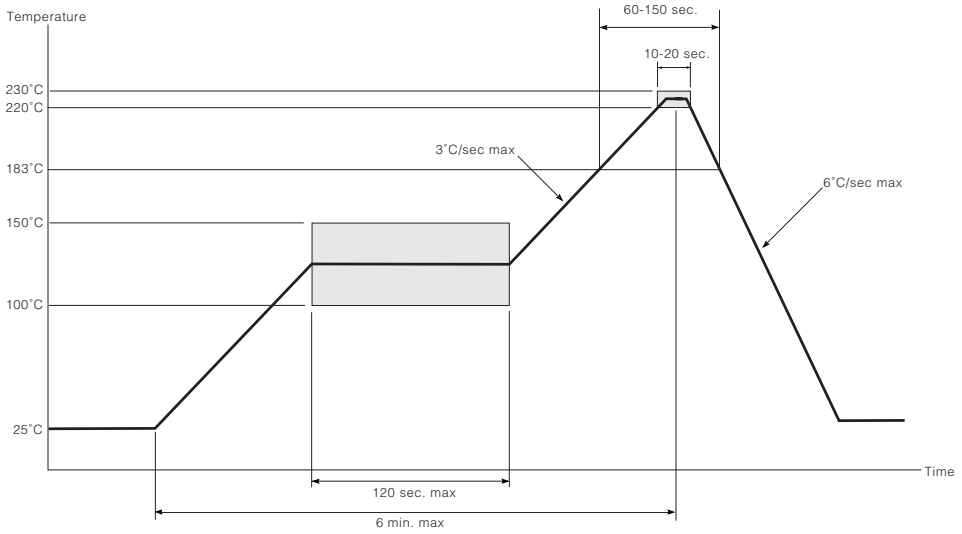


Figure 2-2: Standard Pb Solder Reflow Profile (Pb-free package)

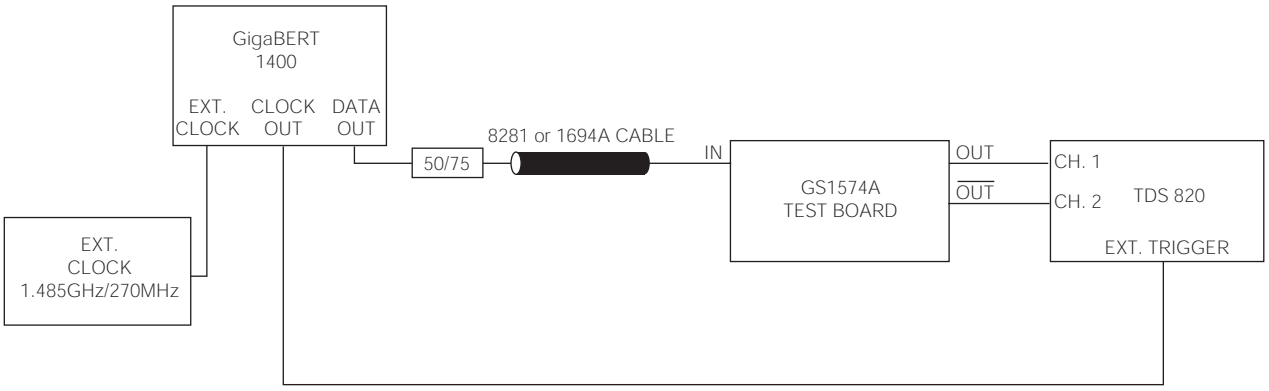


Figure 2-3: Test Circuit

3. Input / Output Circuits

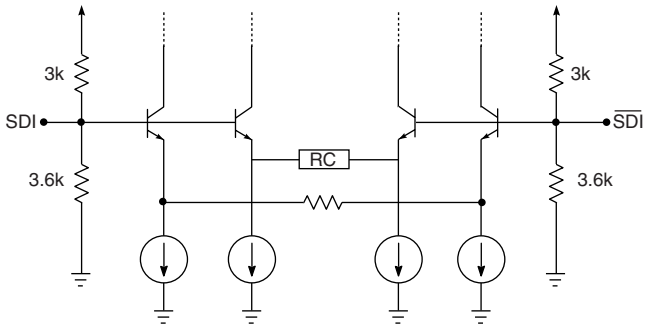


Figure 3-1: Input Equivalent Circuit

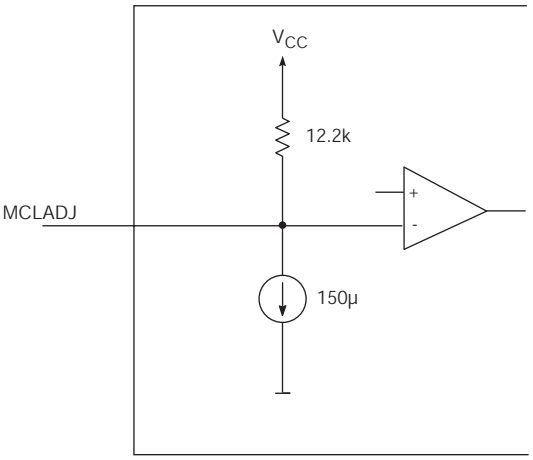


Figure 3-2: MCLADJ Equivalent Circuit

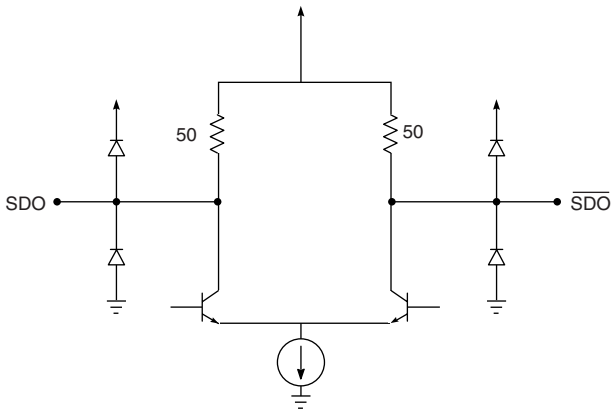


Figure 3-3: Output Circuit

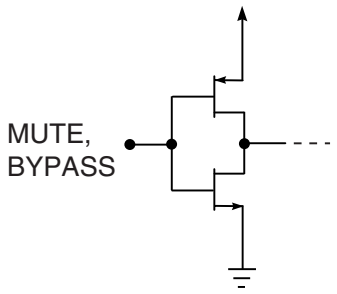


Figure 3-4: MUTE and BYPASS Circuits

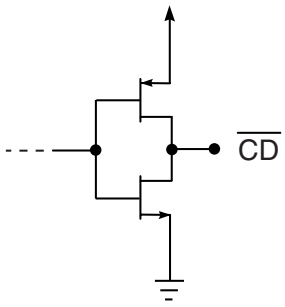


Figure 3-5: $\overline{\text{CD}}$ Circuit

4. Detailed Description

The GS1574A is a high speed BiCMOS IC designed to equalize serial digital signals.

The GS1574A can equalize both HD and SD serial digital signals, and will typically equalize greater than 140m of Belden 1694A cable at 1.485Gb/s and 350m at 270Mb/s.

The GS1574A is powered from a single +3.3V power supply and consumes approximately 215mW of power.

4.1 Serial Digital Inputs

The serial data signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.2 Cable Equalization

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling. The digital output signals have a nominal voltage of 750mV$_{pp}$ differential, or 375mV$_{pp}$ single ended when terminated with 50Ω as shown in Figure 4-1.

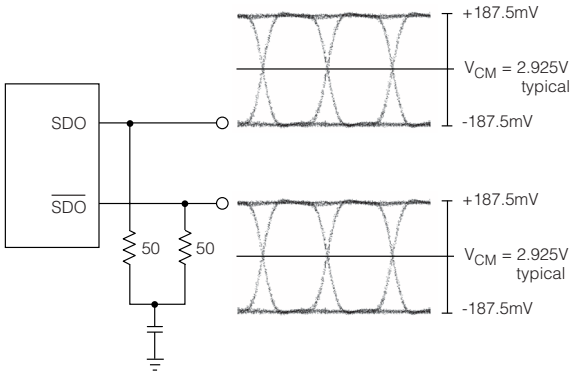


Figure 4-1: Typical Output Voltage Levels

4.3 Programmable Mute Output

For SMPTE 259M inputs, the GS1574A incorporates a programmable threshold output mute (MCLADJ).

In applications where there are multiple input channels using the GS1574A, it is advantageous to have a programmable mute output to avoid signal crosstalk.

The output of the GS1574A can be muted when the input signal decreases below a certain input level. This threshold is determined using the input voltage applied to the MCLADJ pin. The MCLADJ pin may be left unconnected for applications where output muting is not required.

This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference.

NOTE: MCLADJ is only recommended for data rates up to 360Mb/s. For data rates above this, MCLADJ should be left floating.

4.4 Mute and Carrier Detect

The GS1574A includes a MUTE input pin that allows the application interface to mute the serial digital output at any time. Set the MUTE pin HIGH to mute SDO and $\overline{\text{SDO}}$. In this case, the outputs will mute regardless of the setting of the BYPASS pin.

A Carrier Detect output pin ($\overline{\text{CD}}$) indicates the presence of a valid signal at the input of the GS1574A. When $\overline{\text{CD}}$ is LOW, the device has detected a valid input on SDI and $\overline{\text{SDI}}$. When $\overline{\text{CD}}$ is HIGH, the device has not detected a valid input.

NOTE: $\overline{\text{CD}}$ will only detect loss of carrier for data rates greater than 19Mb/s. The $\overline{\text{CD}}$ output pin may be connected directly to the MUTE input pin to enable automatic muting of the GS1574A when no valid input signal has been detected.

NOTE: If the maximum cable length is exceeded and the device is not in bypass mode the GS1574A will not assert the $\overline{\text{CD}}$ pin even if a carrier is present.

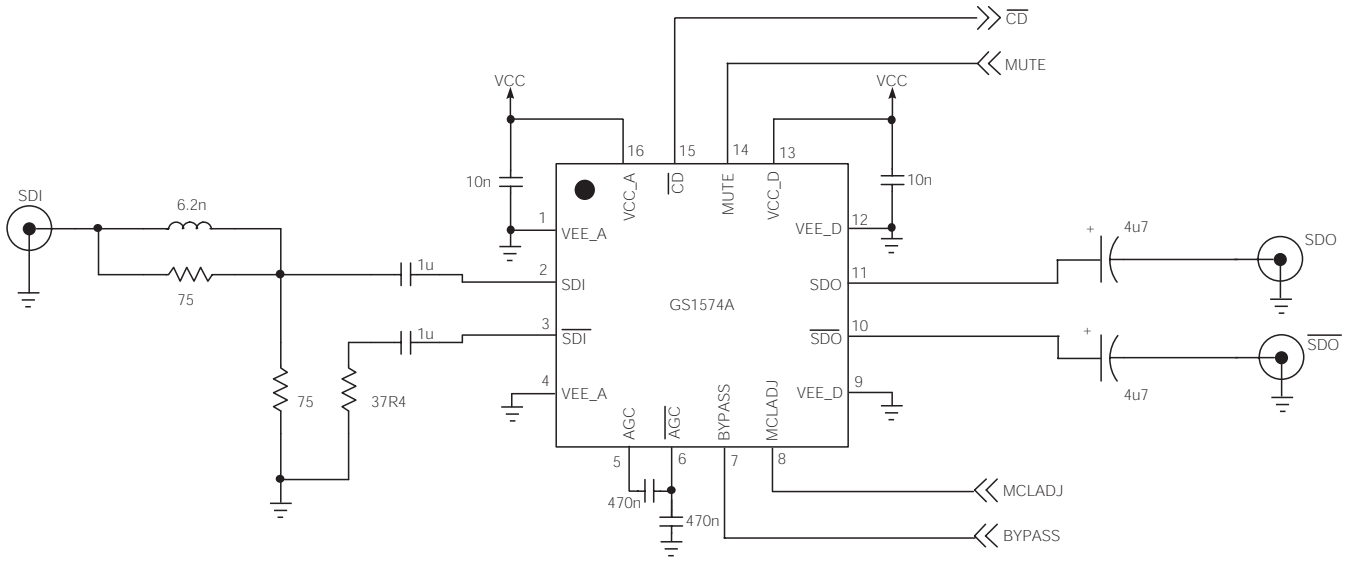
5. Application Information

5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS1574A input components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS1574A output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

5.2 Typical Application Circuit

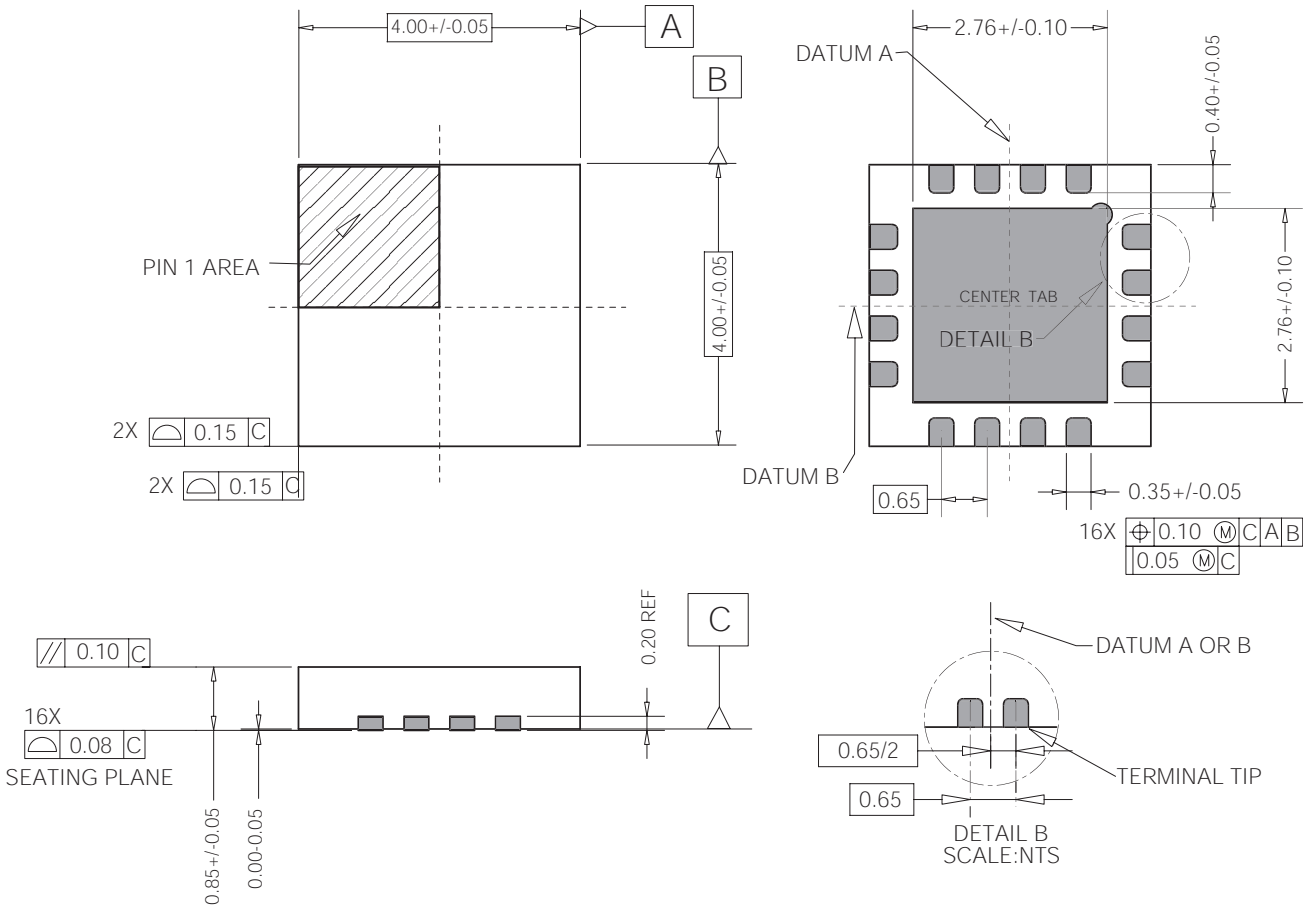


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

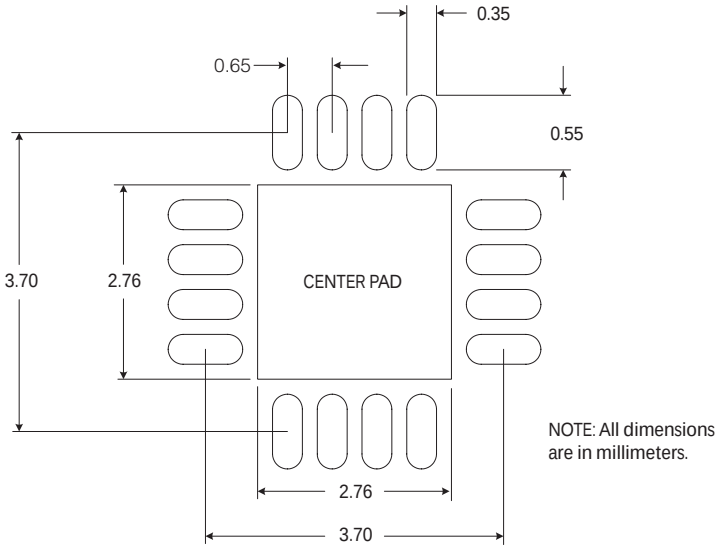
Figure 5-1: GS1574A Typical Application Circuit

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

Note: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi	11.0°C/W
Pb-free and RoHS compliant	Yes

6.4 Ordering Information

	Part Number	Package	Temperature Range
GS1574A	GS1574ACNE3	16-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
0	136149	–	March 2005	Converted to Preliminary Data Sheet. Updated typical application circuit. Updated Input/Output circuits. Updated AC and DC electrical characteristics. Updated description of MUTE and $\overline{CD}$ functionality. Correced minor typing errors. Updated center pad dimensions on PCB footprint.
1	136885	–	May 2005	Corrected description of connection for AGC and $\overline{AGC}$ pins in the Pin Description table. Clarified solder reflow profile descriptions. Corrected minor typing errors.
2	137167	–	June 2005	Rephrased RoHS compliance statement.
3	137321	–	June 2005	Amended notes on use of MCLADJ above 360 Mb/s.
4	137744	–	September 2005	Convert to Data Sheet. Corrected typing errors. Corrected process to BiCMOS.
5	139634	38695	March 2006	Corrected pad standoff height and tolerances for pad width & package dimension. Corrected pad shape.

CAUTION
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